A 4×6.25-Gb/s Serial Link Transmitter Core in 0.18-μm CMOS for high-speed front-end ASICs

Jiacheng Guo, Jiajun Qin, Lei Zhao, Xinyu Bin

State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei City, Anhui Province, China

Jiacheng Guo

1. Background

With the increasing luminosity of high-energy physics experiments and the trend of digitization forward, high-speed serial link is an effective solution for ASICs in front-end readout electronics to deal with the significant increase of data transmission demand, with the advantages of high data bandwidth, few pins and low power consumption.

The high-speed serial link transmitter typically consists of three parts: a phase-locked loop that generates a high frequency clock, serializer for parallel to serial conversion, equalizer for compensating channel loss.

It is reported that the high-speed serial data transmitter has been applied in several pixel readout ASICs, like Timepix3, VeloPix and TaichuPix1. In addition, serial data link has been more widely used in data aggregation ASICs, such as LOCs1, LOCx2, LOCx2-130, GBTX, lpGBT, TDS and GBS20. The highest data rate among the ASICs of two fields are 4×5.12 Gbps and 20.48 Gbps (PAM4).

In this poster, we present a 4×6.25 Gbps serial link transmitter core which achieves the optimal power consumption per Gbps in 0.18 μm CMOS technology while achieving high data throughput bandwidth by optimizing the serializer structure and cell circuits.

2. ASIC ARCHITECTURE

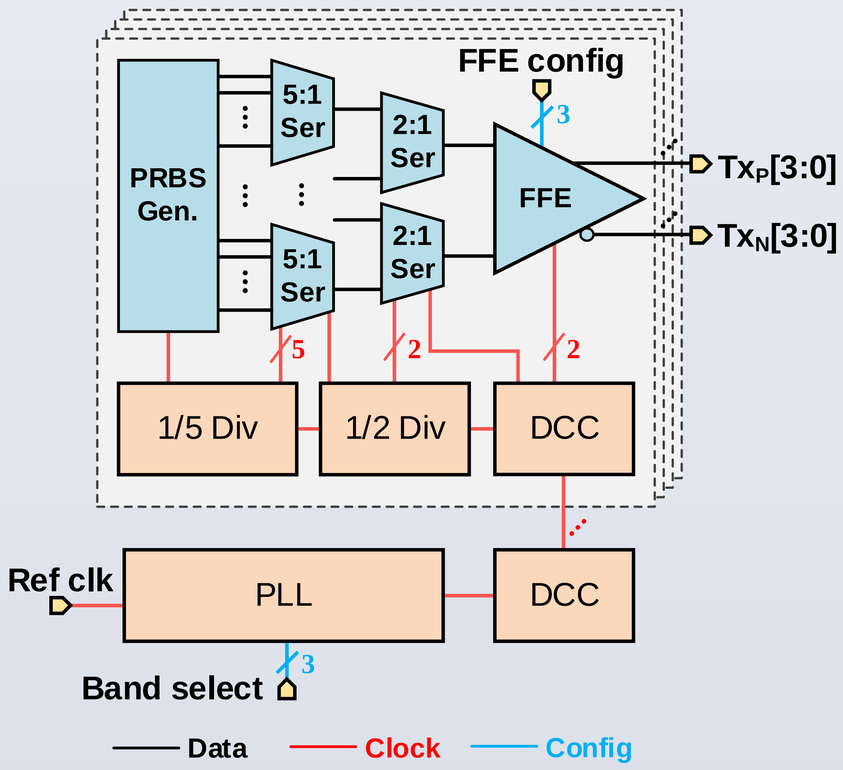


Fig. 1. Block diagram of the prototype ASIC

The overall design block diagram of the transmitter core is shown in Fig. 1. The core consists of a common PLL and four independent transmitter channels. The PLL is based on a 3-stage ring-oscillator, which is used to multiply the frequency of reference clock ten times. The output clock is then buffered to each transmitter channel. Each transmitter channel consists of a 20:2 serializer, a half-rate 2-stage feed-forward equalizer, a clock manager circuit and an embedded PRBS-7 generation circuit for self-test.

The block diagram of the PLL is shown in Fig. 2. In order to optimize the jitter performance, the VCO is composed of 3-stage differential delay cells. The frequency band of VCO is selected by 3 configuration bits. There is about 40% overlap between the adjacent frequency bands, so that the VCO output frequency can be continuously adjustable to support different serial data rate, and the K_{VCO} is small to reduce the phase noise and spurious of PLL.

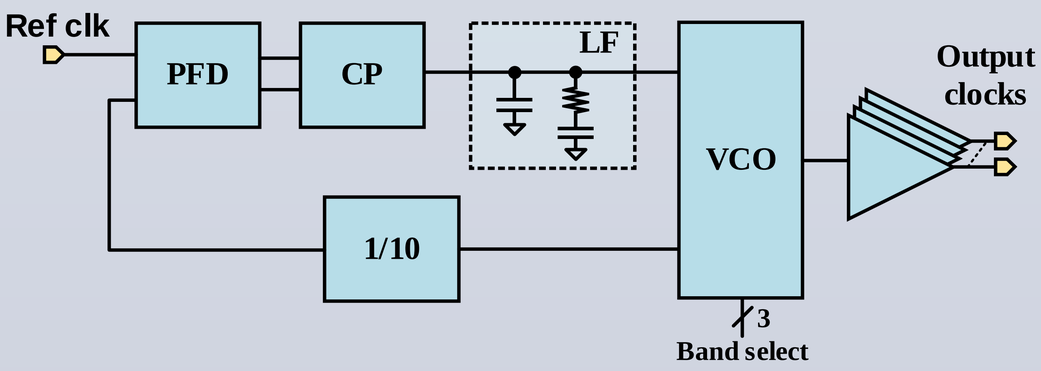


Fig. 2. Block diagram of the PLL

To minimize the power consumption of the serializer, the serialization is divided into three stages. The first stage includes four 5:1 serializers, which adopts multi-phase structure. The second stage consists of two tree structure 2:1 serializers. The final stage is integrated with half-rate feed forward equalizer (FFE), which finishes the last 2:1 serialization and buffers the serial data off-chip. According to the operating frequency of each stage, four different types of latch/flip-flops are utilized. The clock manager circuit provides the multi-phase clocks and half-rate clocks required by each stage.

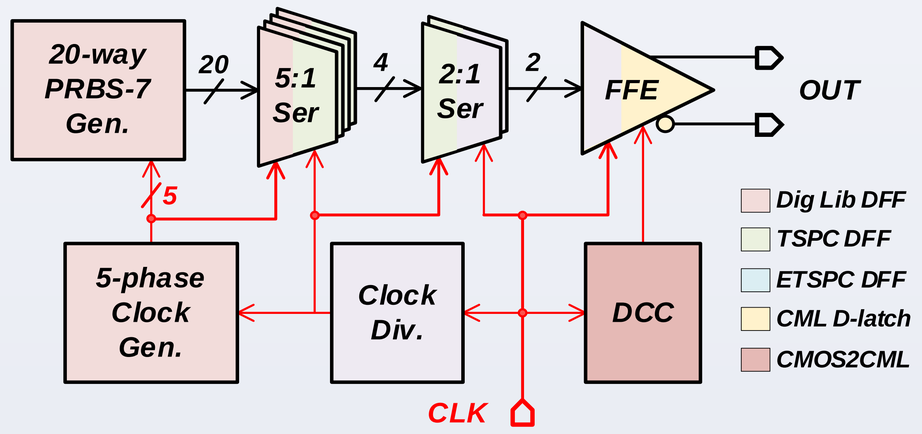
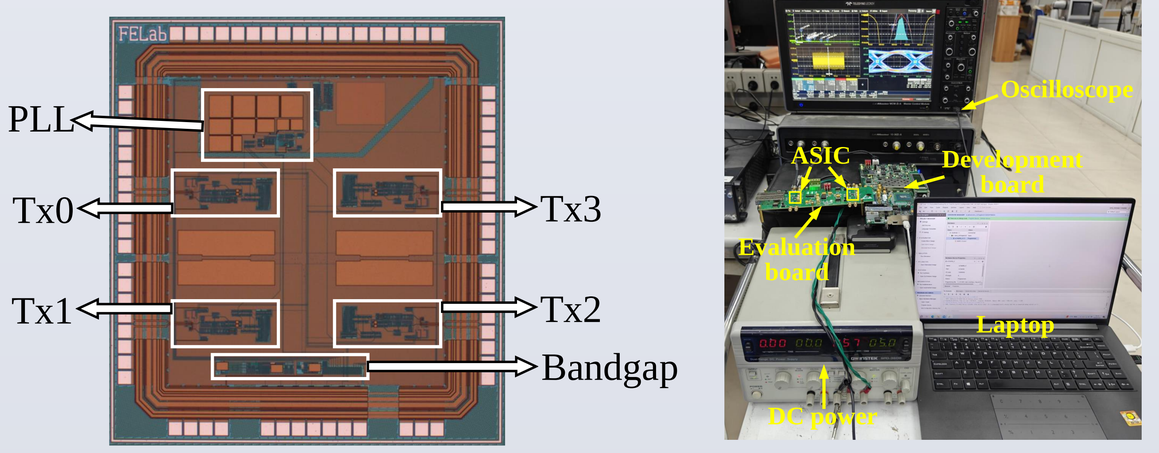


Fig. 3. Block diagram of the transmitter

With the hybrid serialization structure, the maximum operating frequency of the circuit is only half of the serial data rate, which reduces the power consumption of the serializer. The equalization effect of the equalizer is 3-bit configurable to meet the equalization requirements of a wide range of channels.

3. TEST RESULTS

After fabrication of the ASIC, we set up a test platform in the laboratory and conducted a series of tests. Fig. 4 shows the micrograph of the chip and the photograph of the test bench.



(a) Micrograph of the chip (b) Photograph of the test bench

Fig. 4. Micrograph of the chip and photograph of the test bench

Test results show that the transmitter core operates correctly from 3.5 to 6.75 Gbps. Fig. 5 shows serial output ere-diagram at 6.25 Gbps, 3.5 Gbps and 6.75 Gbps captured by the real time oscilloscope (LeCroy LabMaster 10-36Zi-A, 80 Gsps, 36 GHz). At a data rate of 6.25 Gbps, the random jitter (Rj) is 1.007 ps and the total jitter (Tj) of output data is 45.5 ps at a bit error rate of 1×10^{-12}. The output amplitude is differential peak-to-peak 830.3 mV.

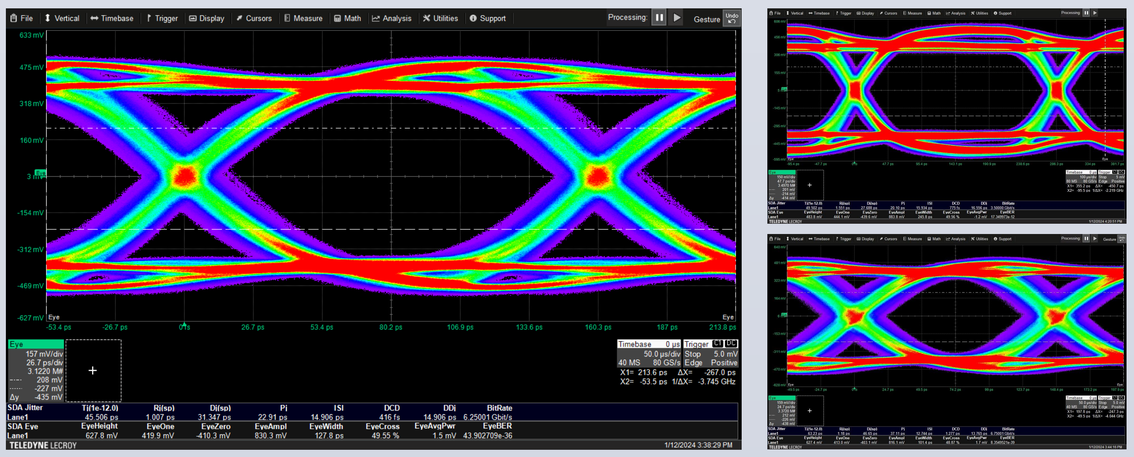


Fig. 5. Eye diagram at 6.25 Gbps (left), 3.5 Gbps (right top), 6.75 Gbps(right bottom)

We connect the serial data to GTP of AC701 development board. After 24-hour testing at 6.25 Gbps (about 5.4×10^{14} bit), no bit error occurred for each channel. Thus, after calculation, the bit-error-rate is less than 1×10^{-14} at 99.54% confidence probability. The other performance of the transmitter core is summarized in Table. 1.

Table. 1. Performance of the transmitter core

Parameter	Value	
Technology	0.18 μm CMOS	
Supply Voltage	1.8 V & 3.3 V	
Data rate	4×6.25 Gbps (3.5~6.75 Gbps)	
Area	PLL	0.12 mm^2
	Transmitter	0.08 mm^2×4
Jitter @6.25 Gbps	PLL	1.006 ps RMS
	Transmitter	45.5 ps @BER=1×10^{-12}
Power @6.25 Gbps	PLL	79 mW
	Transmitter	154 mW×4
	Overall	27.8 mW/Gbps