Real Time Data Acquisition for PET Detector Evaluation based on dual-polarity Charge-to-Digital Converter

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Introduction

Positron emission tomography (PET) systems have been developed very rapidly in recent years. However, the readout electronics system for the PET scanner is usually designed with the ASIC (Application-Specific Integrated Circuit), which has a long period and a huge cost. To design a low-cost and ASIC-free front-end electronics system, a 128-channel front-end electronics (FEE) system, fig.1, based on dual-polarity charge-to-digital converter (dQDC) was proposed. With the dQTC technology, it is feasible to design a multi-channel, high-density and low-power electronics for different radiation detectors. A PET detector was designed to validate its capability of the 128-channel electronics system.

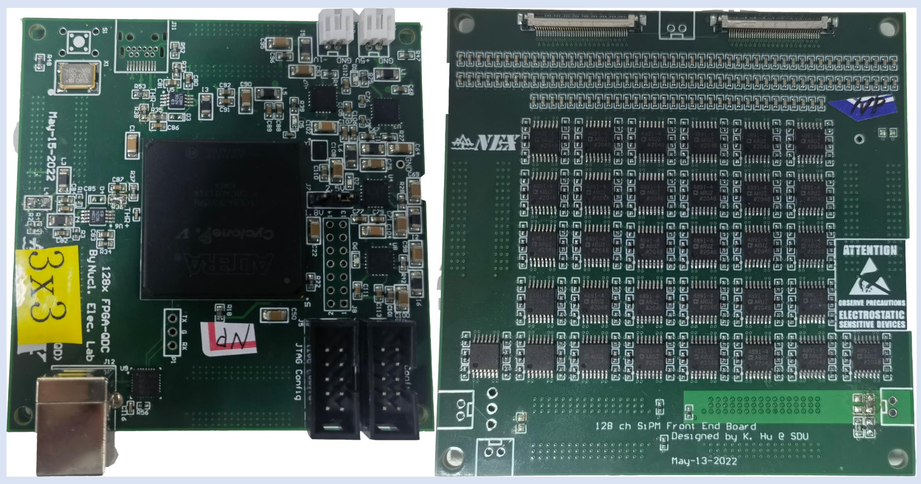

Fig.1 128-channel electronics system

Schematic of PET detector evaluation

This section will introduce the schematic of the PET detector evaluation, as shown in Fig.2(a), which consists of two parts: the detector and the FEE system.

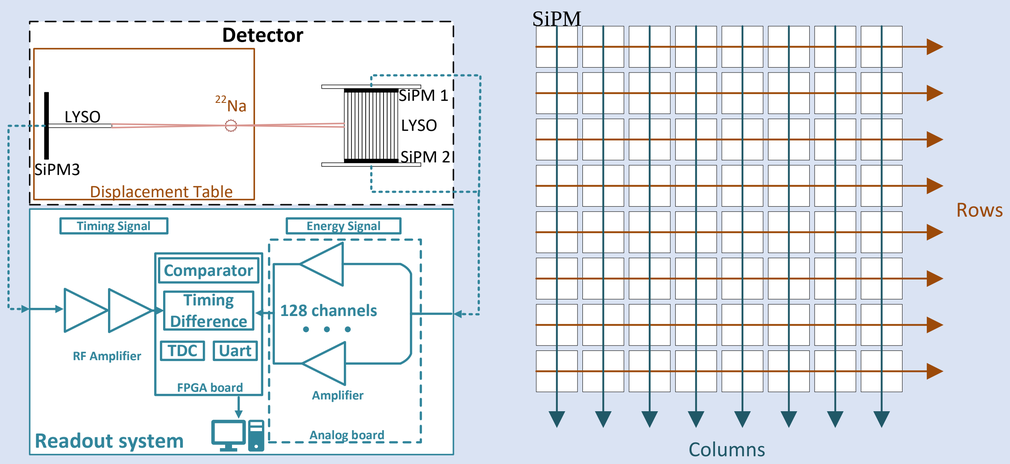

Fig.2 (a) PET system schematic (b) The '8+8' readout scheme schematic

A. Detector

The detector component consists of a 15×15 lutetium-yttrium oxyorthosilicate (LYSO) crystal array with two 8×8 arrays of Silicon photomultiplier (SiPM) arrays coupled to both ends of LYSO array.

To mitigate the complexness of readout electronics for SiPM detector, a row-column summation scheme is used. For comparison, a matrix readout scheme is also used due to sufficient readout channels. 64 SiPM pixels are read out in the matrix readout scheme. Two 8×8 SiPM at two ends of the LYSO array can be read out by the 128-channel FEE system. In the row-column summation scheme, 8 columns of anode signals and 8 rows of cathode signals are connected to form a "8+8" SiPM, as illustrated in Fig. 2(b).

B. Readout system

The FEE readout system consists of an analog board and an FPGA board. The analog board features 128 channels for charge integration; each channel is equipped with two resistors, a capacitance, and an amplifier.

The dual-polarity charge readout method for the analog board is shown on the left side of Fig.3. The cathode current signal flows into the inverting input of the amplifier when the PET detector detects 511 keV γ-photons. The signal is converted to a positive signal and then fed into the FPGA after charge integration. The comparator outputs a logic '1' time pulse when the signal voltage is greater than the V_{thr}, which is set at 50 mV in this work. Then Three State Buffer (TSB) turns high Z state to logic state '1' and the Time to Digital Convertor (TDC) starts to record the time information of the waveform. Due to the virtual-short characteristic of the amplifier, the voltage at the noninverting input is equal to the voltage at the inverting input. The voltage, V_{stage}, is set to ground. Logic '1' from the TSB provides 2.5V to constant-current discharge via R_{dis} until the signal falls below

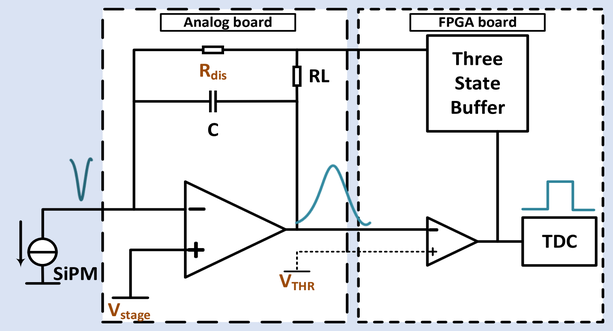

Fig.3 PET system schematic

V_{thr}, after which the circuit resets to initial state. For the positive current signals on the anodes, the V_{stage} is set to be 2.5V and V_{thr} to be 2.45V.

Front-end electronics test

A. Flood image and profile plot

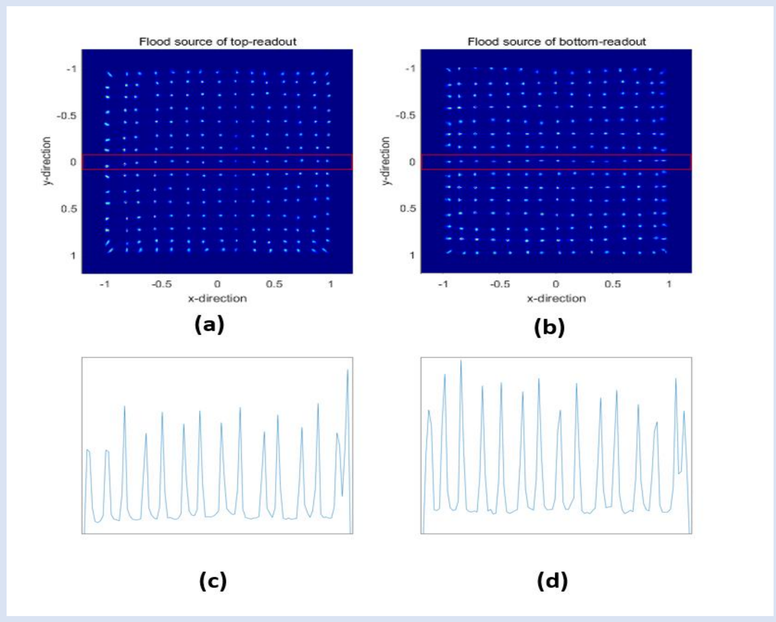

Fig.4 Flood image and profile plot. (a) is the consequence of 128-channel cathode readout method; (b) is the consequence of 8+8 readout method; (c) is profile plot of the center row of the flood image for cathode readout; (d) is profile plot of the center row of the flood image for 8+8 readout.

The flood image at one end of the LYSO array is shown in Fig.4, where all crystal can be distinctly distinguished. The profile plots for the selected row of the crystal array are shown on the bottom of the Fig .4. The PVR values for the two readout schemes are 7.76 and 6.02, respectively.

B. Energy spectrum

For the purpose of energy spectrum comparison, the energy spectra of selected crystals for both readout schemes are plotted in Fig. 5. The energy resolution with 128-channel cathode readout scheme is 13.8%. The energy resolution with 8+8 readout scheme is 13.2%.

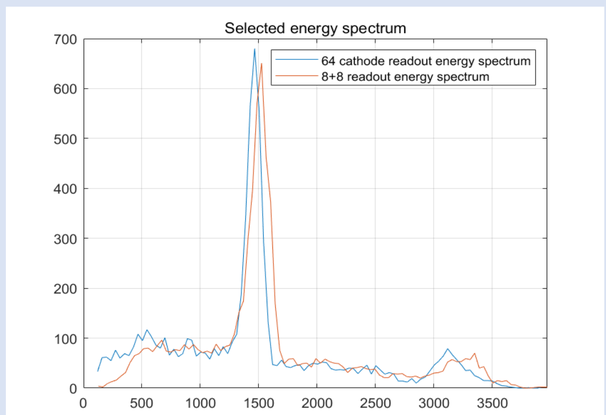

Fig.5 Energy spectrum of two readout scheme

Future work

The results indicate that the FEE in this work has a great readout capability for PET detector. In future work, the timing module (namely TDC) of the FEE system will be developed. The timing evaluation results of the PET detector will be also presented in the meeting.