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System Design and Prototyping of the CMS Level-1 Calorimeter Trigger at the High-Luminosity LHC

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The High-Luminosity LHC (HL-LHC) proposes an ambitious physics program covering high-precision Standard Model (SM) measurements and advancing the searches for new physics. The efficient data gathering and precise events reconstruction in the intense environment of 200 proton-proton interactions per bunch-crossing (40 MHz) are essential for attaining the success of the HL-LHC program. To fulfill these requirements, the CMS experiment is building an entirely new data acquisition (DAQ) and trigger systems. The Phase-2 CMS Level-1 trigger system will drive the massive detector input data bandwidth of 75 Tbps and is aimed to complete the single event processing within 12.5 μs. For this purpose, CMS plans to replace the Phase-1 μTCA-based processor cards and crates with an ATCA specification. Each ATCA board is powered with Xilinx UltraScale+ family FPGA that supports over a hundred high-speed optical links at 25 Gbps, capable of handling the high bandwidth and processing requirements of the HL-LHC. Along with the upgrade in hardware, the Level-1 trigger system will use highly flexible, modular, and adequately sophisticated algorithms currently feasible solely in offline reconstruction, such as a particle-flow (PF) algorithm. The flexible and modular architecture will assist in addressing the HL-LHC physics requirements. This talk will discuss the system design, prototyping, and algorithms being developed for the Phase-2 Level-1 Calorimeter trigger system.

Minioral

No

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No

Are you a student?

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