Development of Radiation-tolerant Slow-Control Board based on Atom Switch-based FPGA

Kazuki Ueno, Nanae Taniguchi, Toshitsugu Sakamoto, and Makoto Miyamura

***Abstract*—The Atom Switch-based FPGA (AS-FPGA) is a promising candidate for high-radiation environments, such as those encountered in future particle physics experiments using accelerators. To assess its feasibility, we conducted neutron and gamma-ray irradiation tests. No Single Event Upsets (SEUs) were detected at least up to 10^{11} and 10^{12} n/cm^2 with and without applied voltage, respectively. The AS-FPGA withstood Displacement Damage Dose (DDD) levels at least up to 10^{14} n/cm^2 and exhibited no Total Ionizing Dose (TID) effects at least up to 5 and 10 kGy with and without applied voltage, respectively. These results confirm its suitability for high-radiation environments. To facilitate its practical application, we developed an evaluation board to investigate its functions and performance. A prototype slow-control board incorporating a commercial slow-control sensor was constructed. This prototype was used to implement basic logic for temperature data acquisition and tested under neutron irradiation. The slow-control board operated successfully in a high-radiation environment up to 10^{11} n/cm^2, demonstrating the potential of the AS-FPGA and the slow-control board for future particle physics experiments.**

***Index Terms*—Atom switch, FPGA, radiation tolerance, slow control**

I. Introduction

In particle physics experiments using accelerators, Field-Programmable Gate Arrays (FPGAs) are widely used for detector readout, trigger, and slow-control electronics. The trend in improvements to accelerators for future particle physics experiments is to increase intensity, luminosity, and energy. Along with this, detectors and related electronics, including FPGAs, must be tolerant to higher radiation environments. For example, the radiation levels of neutrons and gamma rays for the COMET Phase-I experiment [1] at J-PARC, using the high-intensity proton beam, are expected to be 10^{12} n/cm^2 and 1 kGy for 150 days operation, respectively, including a safety factor of 5. Fig. 1 shows the radiation level of neutrons calculated with PHITS [2]. Even the detector area indicates a high radiation level. For the future experiment, COMET Phase-II, with a higher intensity beam, radiation levels 10 times higher or more are expected. Similarly, for the Belle II experiment [3], using a high-luminosity electron-positron beam, similar radiation levels are expected, and in the future, the higher luminosity beam is expected to further increase the radiation levels by a factor of 5-10.

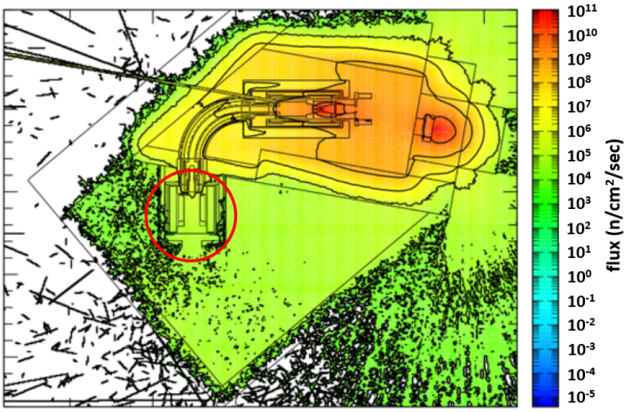

Fig. 1. Radiation level of neutrons for COMET Phase-I calculated with PHITS. Red circle shows the region for detector and front-end electronics.

Atom Switch-based FPGA (AS-FPGA) is expected to be used in such environments. The AS is a resistive-change switch that utilizes programmable conductive bridges. It consists of a polymer solid-electrolyte (PSE) sandwiched between inert Ru and active Cu electrodes. Low and high resistance states, corresponding to On and OFF states, are caused by the formation and annihilation of Cu ion bridges, respectively. Recently, AS has been successfully applied in nonvolatile FPGAs for their routing switches and look-up tables [4], [5].

Previous studies have reported the radiation tolerance of ASs, and these results imply that the AS structure is intrinsically tolerant to total ionizing dose (TID) effects, displacement damage dose (DDD), and single event upsets (SEU) [6], [7]. The newly developed AS-FPGA was irradiated with heavy ions and pulsed lasers, confirming its tolerance to SEUs [8]. For accelerator experiments, further studies in higher radiation environments are necessary. Therefore, we conducted neutron and gamma-ray irradiation tests on the AS-FPGA, evaluating SEU, DDD, and TID.

In order to use the AS-FPGA for particle physics experiments, it is important that the AS-FPGA exhibits good performance, such as high-speed signal handling, low latency, and low power consumption. Additionally, ease of programming logic is crucial. However, since the AS-FPGA is still in the early stages of development, programming tools are just beginning to be developed, and support for handling high-speed signals, such as gigabit transceivers, has not yet been provided. Feedback and improvements are therefore

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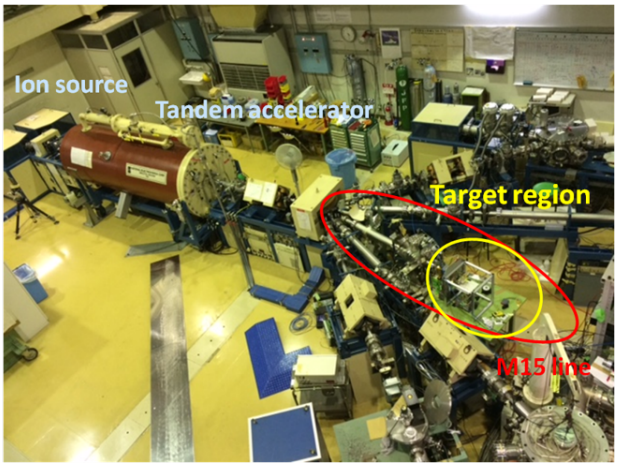

Fig. 2. Photograph of the tandem electrostatic accelerator at Kobe University. A neutron beam can be used at M15 beam line (red circle). The yellow circle shows the target region.

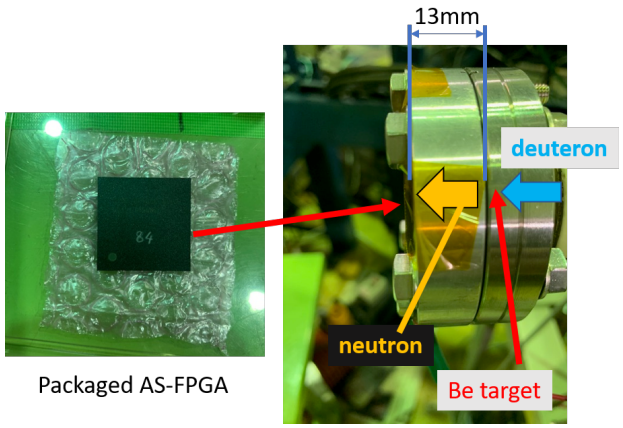

Fig. 3. Photograph of the packaged AS-FPGA and the experimental setup for neutron irradiation test.

indispensable. Thus, we have developed an evaluation board and assessed the AS-FPGA's functions and performance. As a first step, the construction of the prototype system for slow-control devices using the board and environmental sensors has been completed.

II. Irradiation Tests for AS-FPGA

A. Neutron irradiation tests

The neutron irradiation tests for AS-FPGA were performed using the tandem electrostatic accelerator at Kobe University and the Kyoto University Research Reactor (KUR). The accelerator at Kobe University generates a neutron beam with an energy peak of 2 MeV from the ^{9}Be (d,n) ^{10}B reaction. The neutron flux is 4.9×10^{6} n/cm^2/s per 1 μA for the deuteron beam at 10 cm from the Be target on the beam axis in the target region shown in Fig. 2. KUR generates many neutrons with a flux higher than 1×10^{11} n/cm^2/s.

For the evaluation of SEU, two types of tests were conducted at Kobe University in January and June 2019. In the first trial, the packaged AS-FPGA, without applied voltage, was irradiated as shown in Fig. 3. A fixed ON/OFF bit pattern

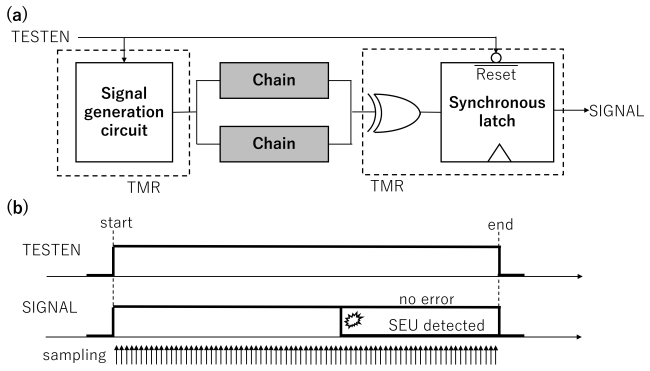

Fig. 4. (a) Schematic view of the evaluation circuit for SEU on the AS-FPGA, and (b) the timing structure of SEU detection.

was set on the AS-FPGA before irradiation, and the difference after irradiation was checked. The electric current of the deuteron beam was measured with a probe connected to the Be target, and the values were recorded with the data logger (GRAPHTEC GL840) during the beam time to evaluate the neutron flux. The AS-FPGA was placed at the beam center, 13 mm from the Be target, and irradiated with neutrons up to 1.2×10^{12} n/cm^2. It was confirmed that there were no differences in the bit pattern before and after irradiation.

In the second trial, the AS-FPGA implemented on the test board with applied voltage was irradiated, and real-time SEU detection was performed. The evaluation logic circuit to detect SEU was implemented on the AS-FPGA. Fig. 4 shows the schematic view of the evaluation circuit on the AS-FPGA and the timing structure of SEU detection. When the TESTEN signal is high, it generates a signal that cycles low/high and is input to the two chain circuits. The difference between the outputs of the two chain circuits is detected in the detection circuit every clock cycle (50 ns cycle). If a difference occurs, the SIGNAL, which is high by default, is dropped to low in the detection circuit. The occurrence of SEU in the chain circuit is detected by periodically sampling the SIGNAL on the PC connected to the test board, and the detection time is recorded on the PC. For safety, triple module redundancy (TMR) was applied to the signal generation circuit and the SEU detection circuit. For comparison, four types of devices under test (DUTs) were prepared: static random access memory (SRAM), a part of the AS region (AS1), another part of the AS region (AS2), and D Flip-Flop (DFF) and the AS region (DFF+AS). The circuit scales for SRAM, AS1, AS2, and DFF+AS were 2 kbit, 96 configurable logic blocks (CLBs), 368 CLBs, and 468 CLBs, respectively. The test board was placed at the beam center, 35 mm from the Be target. As in the first trial, the beam current was measured with a data logger to evaluate the neutron flux. Table I shows the results for SEU counts of the four chains after irradiation. The irradiated neutron fluences for SRAM, AS1, AS2, and DFF+AS were 1.6×10^{11} n/cm^2, 3.6×10^{11} n/cm^2, 1.7×10^{11} n/cm^2, and 1.5×10^{11} n/cm^2, respectively. The SEU count was 5 for SRAM and 0 for the others. There were possibilities that SEUs were detected in the SRAM and DFF+AS chains because the AS-FPGA itself was manufactured using the usual CMOS process

TABLE I
CIRCUIT CHAINS FOR SEU EVALUATION AND RESULTS

DUT type	Scale	Neutron fluence (n/cm^2)	SEU counts
SRAM	2 kbit	1.6×10^{11}	5
AS1	96 CLB	3.6×10^{11}	0
AS2	368 CLB	1.7×10^{11}	0
DFF+AS	468 CLB	1.5×10^{11}	0

and was not tolerant to radiation. The results confirmed that the AS-FPGA was tolerant to SEU at least up to 10^{11} n/cm^2 with 2 MeV neutrons.

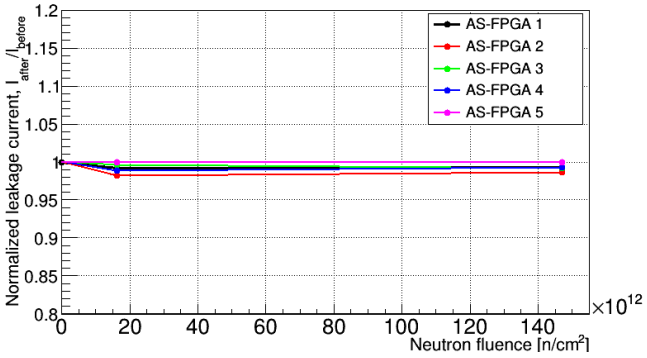

Fig. 5. The leakage currents for 5 AS-FPGA chips before and after neutron irradiation.

For the evaluation of DDD, the packaged AS-FPGA without applied voltage was irradiated at KUR in January 2021. If DDD occurs, it is expected that the leakage current will change. Thus, the leakage currents of the AS-FPGA before and after irradiation were measured. Five chips were irradiated up to 10^{14} n/cm^2 using the pneumatic system at KUR, which provided a neutron flux of 8.2×10^{11} n/cm^2/s with a rated thermal power of 1 MW. Fig. 5 shows the results of the leakage currents before and after irradiation. The leakage current is normalized by the leakage current before irradiation to account for individual chip differences. The results show no differences in the leakage current before and after irradiation up to 10^{14} n/cm^2. For higher fluence, more investigations are planned.

B. Gamma-ray irradiation tests

For the gamma-ray irradiation, we used two facilities: the Cobalt-60 Gamma-ray Irradiation Facility at the National Institute for Quantum and Radiological Science and Technology (QST), and the Chiyoda Technol Cobalt Irradiation Facility at the Tokyo Institute of Technology (TITech). Both facilities provide 1.17 and 1.33 MeV gamma rays from ^{60}Co sources. Dose rates are controlled by changing the distance between the source and the target sample.

To evaluate TID on the AS-FPGA, two types of tests were performed. The AS-FPGA wafer without applied voltage and the packaged AS-FPGA implemented on the test board with applied voltage were irradiated and evaluated. Leakage currents are expected to change when affected by TID, as in

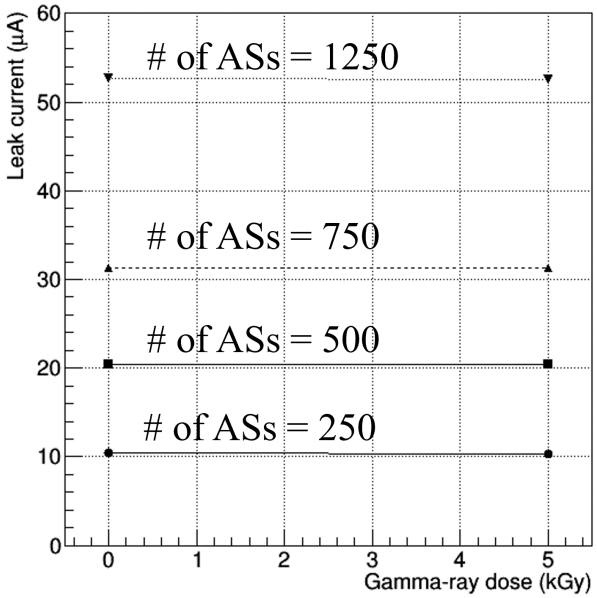

Fig. 6. The leakage currents for AS-FPGA chips before and after gamma-ray irradiation.

DDD, although the process is different. Therefore, the leakage currents of the AS-FPGA before and after irradiation were investigated.

At QST, the AS-FPGA wafer was irradiated with gamma rays at a dose rate of 500 Gy/h up to 5 kGy in February 2020. To avoid the effects of individual differences in leakage current, a wafer composed of 1250 AS-FPGAs, allowing irradiation of many chips at the same time, was used. The leakage currents of the AS-FPGAs before and after irradiation were measured. The leakage currents of 250, 500, 750, and 1250 AS-FPGA chips combined were measured, respectively. Fig. 6 shows the results of the leakage currents before and after irradiation. No changes in the leakage currents were seen. It was confirmed that no differences were observed under these conditions up to 5 kGy.

The packaged AS-FPGA implemented on the test board with applied voltage was irradiated with gamma rays at TITech in May 2021. The leakage current was measured using a standard shunt resistor and an operational amplifier on the test board, and the measured value was recorded by the data logger (AKIZUKI AE-LOGGER). The test board was placed 17.3 cm from the ^{60}Co source, corresponding to a dose rate of 500 Gy/h. To avoid radiation damage to parts other than the AS-FPGA on the test board, the board was shielded by lead blocks except for the AS-FPGA region, as shown in Fig. 7. The measurement of the leakage current of the AS-FPGA with gamma-ray irradiation was conducted up to 10 kGy. For comparison, the leakage current of another commercial Low-Power FPGA (LP-FPGA) was also measured up to 10 kGy. Fig. 8 shows the result. No change was seen in the leakage current for the AS-FPGA up to 6 kGy, while the leakage current increased linearly for the LP-FPGA immediately after irradiation. However, a slight current increase was observed

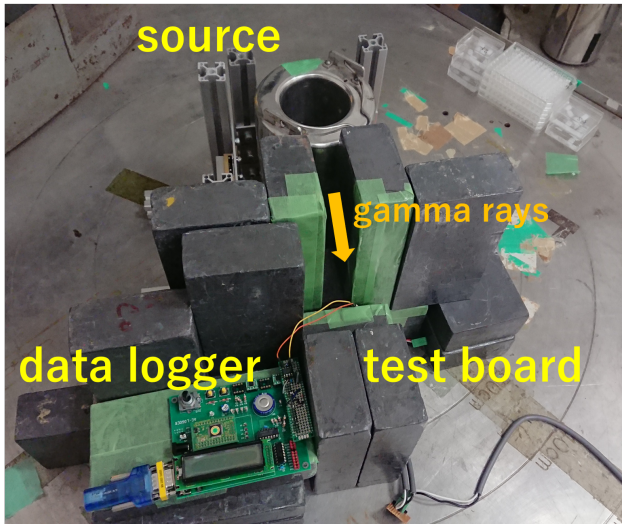

Fig. 7. Photograph of the experimental setup of gamma-ray irradiation for AS-FPGA at TITech.

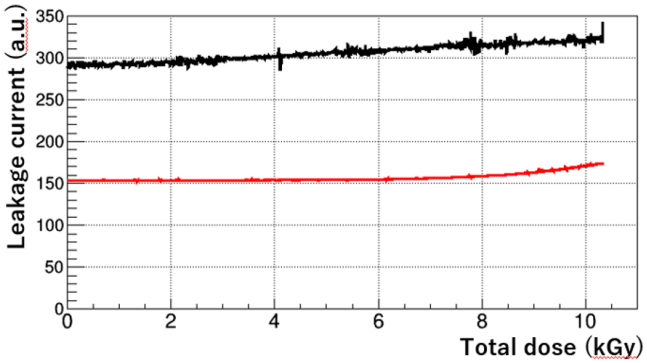

Fig. 8. Leakage currents during gamma-ray irradiation for the AS-FPGA (red) and the LP-FPGA (black).

for irradiations above 6 kGy in the AS-FPGA. This increase seemed to be due to degradation by TID in the CMOS. We confirmed that the AS-FPGA works even after the current change, i.e., after 10 kGy irradiation. More detailed investigations and improvements are planned.

III. Slow-control board

The above results indicate that the AS-FPGA has sufficient potential for future accelerator particle physics experiments, although some improvements and further investigations are required. The performance and usability of the AS-FPGA for particle physics experiments must also be investigated and improved. Consequently, our initial objective is to develop a relatively simple slow-control board that can operate effectively in high-radiation environments. To achieve this, we have developed a general-purpose evaluation board designed to assess the functions and performance of the AS-FPGA, allowing for iterative feedback and improvements.

The prototype of the evaluation board for the AS-FPGA has been developed as shown in Fig. 9. The board consists of an IC socket (Yamaichi Electronics IC201-1004-008), an

Fig. 9. Photograph of the evaluation board for the AS-FPGA.

oscillator (EPSON SG3225CAN 25.0000M), regulators (Analog Devices ADP2303, LTC3526, LTC3561, and LTC3542), current monitor circuits, 4 LEDs (Lite-On TST-C191KGKT), 2 switches (TE Connectivity FSM2JH), and 24 I/O pins. The IC socket mounts the packaged AS-FPGA chip, which can be easily replaced. The oscillator provides a 25 MHz clock used as the system clock for the AS-FPGA. The board is powered by a 5 V supply via the power connector. The regulators provide 3.3 V, 3.0 V, 2.5 V, and 1.2 V for the chips on the board and the additional sensors/chips via I/O pins, which are produced from the main 5 V power supply. To measure the leakage current, the current monitor circuits based on the shunt resistor and the operational amplifier (Analog Devices AD8210) are implemented on the board. For general purposes, LEDs, switches, and I/O pins are provided, similar to a standard FPGA evaluation board, allowing us to evaluate the functions and performance of the AS-FPGA easily. For some I/O pins, a standard pin assignment was adopted, allowing commercial slow-control sensors like thermometers, pressure sensors, and others to be connected directly.

As a first step in the evaluation board study, we aimed to confirm that the board can be used as a slow-control board in a high-radiation environment. For the slow control sensor, we adopted a combined temperature, humidity, and pressure sensor (BOSCH BME280), which has already been tested in a high radiation environment up to 10^{12} n/cm^2 for neutrons and up to 1 kGy for gamma rays. A sensor module using this sensor (AKIZUKI AE-BME280), which has the standard pin assignment, was connected to the I/O pin on the evaluation board. Simple logic that reads temperature data every second through SPI communication is implemented in the AS-FPGA.

In December 2023, we conducted a neutron irradiation test

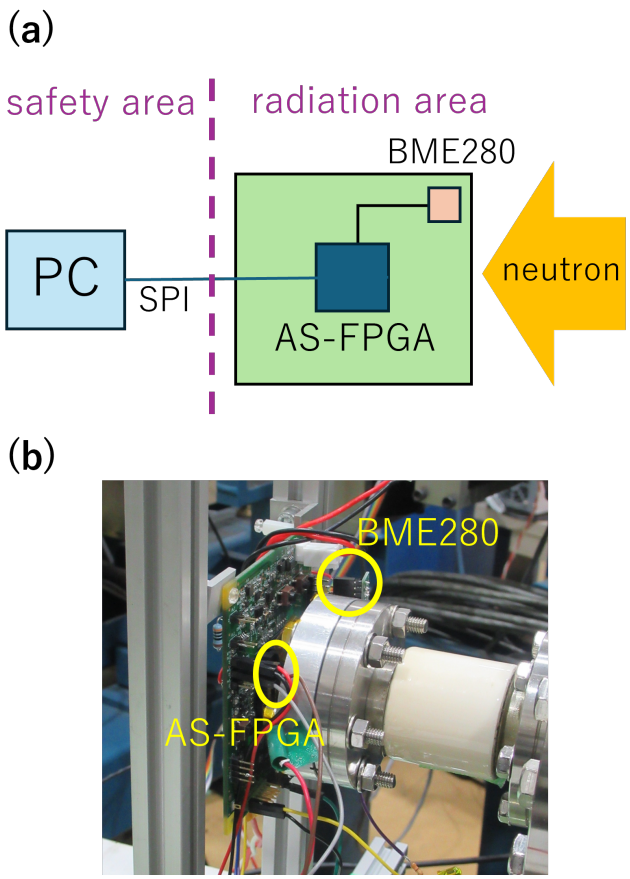

Fig. 10. (a) Schematic view of the experimental setup for the neutron irradiation test of the newly developed slow-control board. (b) Photograph of the experimental setup. The center of the slow-control board was set at the beam center, 20 mm from the Be target.

using the slow-control board based on the evaluation board equipped with the BME280 sensor module at Kobe University. Fig. 10 illustrates the schematic view of the experimental setup. The evaluation board was positioned at the beam center, 20 mm from the Be target. Data from the BME280 sensor was read by the AS-FPGA and transmitted to a PC located in a safety area via SPI communication. The neutron flux was evaluated by measuring the beam current with the data logger. In this configuration, neutron irradiation was carried out up to 10^{11} n/cm^2 while continuously acquiring temperature data.

Fig. 11 shows the results of the temperature data obtained from the BME280 sensor and the neutron fluence. The data was collected without any issues during neutron irradiation. This confirms that the newly developed slow-control board has the potential to be used in high-radiation environments. Although this measurement was only performed up to 10^{11} n/cm^2 due to time limitations, it is expected that the system can be used for higher irradiation environments in future experiments.

IV. Conclusion

The Atom Switch-based FPGA (AS-FPGA) is a potential candidate for use in high radiation environments, such as future particle physics experiments using accelerators. To confirm the feasibility of utilizing the AS-FPGA for particle

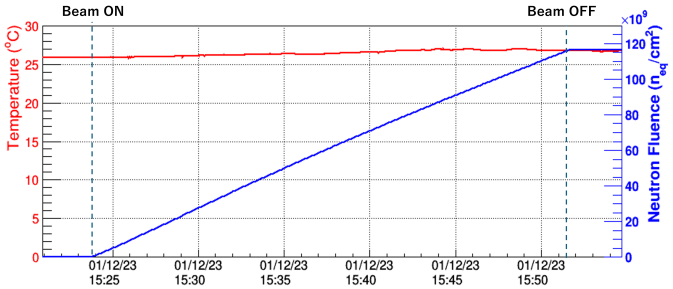

Fig. 11. Obtained temperature data from the newly developed slow-control board (red) and neutron fluence (blue).

physics experiments, we performed neutron and gamma-ray irradiation tests for the AS-FPGA. No SEUs were observed at least up to 10^{11} and 10^{12} n/cm^2 with and without applied voltage, respectively. It tolerated DDDs at least up to 10^{14} n/cm^2 and showed no TIDs effects at least up to 5 and 10 kGy with and without applied voltage, respectively. These results confirm the suitability of the AS-FPGA for such environments. Further tolerance tests for SEUs, DDDs, and TIDs at higher radiation levels are planned.

To realistically apply the AS-FPGA in experiments, additional evaluations and improvements are necessary. We have developed an evaluation board to investigate the functions and performance of the AS-FPGA. As a first step, we constructed a prototype slow-control board using the evaluation board and a commercial slow-control sensor. Using the prototype board, we implemented simple logic to obtain temperature data and conducted an operational test under neutron irradiation. We successfully operated the slow-control board in a high-radiation environment at least up to 10^{11} n/cm^2. These results confirm that the AS-FPGA and the slow-control board have the potential to be used in future particle physics experiments.

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