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Cross-Chip Partial Reconfiguration for the Initialisation of Heterogeneous Systems

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Reconfigurability is one of the main advantages of FPGAs over ASICs. Partial reconfiguration exploits this ability even further by allowing to exchange the logic on predefined FPGA regions at runtime. This is especially relevant in heterogeneous SoCs, combining FPGA fabric with conventional processors on a single die. Tight integration and supporting frameworks, such as the FPGA subsystem in Linux, create appealing options, including dynamically loading custom hardware accelerators or real-time logic modules.

Due to the high flexibility and performance of heterogeneous SoCs from AMD Xilinx, they are commonly used in data acquisition systems of all kinds. Qubit control systems based on a single RFSoC are currently limited by the number of readout and manipulation channels and are thus mainly used for characterising a small number of qubits. To scale to hundreds or even thousands of qubits, connecting auxiliary FPGAs to control further channels is a promising option. While cross-chip buses like AXI Chip2Chip allow to easily connect the logic in the devices, partial reconfiguration on the peripheral FPGAs is not supported by the vendor. To overcome this restriction, this contribution proposes a system architecture that uses an AXI Chip2Chip connection in combination with an AXI ICAP controller and custom Linux drivers. This enables the operating system running on the SoC to directly access the configuration ports of the peripheral FPGAs. As a result, updates from the network can be installed at runtime and peripheral FPGA devices can be added and remove during operation.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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