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Optimization of the Upgraded Timing Distribution System of the LHCb experiment at CERN

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The Timing Distribution System of the LHCb Experiment at CERN employs FPGA firmware cores to ensure synchronicity across all Front-End and Back-End modules of the Detector Readout System. The control signals are centrally generated in an FPGA-based card, the Readout Supervisor (SODIN), which receives the LHC synchronous clock, and packs timing and control signals into data words (TFC data), distributing it downstream with fixed and deterministic latency. The TFC system is divided into two levels of hierarchy. SODIN transmits the TFC data to FPGA-based Control Cards, which recovers the clock and control signals and forwards them to the Readout Cards and the Front-End modules.
While the clock is recovered at the Control and Readout Cards with a fixed phase within a window of 30ps, at the Front-End modules such window is measured to be 4ns, causing a time-alignment shift of up to 4ns after each clock loss. The reason is that the FPGA internal PLL used for generating the reference clock for the transceivers and the external PLL used for jitter-cleaning don't keep the same input-to-output phase after a loss of lock.
This paper focuses on the components responsible for timing distribution between the Control Cards and the Front-End modules, achieved through individual bidirectional control links implemented using the GBT-FPGA firmware core. Different firmware and clock routing alternatives were studied for such a link, reducing the window from 4ns to the order of tenths of picoseconds. This paper describes such implementations and the results obtained with each of them.

Minioral

Yes

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No

Are you a student?

No

Author: FEO, Mauricio (Technische Universitaet Dortmund (DE))

Co-authors: ALESSIO, Federico (CERN); HACHON, Frederic (Centre National de la Recherche Scientifique (FR)); VOUTERS, Guillaume (Centre National de la Recherche Scientifique (FR)); CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR)); DURANTE, Paolo (CERN)

Presenter: FEO, Mauricio (Technische Universitaet Dortmund (DE))

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