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Science Rate Acceleration with ESnet-JLab FPGA Accelerated Transport Load Balancer

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To increase the science rate for high data rates/volumes, Thomas Jefferson National Accelerator Facility (JLab) has partnered with Energy Sciences Network (ESnet) to define and implement an edge to compute cluster data event load balancing architecture with hardware accelerated elements to address compression, fragmentation, dynamically switched destination transport and reassembly at the event level. A core component is the ESnet-JLab FPGA Accelerated Transport (EJFAT) that functions as a network Forwarding-Plane (FP) in conjunction with an associated control-plane (CP) that handles compute node subscriptions and balances node workloads at the event level based on node feedback. This core load-balancer (LB) provides for three-tier horizontal scaling across (1) multiple FPs, (2) cluster nodes subscribed to an FP, and CPUs within a node. EJFAT effectively provides seamless integration of edge / cluster computing to support direct experimental data processing for immediate use by JLab science programs and others such as the Electron-Ion Collider (EIC) as well as data centers of the future requiring high throughput and low latency for both time-critical data acquisition systems and data center workflows. When completed, EJFAT will have an operational impact for integrated research infrastructure as called for in \cite{b0}, \cite{b1}, \cite{b2}, \cite{b3}, \cite{b4}, \cite{b5}, \cite{b7}, \cite{b8}, \cite{b9}, and \cite{b10}, and currently operates a new load balancing architecture. We report on future plans and experiences to date with cluster node load balancing and science rate acceleration both at JLab and also in conjunction with ESnet and Lawrence Berkeley National Laboratory (LBNL).

Minioral

Yes

IEEE Member

No

Are you a student?

No

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