Design of a fast readout CMOS pixel sensor for the first prototype of CEPC Vertex Detector

Xiaomin Wei, Ying Zhang*, Wei Wei*, Tianya Wu, Xiaoting Li, Liang Zhang, Raimon Casanova, Zhijun Liang, Shuqi Li, Wei Wang, Jia Zhou, Ziyue Yan, Yiming Hu, Xiaoxu Zhang, Xinhui Huang, Lei Zhang, Ming Qi, Hao Zeng, Xuewei Jia, Jun Hu, Jinyu Fu, Hongyu Zhang, Gang Li, Linghui Wu, Mingyi Dong, Jianing Dong, Jia Wang, Ran Zheng, Weiguo Lu, Sebastian Grinstein, João Guimarães da Costa

I. Introduction

The CEPC (Circular Electron Positron Collider) is a frontier high-energy research facility. It aims to produce a large amount of the Higgs bosons in a relatively clean environment and to measure the properties as precisely as possible, and then move to lower center-of-mass energies for collecting large samples of W, and Z bosons. CMOS Pixel Sensors (CPSs) are attractive for the design and construction of the CEPC vertex detector due to their low material budget, high spatial resolution, fast readout speed and low power consumption. Since 2015, several series of CPS chips are developed for studying the properties of sensing elements, the different readout architectures and different processes. This study presents the design of TaichuPix3. The object of the TaichuPix3 is to develop fully functional large-scale sensors for studying the design of a ladder and a vertex detector prototype.

According to the CEPC conceptual design report, the pixel sensors for the vertex detector require a high spatial resolution of 2.8 μm, low mass of 0.15% X0/layer and high hit rates of 3.5M, 11M, 10M hits/cm^2·s with spacing times of 680 ns, 210ns, 25 ns at energy 240 GeV, 160 GeV and 91 GeV, respectively [1]. In addition, low power and moderate radiation hardness should be considered. Based on the previous study in TaichuPix1 and TaichuPix2, we expected that TaichuPix3 achieves a spatial resolution below 5 μm and fulfill the readout speed requirements in the prototype vertex detector with reasonable radiation hardness and power consumption. This study will present the circuit designs and the test results of TaichuPix3.

II. Circuit Design

For the construction of a ladder or prototype of vertex detector, the pixel array is 512×1024 in TaichuPix3. The pixel pitch is 25 μm. The maximal hit density is 120M pixels/s·chip calculating from the production of W bosons. Each pixel information is recorded with 32 bits, which includes 1bit of valid flag, 8 bits of timestamp, 19 bits of address, and the rest 4 bits for data compression encoding. The parallel data are out put with a clock with 140 MHz. As a results, the serial output data rate is 4.48 Gbps in a triggerless mode. A trigger mode is also designed for reducing the data rate. The trigger latency is supposed as 3~6 μs and the average trigger rate is supposed as 50 kHz. In trigger mode, the typical output data rate is 160 Mbps. In order to achieve a detection efficiency of 99%, the dead time for a double column should less than 500 ns. Considering the bunch spacing time of 25ns at 91 GeV, the signal should be readout fast and the time walk should be optimized.

The block diagram of TaichuPix3 is shown in Fig. 1. The pixels are organized as double columns (Dcols). In order to achieve the dead time less than 500 ns, all the double columns are readout parallel. A timestamp is recorded at the end of the double column due to the limit pixel pitch. As a result, the data is matched in a time window with trigger signal. The matched data are buffered for output in case of trigger mode. In the triggerless mode, all the data are buffered and output. The peripheral readout includes two level FIFOs. The first level FIFOs (FIFO1) are used to buffer the high-speed parallel data from pixel array according and to store the data waiting to be distinguished in trigger mode. The second level FIFOs (FIFO2) are used to match the readout speed of chip interface. Considering the ease of use and the chip tests, the TaichuPix3 includes slow controller based on SPI (Serial Peripheral Interface), DACs (Digital to Analog Converters) providing the required bias voltages, PLL (Phase-Locked Loop) and Serializer.

The circuit design is based on a 0.18 μm CIS process with deep P well. The sensing element is a Nwell/Pepi diode. The analog front-end circuits read out and digitize the charges collected by the sensing element. we adopted the analog front-end circuit topology in the ALPIDE chip [2] and optimize the parameters for a fast readout. Fig. 2 presents the simulation results of the time walk under different power consumption. The time walk is well controlled in 100 ns.

In the column level readout in pixel array, we realized a data-driven readout schema, where only the addresses of the hit pixels are output. The readout cycle is 50 ns. In the peripheral logic, we designed a Dcol reader for reading and resting the pixels. Especially, a real-time data compression strategy is proposed and realized before sending data to the first level FIFOs. Fig. 3 presents the circuit blocks. With a system clock of 40 MHz, there is no additional timing expense for the data compression circuits. Enable the data compression function, the data volume can be reduced and the readout speed is increased.

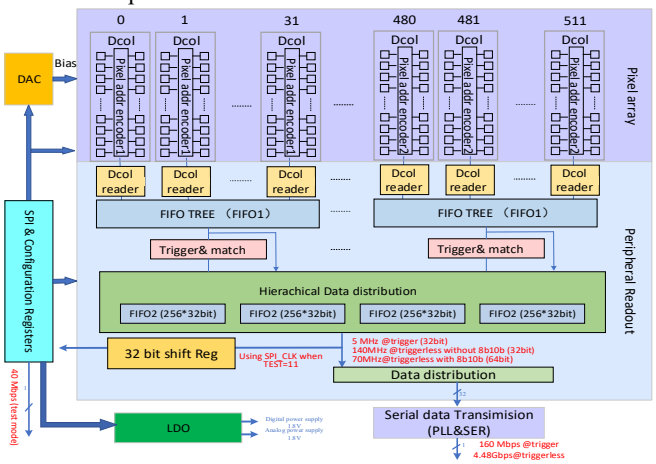

Fig. 1. Block Diagram of TaichuPix3

The fast chip level readout is closely related with the accesses of FIFO1s and FIFO2s. For FIFO1s, we propose a sharable

architecture as shown in Fig. 4. The shared FIFO owns flexible volumes to occur the random hit burst. Thus, higher hit flux can be accepted even with a reduction of total memory volume. For FIFO2s, the arbiter circuits in TaichuPix1 is kept, because there is no empty readout cycle if any FIFO2s are not empty.

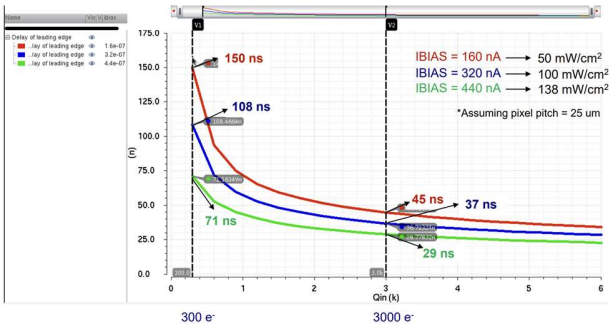

Fig. 2. Simulation of the Delay of leading edge vs. input charge

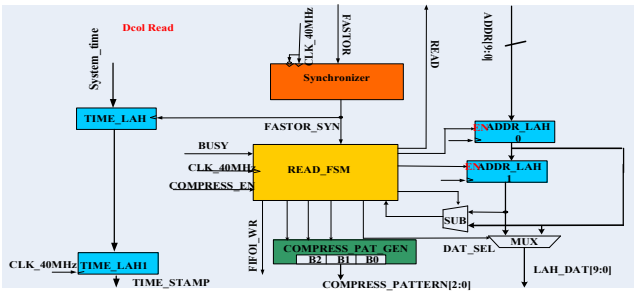

Fig. 3. Block diagram of Dcol reader for a double column.

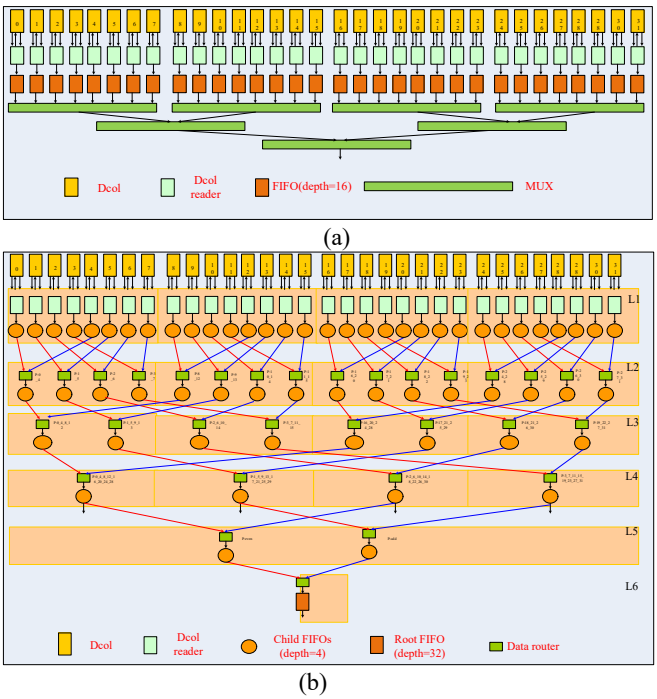

Fig. 4. Architecture of the general FIFO architecture(a) and shared FIFO architecture in this study (b)

III. Experiment Results

Fig. 5 presents some results to evaluate the data compression strategy and shared FIFO architecture in this study. Both of the results indicates that our proposal promotes the design for accepting high hit flux. The size of TaichuPix3 chips is 15.9 mm × 25.7 mm. We characterized the chips with test pulses, X-ray, laser source, ^{90}Sr source and electron beam [4][5]. The time walks are evaluated about 60 ns to 90 ns with different power consumptions seen from the statistics of digital output. In the first 6-layer CEPC vertex detector prototype, 24 chips were installed as in Fig.6. Fig.7 presents some results from beam tests. The spatial resolution is below 5μm and the detection efficiency is about 99%.

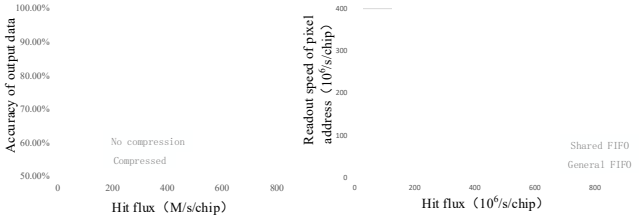

Fig. 5. Simulation evaluation of data compression (a) and the proposed FIFO architecture (b). The data compression simulation was done with an average cluster size of 3.

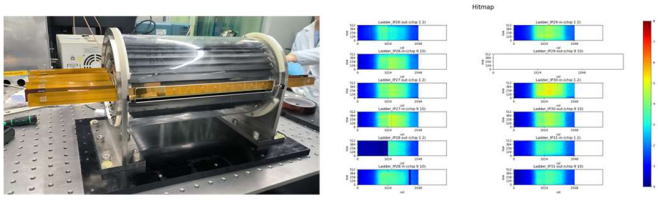

Fig. 6. Prototype with 6 ladders and 4 chips/ladder (a) and the hit maps on Prototype

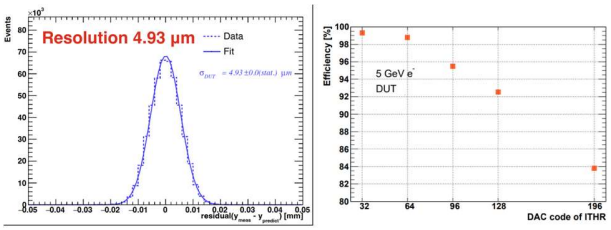

Fig. 7. Resolution (a) and detection efficiency of one chip (b) in the prototype.

References

[1] CEPC Conceptual Design Report: Volume 2 -Physics & Detector (2018)
[2] G. Rinella, The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System, NIMA 845(2017):583-587.
[3] X. Wei, et al., High data-rate readout logic design of a 512 × 1024 pixel 311array dedicated for CEPC vertex detector, JINST 14 (12) (2019).
[4] Y. Zhang, et al., Development of a CMOS pixel sensor prototype for the high hit rate CEPC vertex detector, NIMA 1042 (2022)
[5] T. Wu, et al., Beam test of a 180nm CMOS Pixel Sensor for the CEPC vertex detector, NIMA (2023)

Acknowledgment

The research was supported and financed in large part by the National Key Research and Development Program of China under Grant No. 2018YFA0404302 296 from the Ministry of Science and Technology. The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). Additional support was provided by the Youth Scientist Fund from the National Natural Science Foundation of China under Grant No. 12205313,

China Postdoctoral Science Foundation under Grant No. 2021M693182 and State Key Laboratory of Particle Detection and Electronics under Grant No. SKLPDE-ZZ-202315.