Design of a fast readout CMOS pixel sensor for the first prototype of CEPC Vertex Detector

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on behalf of the CEPC MOST2 vertex detector design team

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- Chip Design
- Simulation and Tests
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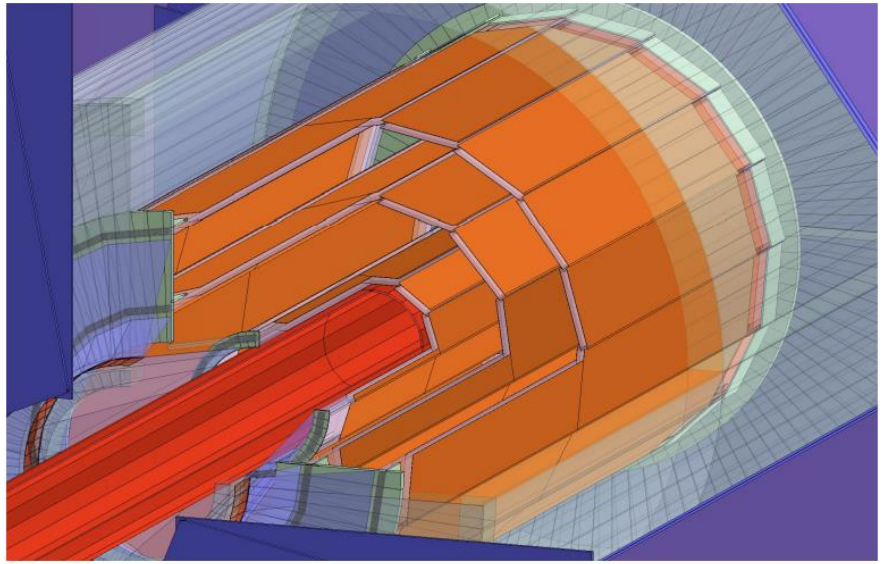
Requirements of CMOS Pixel Sensors for CEPC



Schematic View of CEPC Vertex detector

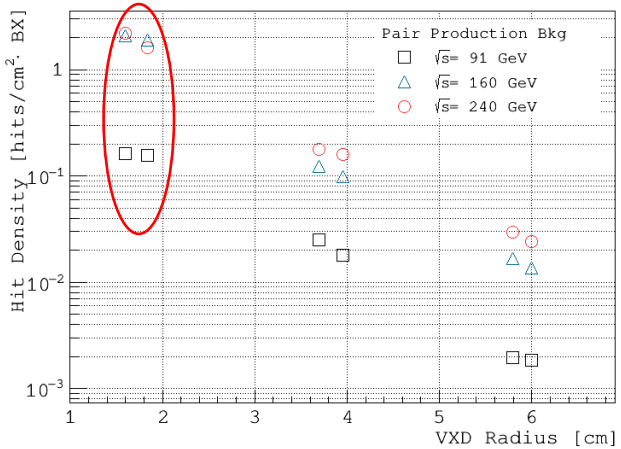
Main Requirements* :

- Spatial Resolution ： ~3 μm
- Fast readout: according to the bunch spacing of 25 ns @ 90GeV
- Maximal Hit rate：~ 36 MHz/ cm^2 @ 160 GeV
- Power consumption：50 mW/ cm^2
- Radiation hardness

Baseline design parameters of CEPC vertex detector*

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ(μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Hit density vs. VXD Radius *



Bunch Spacing & hit density *

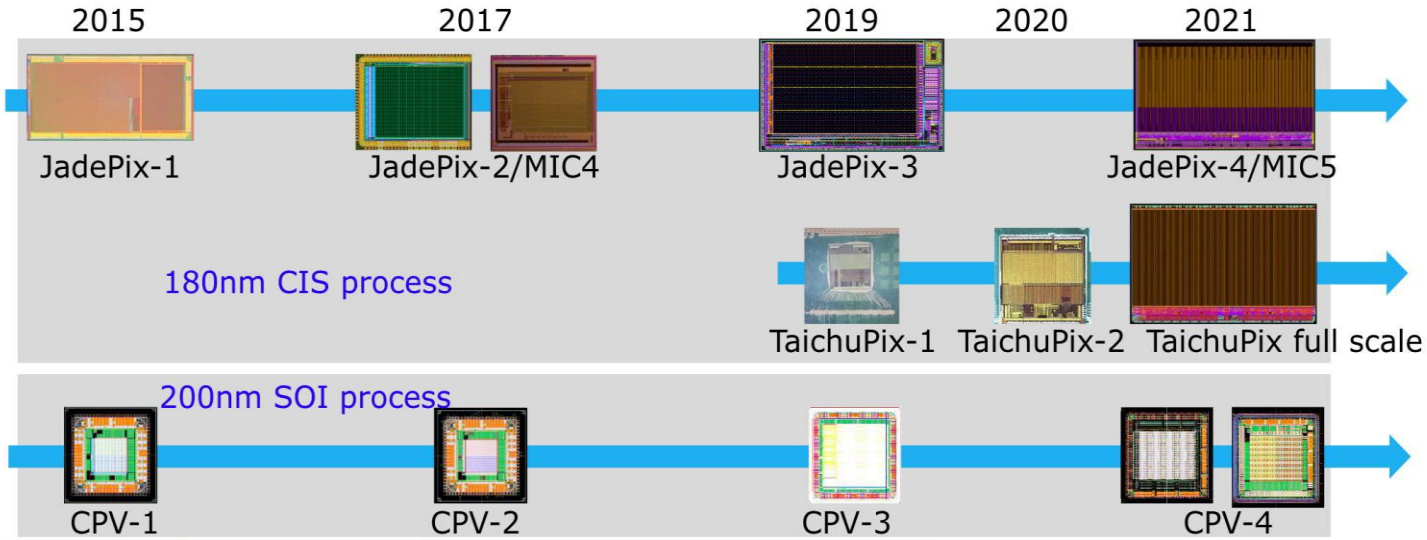
Parameter	Unit	Higgs	W	Z
Bunch spacing	ns	680	210	25
Hit density	hits/bunch/cm^2	2.4	2.3	0.25
Hit rate	MHz/cm^2	12	36	32
Data Rate	MHz/chip	36	108	96

** From "CEPC CDR, Volume II" , the requirements in CEPC TDR will be beyond that in the CDR. The trend is higher data rate and higher radiation tolerance.*

Current States of CPS for the CEPC

- since 2015, JadePix, CPV : Different sensor designs, kinds of readout architectures and SOI process => high radiation tolerance and high spatial resolution
- since 2019, TaichuPix: To realize fully functional sensors for the prototype

This report will focus on TaichuPix3, which is with a pixel array of 1024×512 and was used to structure the prototype of the vertex detector.



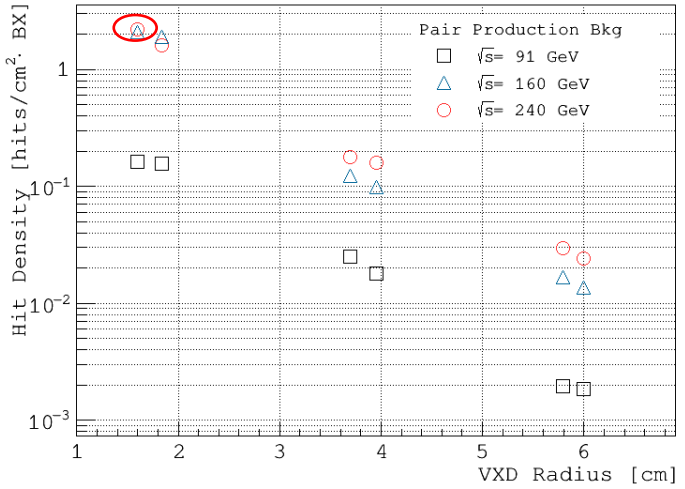
CPS chips for CEPC Vertex detector*

* From "Xingye Zhai, Yunpeng Lu, et al. Performace study of Conference on Nuclear Electronics and Nuclear Detection Technology

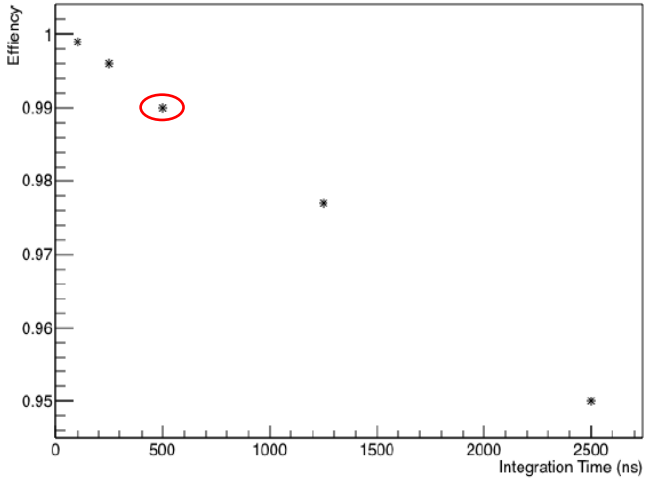
Specifications of TaichuPix3

Full size and fully functional sensors

- Pixel array：1024×512
- Pixel pitch：25 μm
- Data rate*：3.84 Gbps（120 Mpixels/s·chip ）
- Support trigger and triggerless modes*
  - Triggerless mode：4.48 Gbps
  - Trigger mode：160 Mbps
- Pixel readout：
  - Cycle：50 ns （double column level: 500 ns）
  - Response time dispersion: ~100 ns
- Power consumption：200 mW/cm^2



Hit density vs. VXD Radius

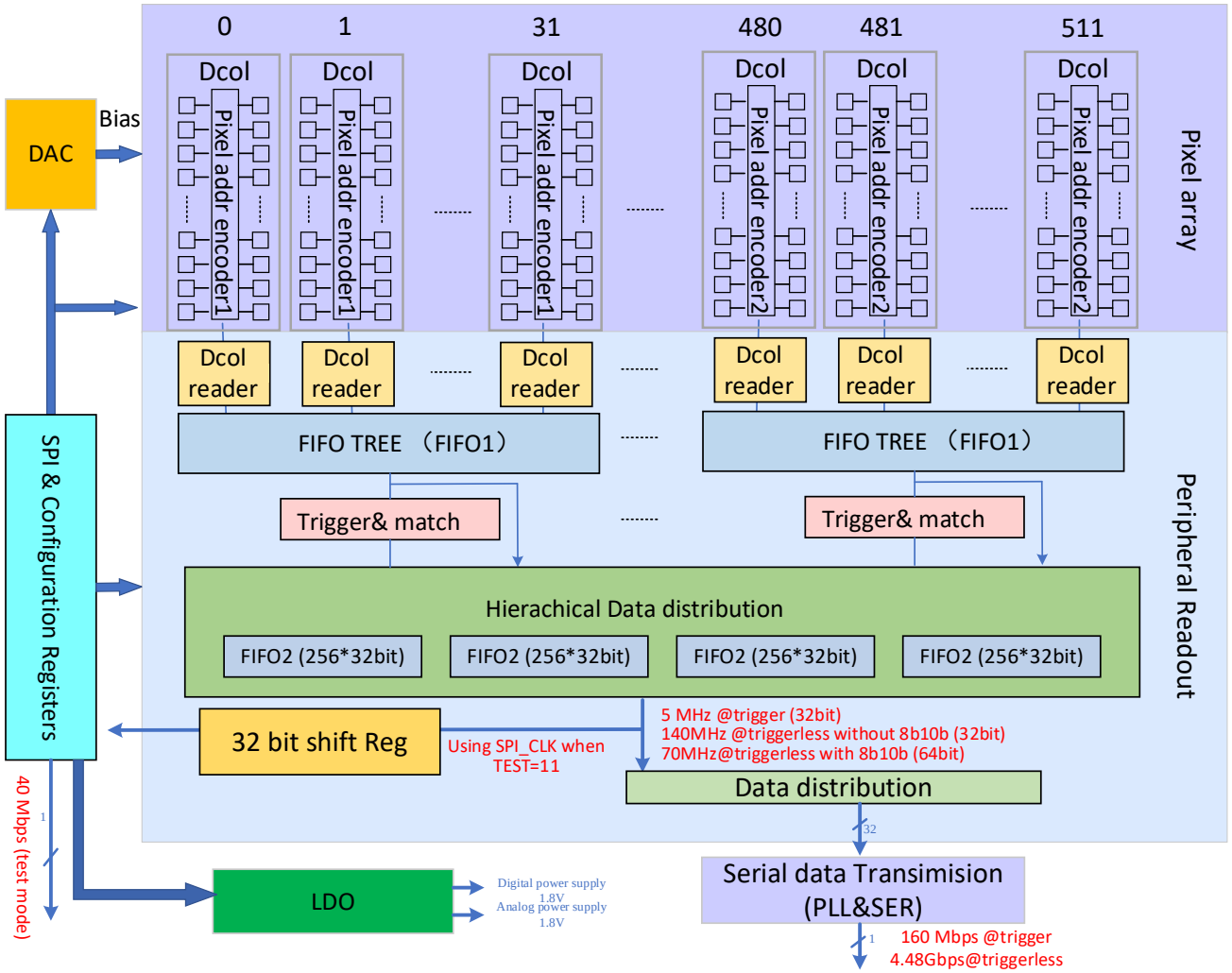


Simulation: Detection Efficiency vs. Deadtime

* Estimation condition:

1) The chip sensing active area is 3.2768 cm^2 (1024*512 pixel array, 25 μm pixel pitch),
2) The cluster size is 3 pixels.
   Each hit pixel is recoded with 32 bits (Timestamp: 8 bits, pixel address: 19 bits).
3) The trigger latency is supposed 3~6 μs, and the average trigger rate is 50 kHz.

Fast readout architecture of TaichuPix3



Block Diagram of TaichuPix3

- Pixel array：1024 x 512
  - 512 Double columns
  - Configurable and testable
- Peripheral Readout
  - Dcols are read out in parallel. The data are compressed during the readout, and then sent to the first level FIFOs (FIFO1).
  - Trigger signal is matched when data are read out from FIFO1.
  - FIFO2 is used to satisfy the chip interface speed.
- Three data readout modes
  - Trigger mode： 160 Mbps
  - Triggerless mode： 4.48 Gbps
  - Slow control mode：data output by SPI
- Fully functional integrated
  - DAC, PLL, Serdes
  - Debug and test mode
  - Scan Chain and memory BIST

Analog Front End Design

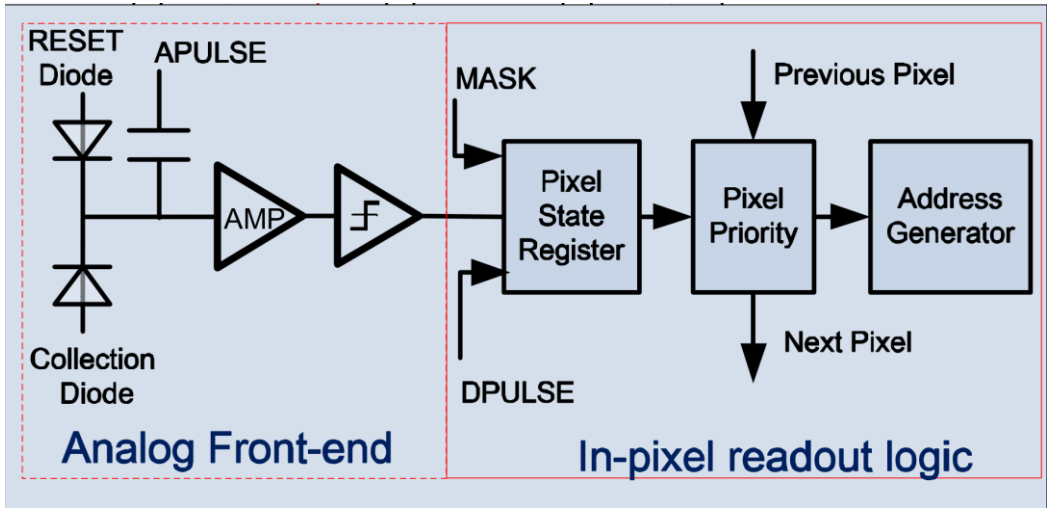
Optimize the response time

- ALPIDE topology

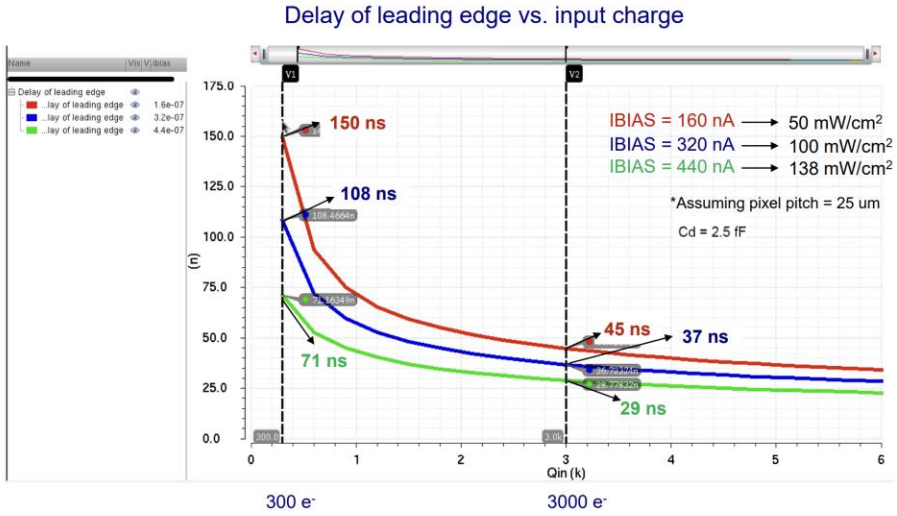
  time walk ~μs ⟶ ~100 ns

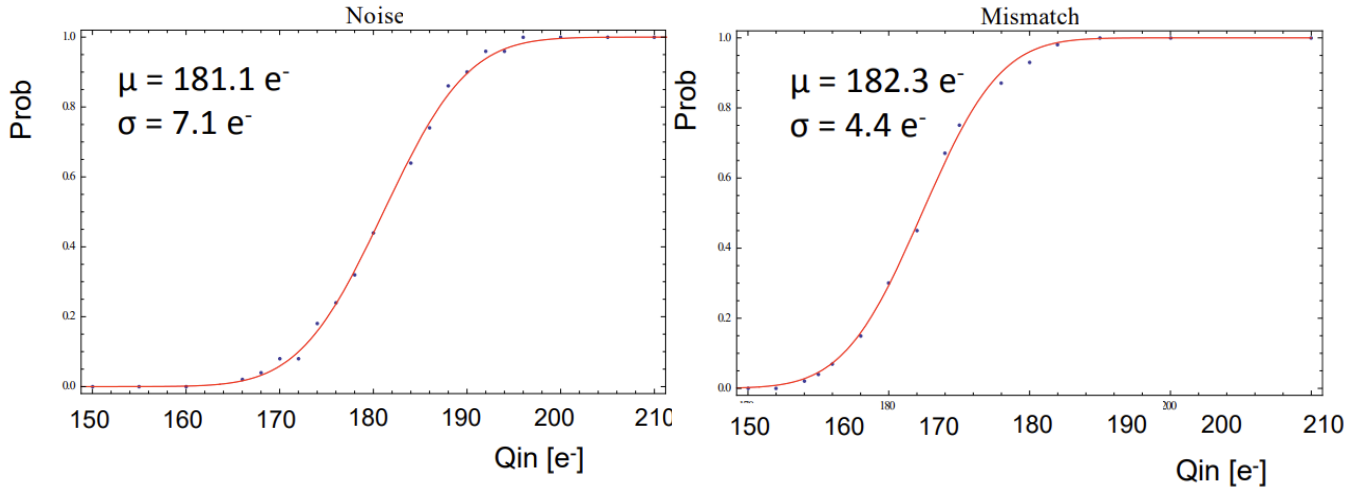
- Simulation results：

Threshold < 200 e- , ENC <10 e-



Block diagram of a pixel



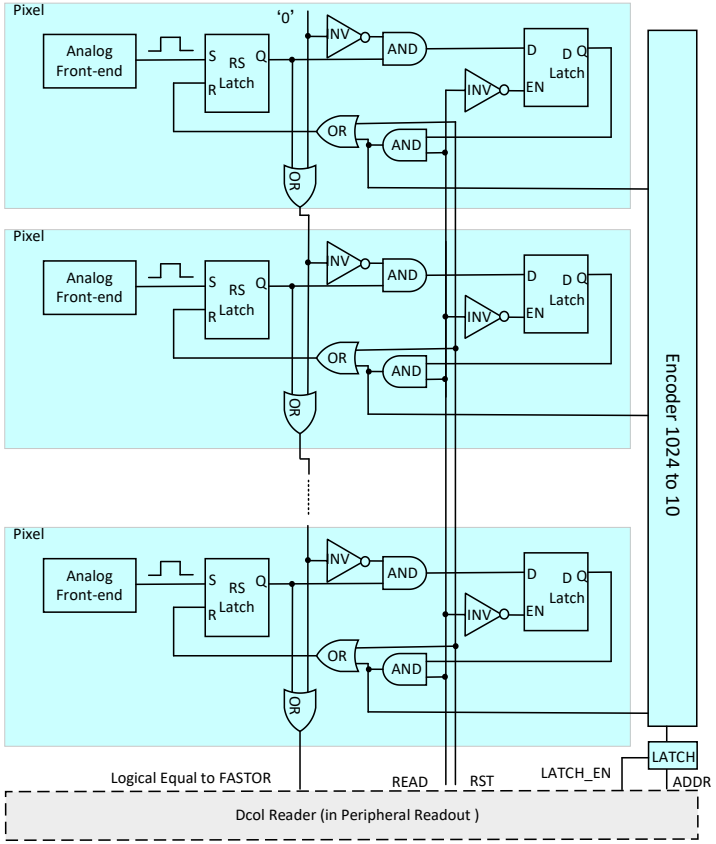


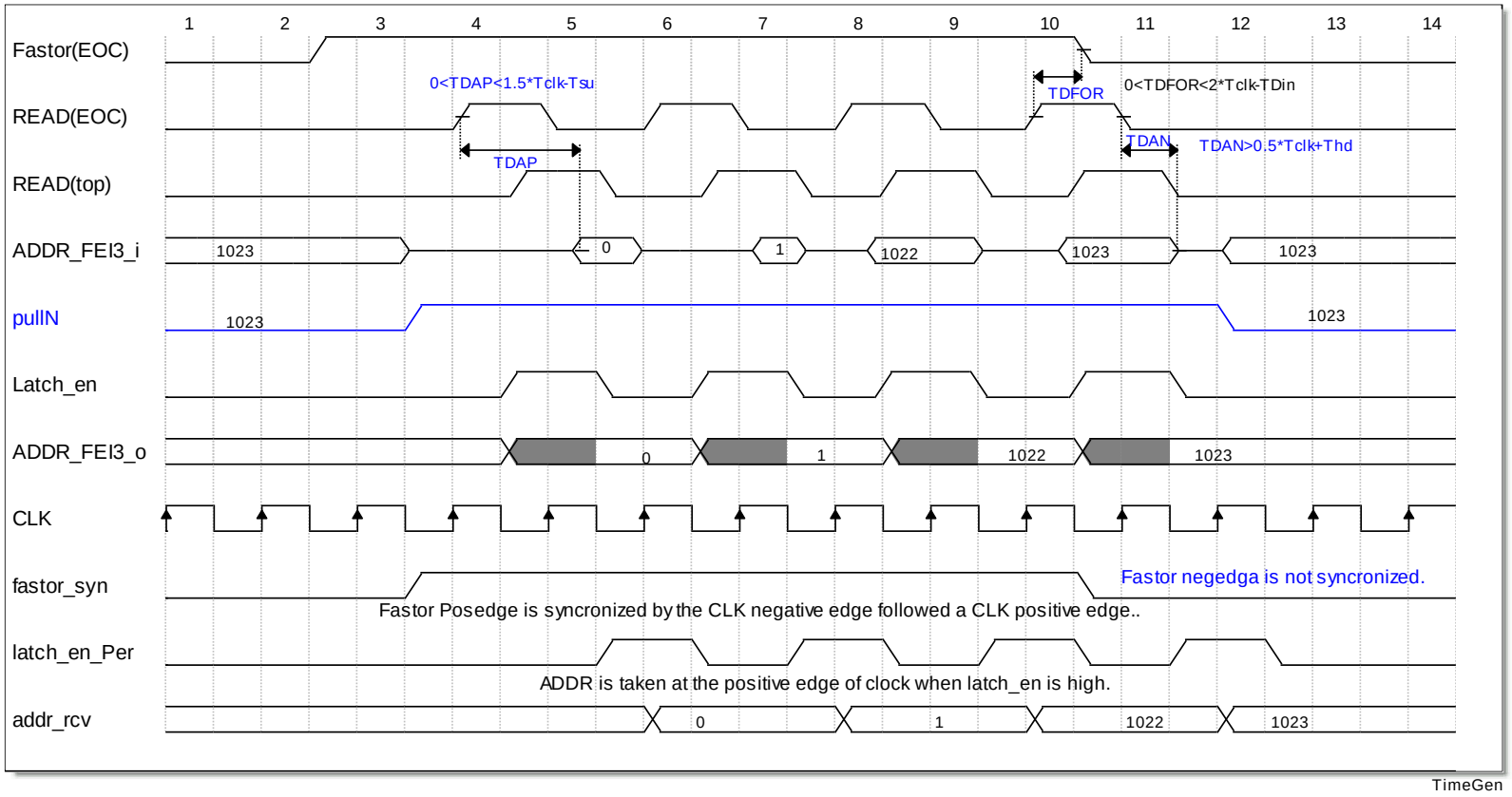
Simulation results

Digital readout logic in pixel

The main limitation is the small area.

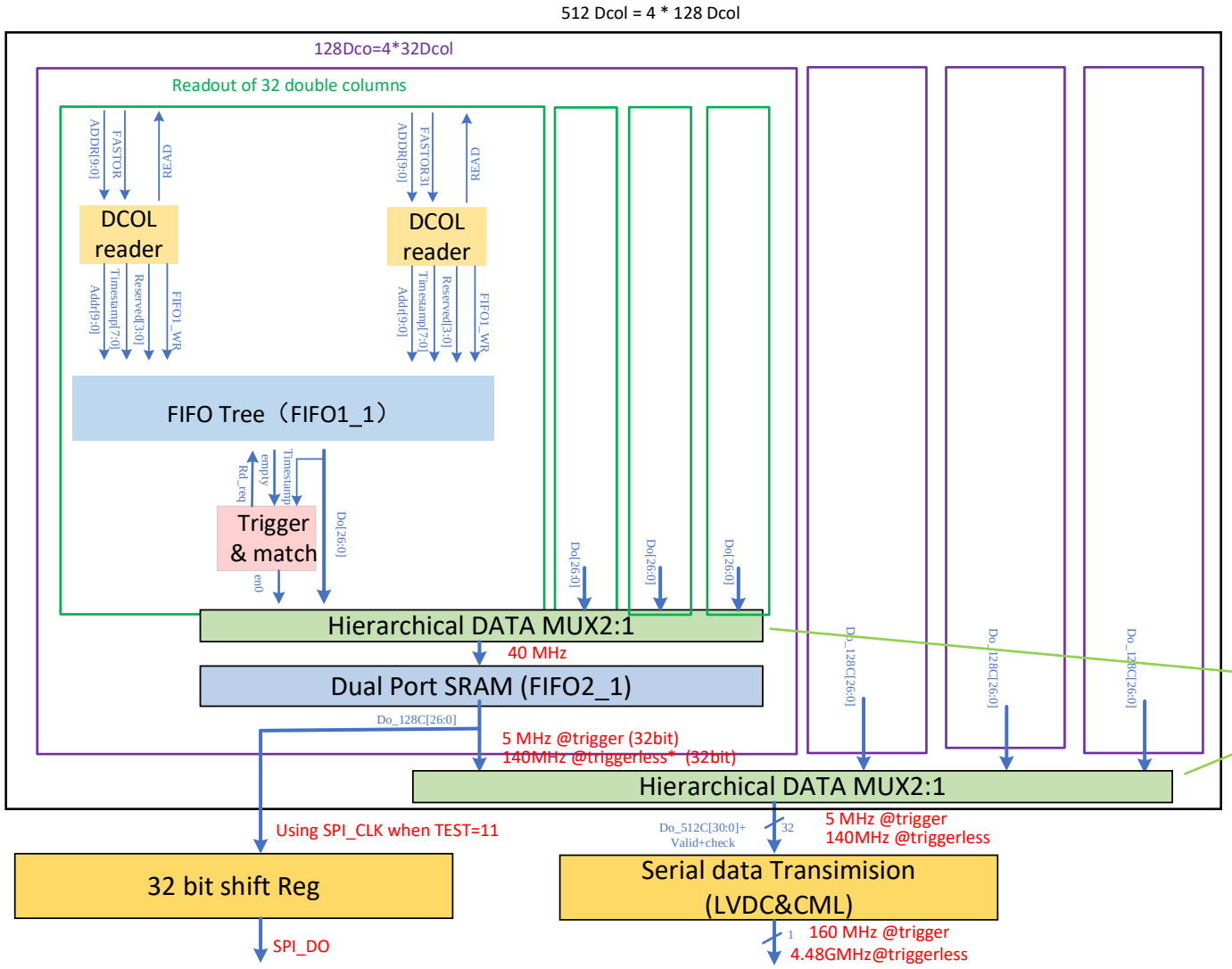
- In pixel columns, priority control and address encoder are realized combining with the configuration of pixel mask, bias and test signal. The readout cycle is 50 ns.
- The timestamps are recorded in the EOC, and thus a time window is necessary for data match.





Readout logic and Timing in a Dcol

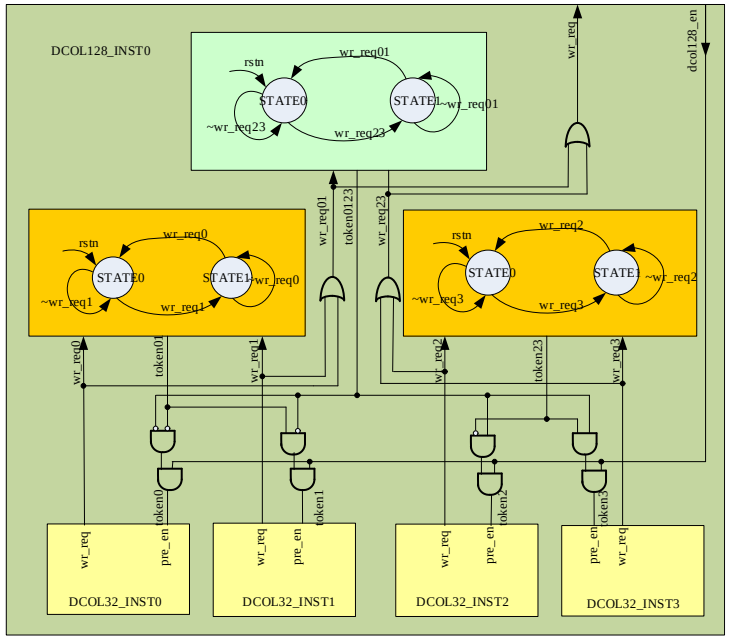
Peripheral readout in TaichuPix3



Block diagram of peripheral readout

High speed readout

- Dcol：real time data compression
- 32 Dcols： a sharing FIFO tree
- 128 Dcols and the top level：Hierarchical data multiplexers, not to waste any clock cycles



Hierarchical DATA MUX2:1

Real time data compression (in Dcol Reader)

Strategy：

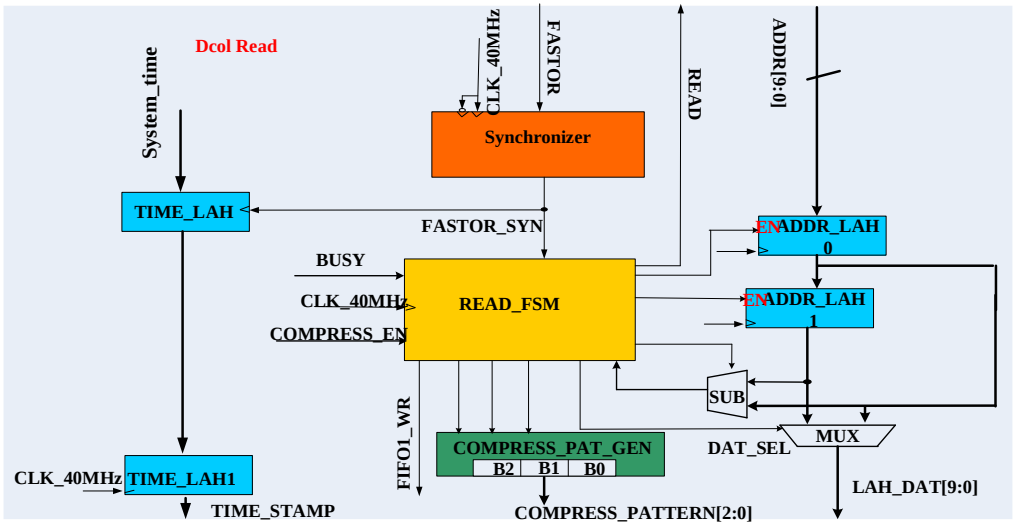
- The adjacent several addresses are compressed in one word.
- Only the first address is recorded and the rest pixel addresses in the compression range (5 adjacent addresses in TaichuPix3) are noted as ‘0/1’ in the following bits.

Area costs：

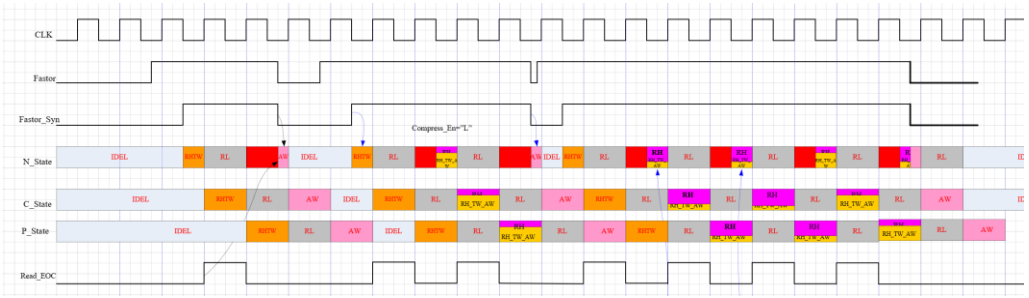
- Additional latch for storing the first address in a pattern
- A compression pattern should be added for each word
- The readout control is much complex.

Timing overhead：

- In Taichupix3, there is no additional timing overhead. Because two clock cycles are required for reading one address from pixel column. It is enough for reading and compressing the data.
- In other cases, the circuit should be carefully.



Block diagram of Dcol reader



Timing in Dcol reader

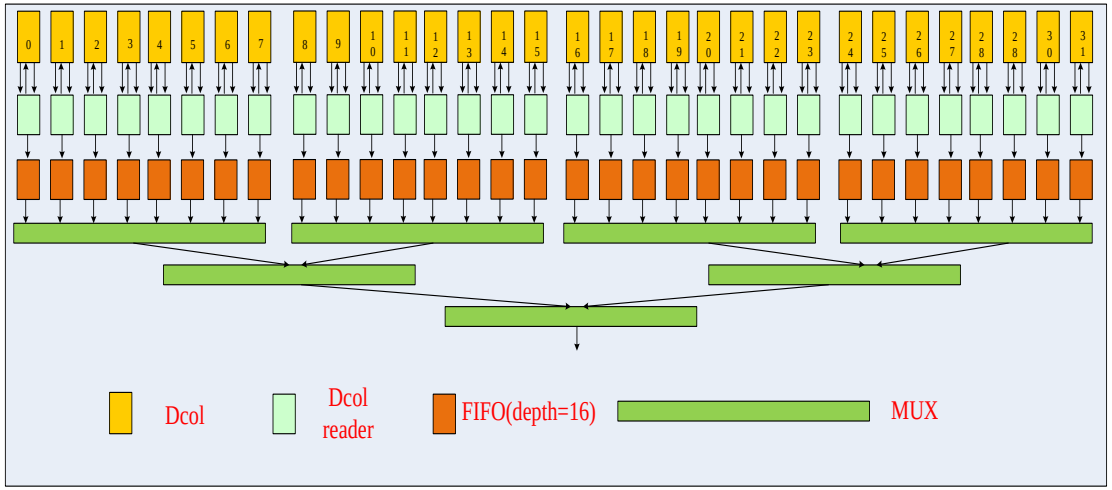
Shared FIFO tree (32 Dcols)

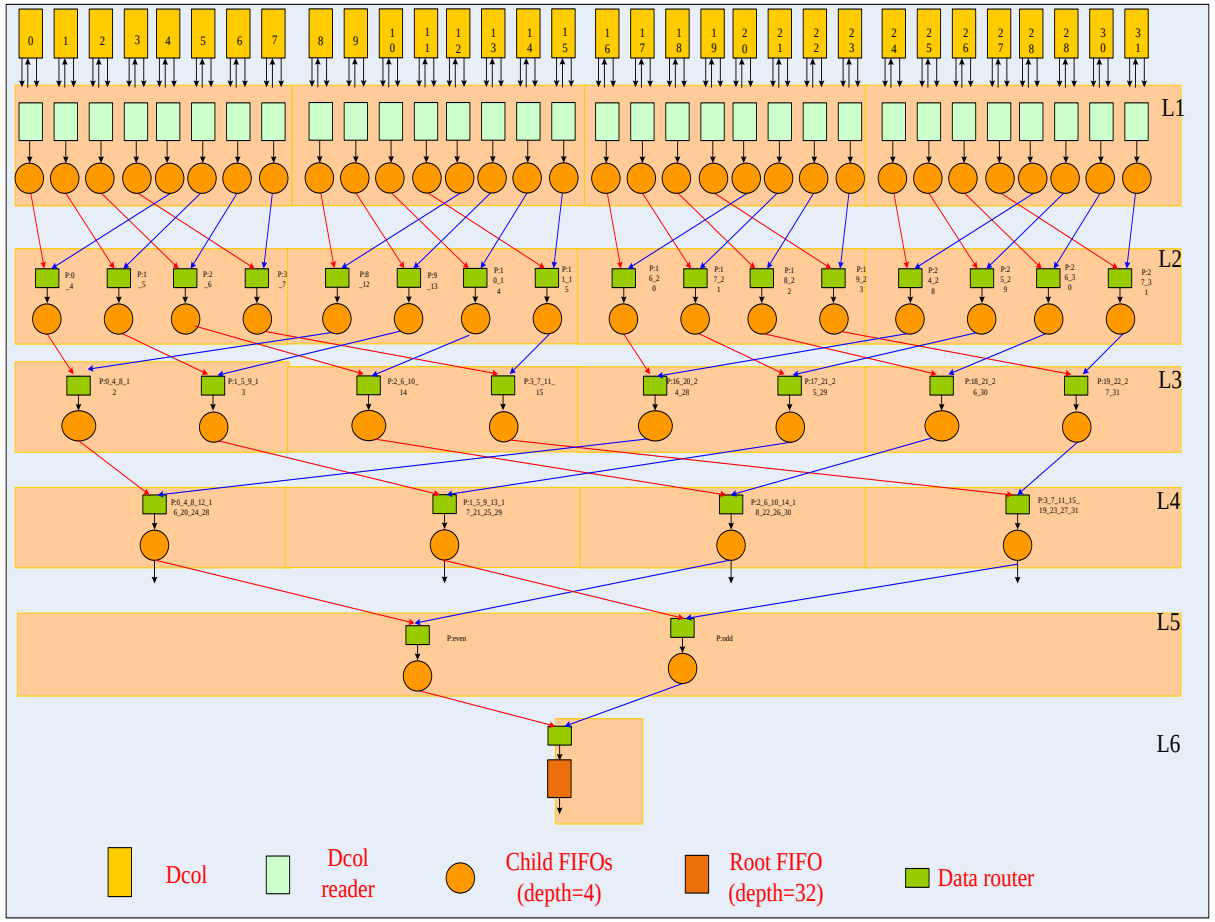
TaichuPix1：One FIFO for each Dcol

- 12 words（corresponding 4 hits with cluster size of 3）
- 384 words in total

TaichuPix2/3：a shared FIFO tree

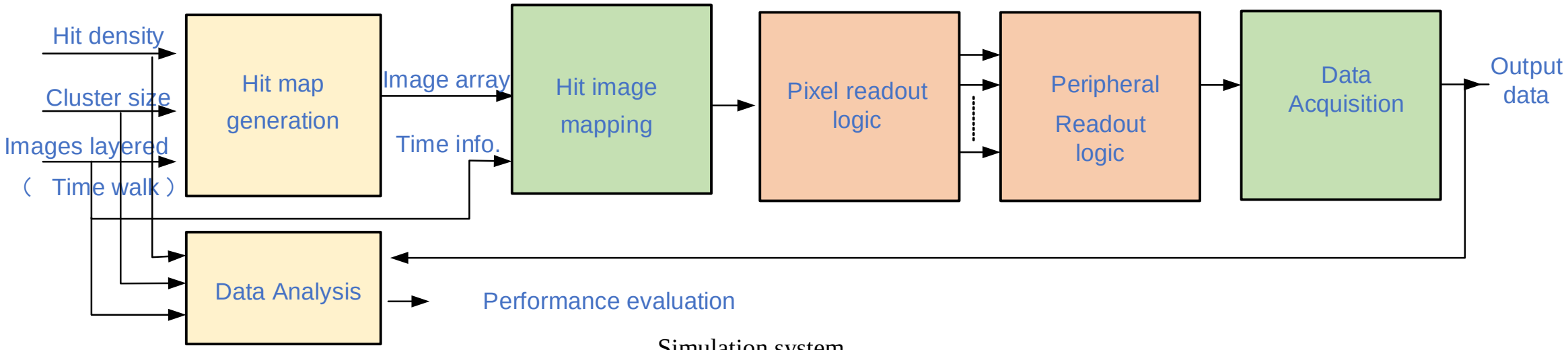
- 280 words in total
- 8.7(in average) - 52(in maximal)words for each Dcol
- Cross access to reduce the conflicts in one cluster



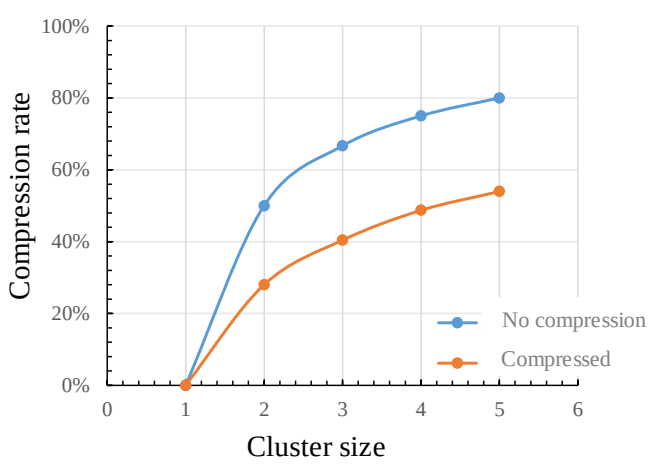


- Advantages：Higher data rate can be accepted. The die size is reduced (The layout height is reduced from 1.3mm to 1.1mm). The loads on the clock transmission line are reduced.
- Costs：The control logics are much complicated.

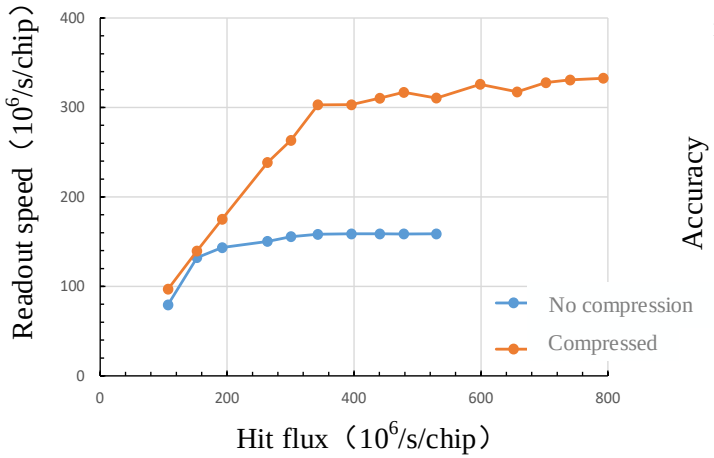
Simulation of the chip readout



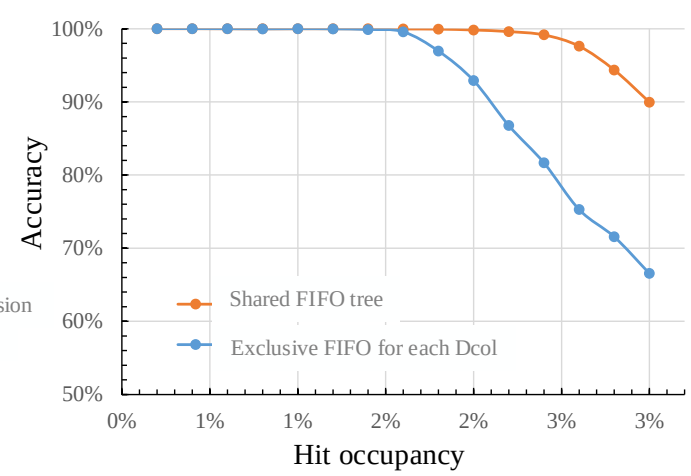
Simulation system



(a)



(b)



(c)

Simulation of TaichuPix3 & TaichuPix1 (the cluster size is 3 in Fig (b) and (c))

(a) Compression rate vs cluster size (b) Readout speed vs hit flux (c) Readout accuracy vs hit occupancy

Chip test results

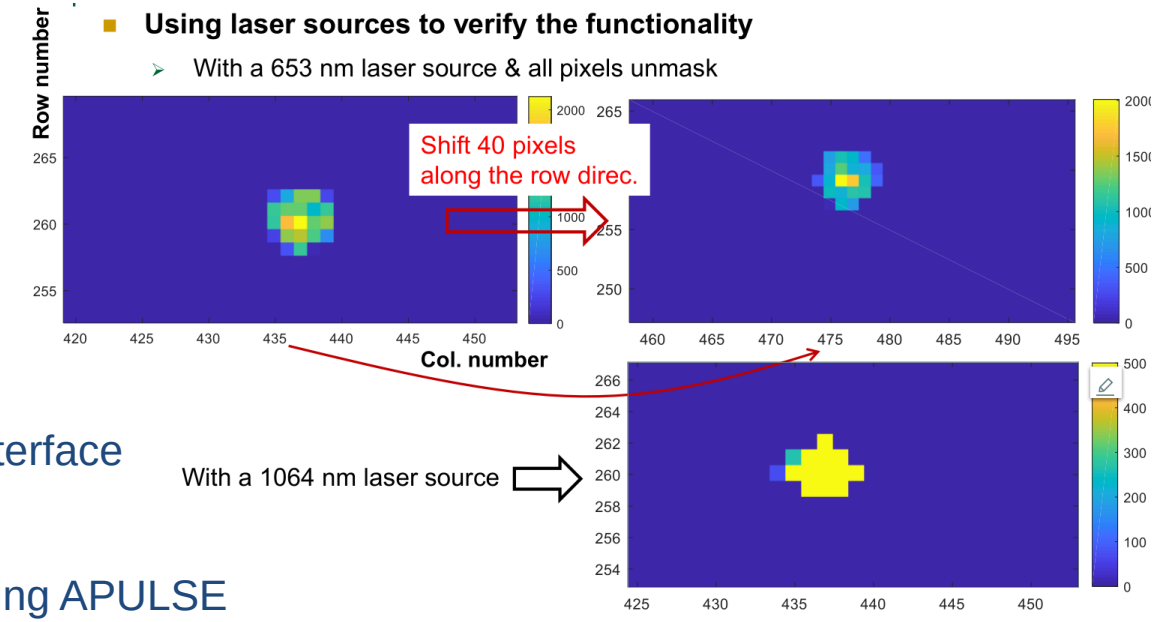
- Chip size：15.9 mm ×25.7 mm
- Noise：
  - Noise：FPN 43 e^-, random ~12 e^-
  - Threshold：~215 e^-
- Function test with Laser：Work well with

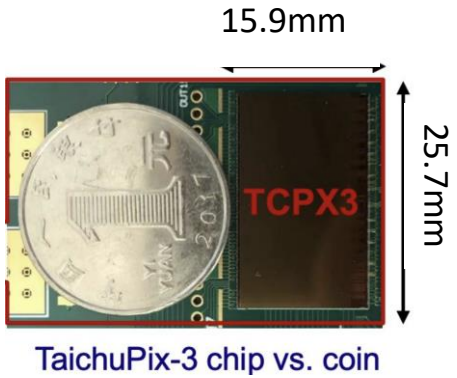
Sensor+ pixel analog + pixel digital + periphery readout + data interface

- Response speed

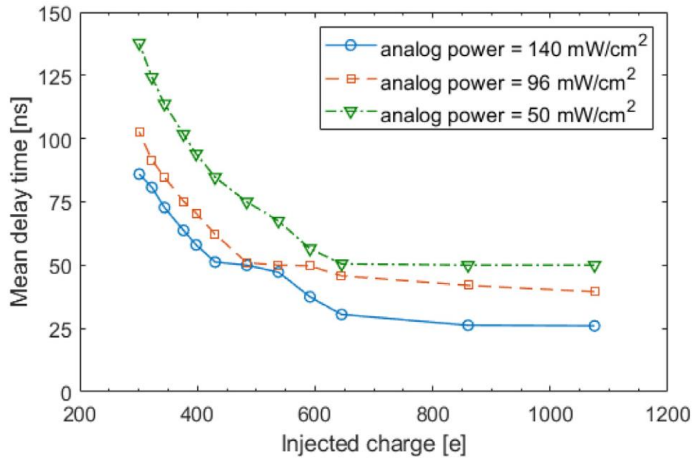
  the statistics of timestamps in output digital data when providing APULSE
  - Time walk: ~ 60-95 ns
- Power consumption：

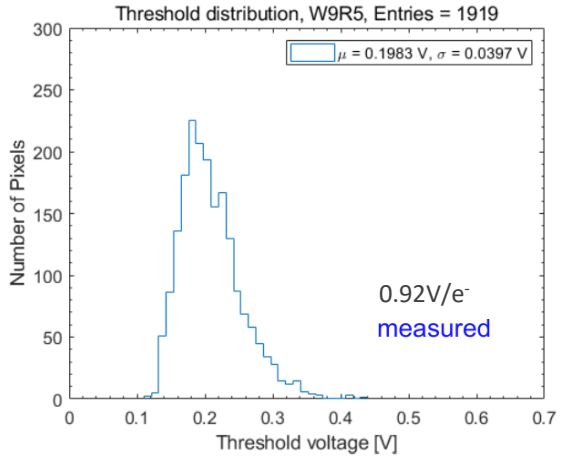
89-164 mW/cm^2 (with different Bias currents) @ Clk: 40 MHz & Serdes: 160 Mbps

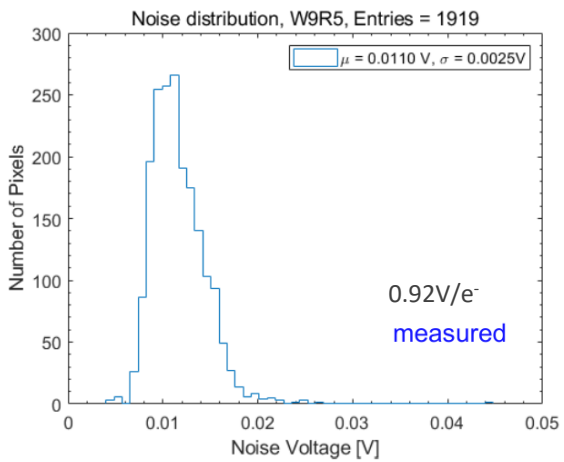




TaichuPix-3 chip vs. coin

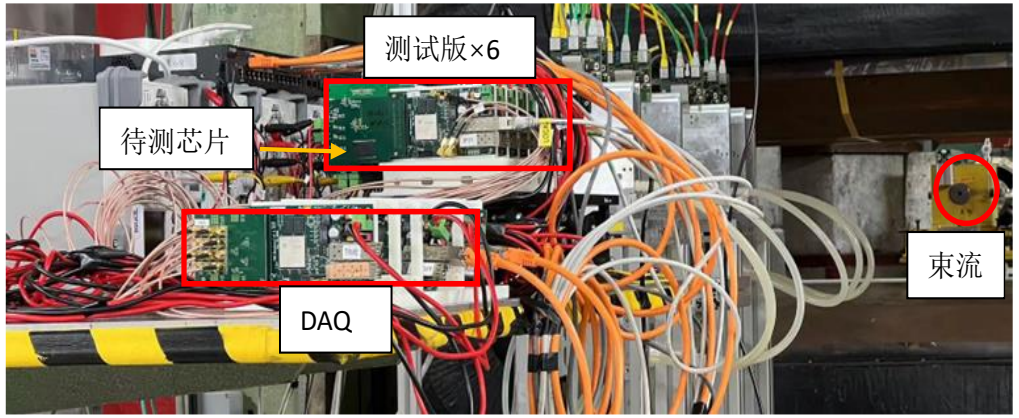






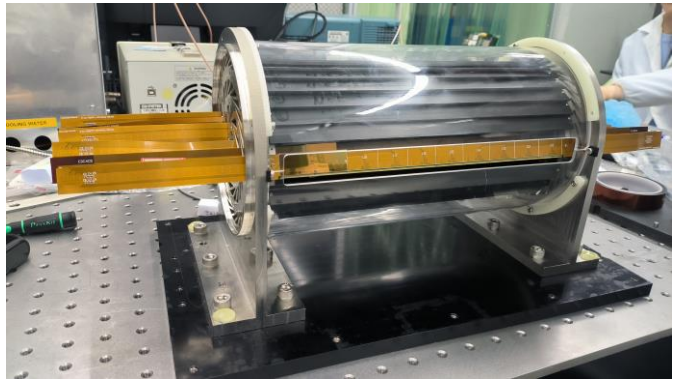
Beam test @DESY

- Telescope tested in December 2022

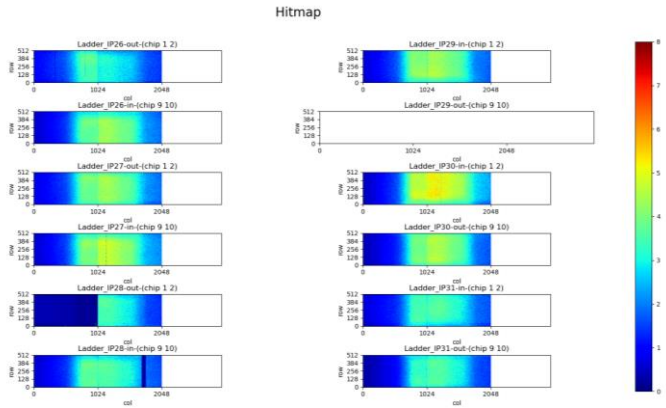


Telescope with 6 PCBs

- Prototype tested in April 2023



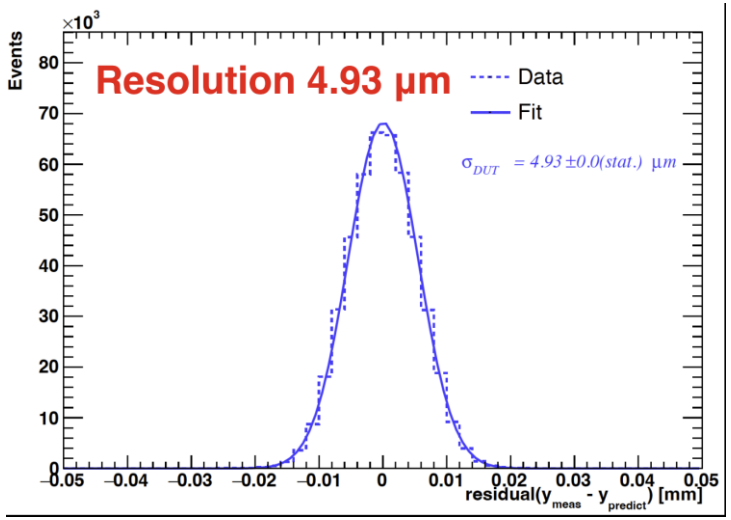
Prototype（6 ladders， 4chips/ladder）



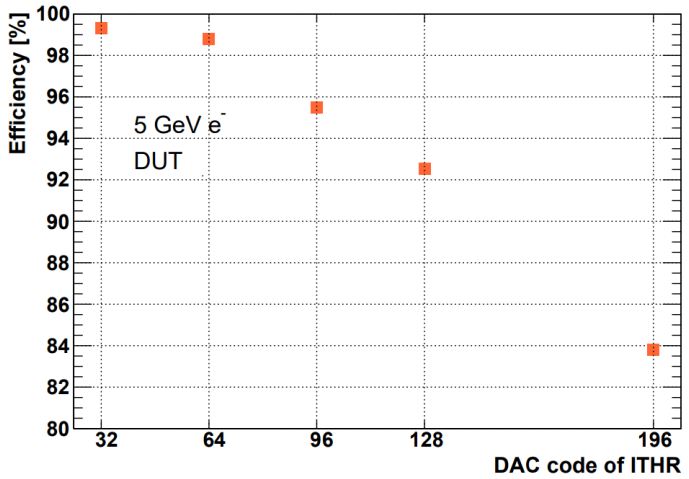
Hit maps on Prototype

- Results
  - Spatial resolution: ~5 um
  - Detection efficiency：~99%

<u>The resolution and efficiency in the prototype is slightly worse than in the telescope.</u>



Resolution of Prototype



Detection efficiency of a DUT on the prototype

Summary

- The design specifications and the implementation of TaichuPix3 are introduced. Fast pixel design and high-speed peripheral readout logic were adopted to achieve high hit rate readout with large pixel array.
- A simulation system is constructed to analyze the chip readout with different cluster sizes and hit rates. The results show that the real-time data compression and the shared FIFO tree are helpful for fast data readout.
- The test results of the prototype and the telescope indicate that the spatial resolution of TaichuPix3 can reach 5 μm and the detection efficiency can be above 99%.

Future works

- The tests are still progressing. The performances in the trigger mode and in the high data rate mode still need to be evaluated.
- The power consumption and the robust of the chip should be improved.
- TDR of the accelerator indicates higher data rate and new challenges, the new requirements are studying.

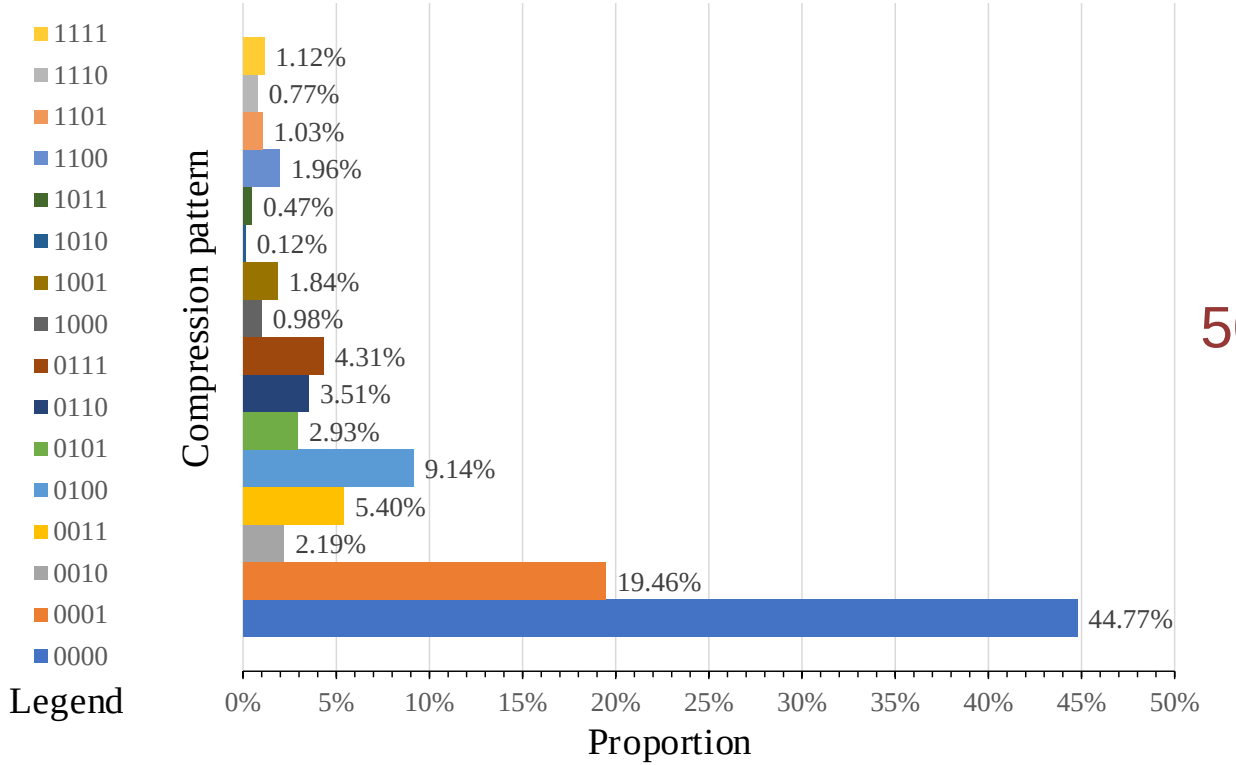
Acknowledgement

We greatly acknowledge DESY for providing the beam test environment and lots of supports!

Thank you for your attention!

Test Results

- The compression function is indicated feasible in the single chip test. The compressibility of the data has been preliminarily calculated. Practicality still need to be evaluated in advance.

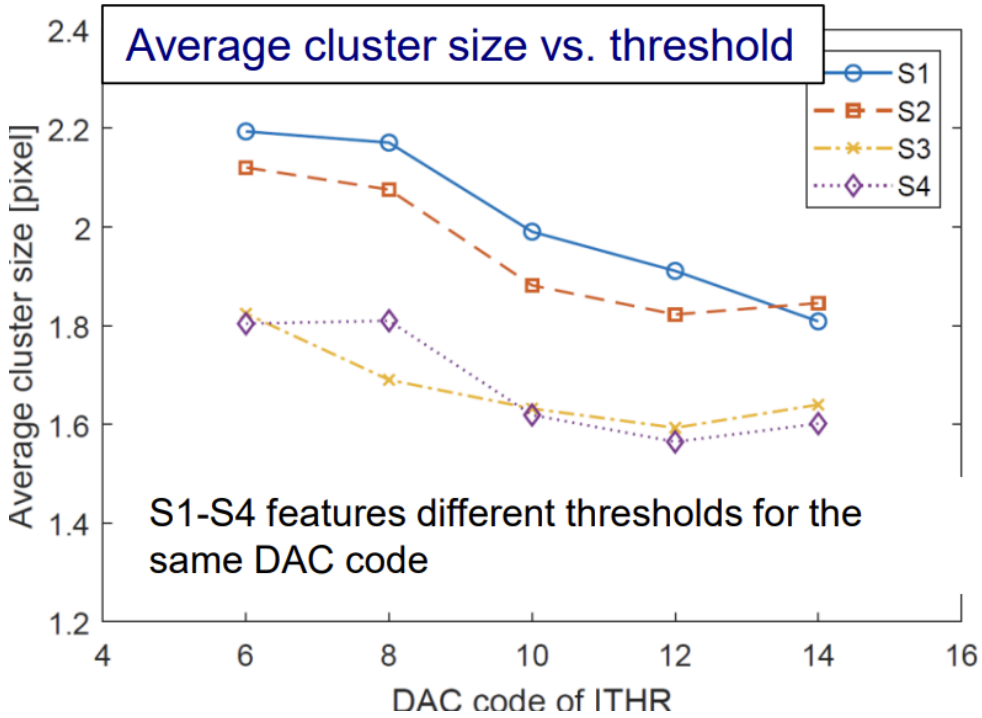


50% of data is compressible !

Probability of each compressed code appearing under 90Sr source irradiation in TaichuPix3

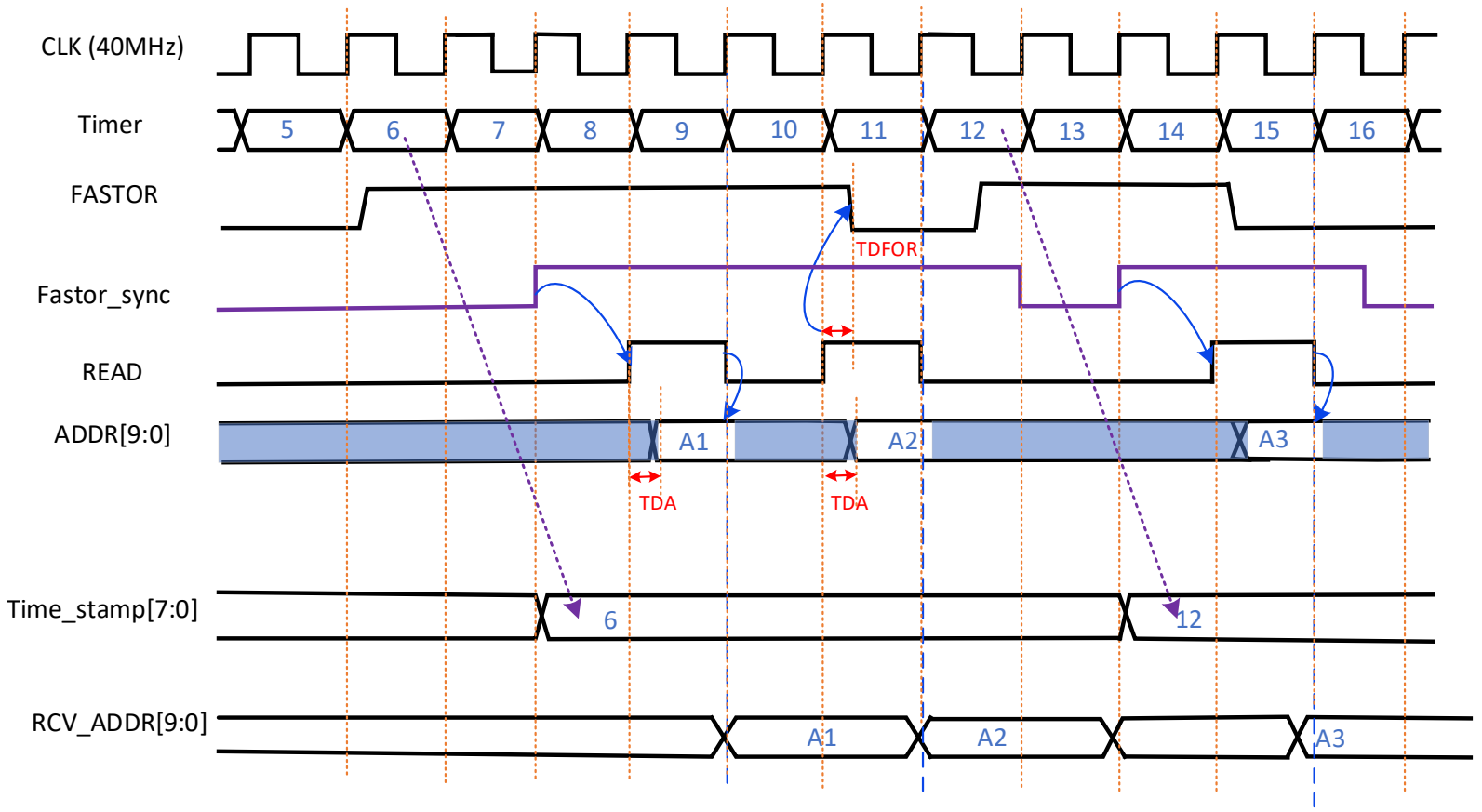
Cluster size vs. threshold

Sectors	Front-end design features
S1	Reference design, inherited from TaichuPix-1
S2	PMOS in independent N-wells
S3	One transistor in an enclosed layout
S4	Increased transistor size to reduce the threshold dispersion



TaichuPix2 under ^{90}Sr source

Data match in trigger mode



- In order to reduce the pixel area, the timestamp is only recorded in Dcol level. Uncertain of the timestamp is considered in the trigger discriminating logic.

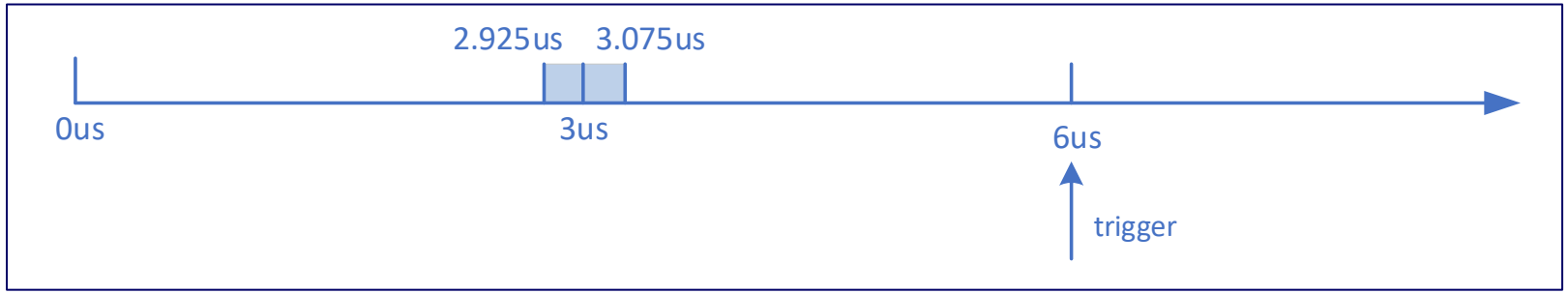
Data match in trigger mode

- Register control of trigger parameters:

TRIGGER_LATENCY: 0-6 μs (8-bit register)

=> Only the data in recent 6 μ s are stored; the old data is discarded.

TRIGGER_UNCERTAIN: 0-175 ns with step of 25 ns (3-bit register)

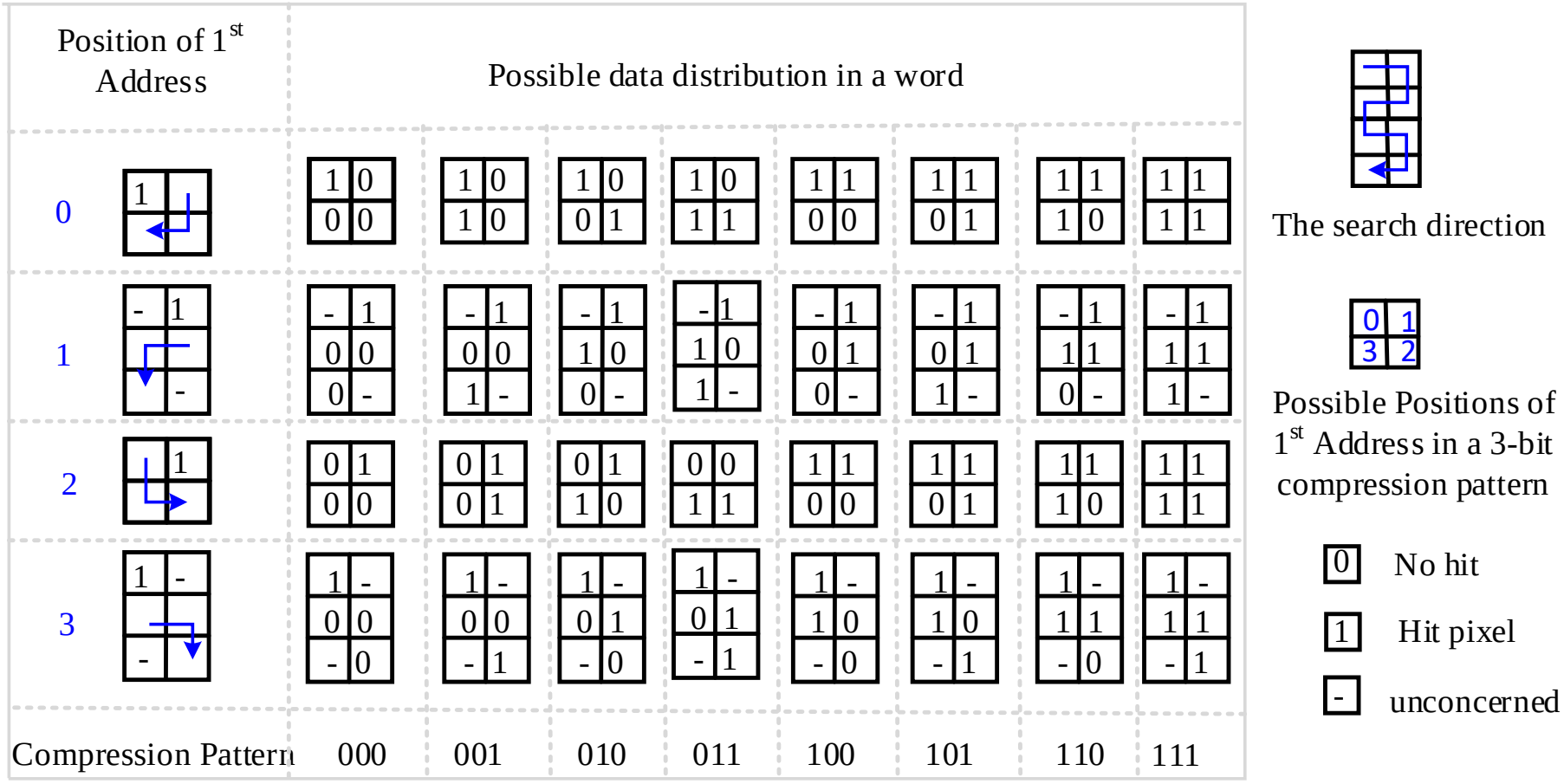


Example of setting trigger latency and trigger uncertain

- Example: Suppose the trigger signal comes at 6 μs, and users wants to acquire the hits from 2.925 μ s to 3.075 μs, then we should set TRIGGER_LATENCY as 8'd 123 (123*25 ns = 3.075 μs), and TRIGGER_UNCERTAIN as 3'b110 (6*25 ns = 0.15 μ s).

Real-time data compression

- Recording the address of the first pixels in a package, the following three pixels are indicated by a three-bit code, where “0” indicates no hit in the pixel and “1” indicates a hit pixel.



Example of Data compression in peripheral logic

The hit density in CEPC-CDR

Parameter	Unit	Higgs	W	Z
Bunch spacing	ns	680	210	25
Hit density	hits/bunch/cm^2	2.4	2.3	0.25
	hits/bunch	7.87	7.54	0.82
	pixels/bunch	24	24	2.5
Hit pixel rate	MHz/cm^2	12	36	32
	MHz/chip	36	120	96
Chip data rate (triggerless, no 8b10b)	MHz/32bit	36	120	96
Chip data rate (trigger)	MHz/32bit （min）	1.2	1.2	0.125
	MHz/32bit （max）	1.2	1.2	1
Designed data rate (trigger)	MHz/32bit	5		
	Mbps	160		
Designed data rate (triggerless, 8b10b)	MHz/64bit	70		
	Gbps	4.48*		
~~**Designed data rate (triggerless, JESD204b)**~~	~~MHz/40bit~~	~~120~~		
	~~Gbps~~	~~4.8~~		