Study of single-slope ADC using FPGA TDC for streaming readout data acquisition

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Outline

- Introduction
  - Motivation
  - Single-slope ADC
- Ongoing studies
- Summary

Introduction

R&D for general purpose streaming readout

- Software
  - NestDAQ (talk by Igarashi)
- Frontend electronics
  - TDC module : AMANEQ, clock sync. : MIKUMARI and LACCP (talk by Honda)
- Application
  - J-PARC, Grand Raiden in RCNP (talk by Igarashi, and Ota)
- Standardization
  - SPADI-Alliance (talk by Ota)

Motivation : To extend applicable field of streaming DAQ

What we have already achieved : free-streaming TDC

- Hit arrival time
- Charge measurement using Time-over-Threshold (ToT)
  - Still issues: pulse pile up, linearity

Charge measurement without dead time ⇒ challenging!

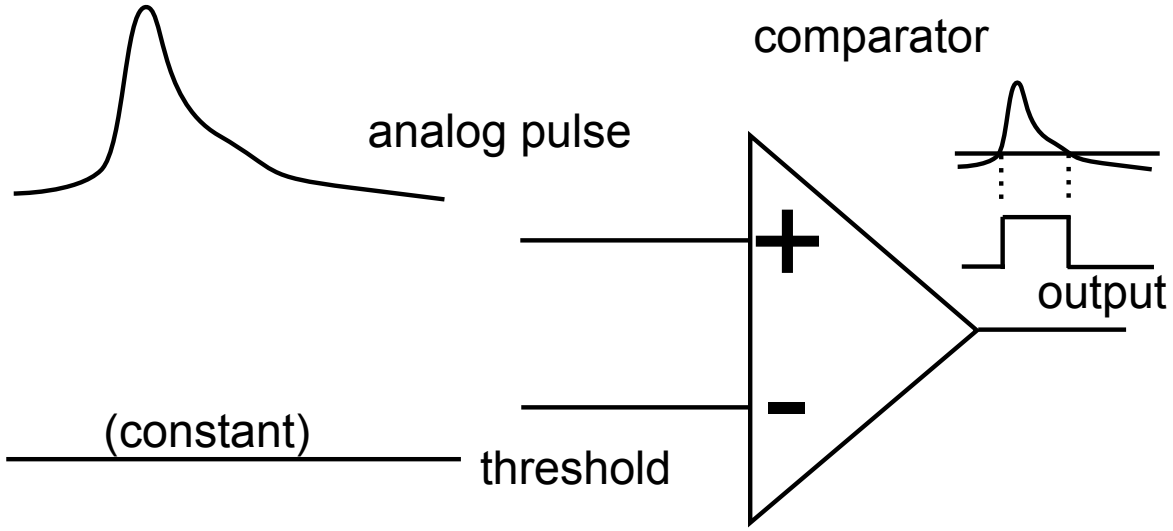
- High-speed waveform digitizers
  - Commercially available but expensive

➡ **Single-slope ADC (SS-ADC)** as a cost-effective circuit

SS-ADC : Principle (1) 1-bit A/D conversion with comparator

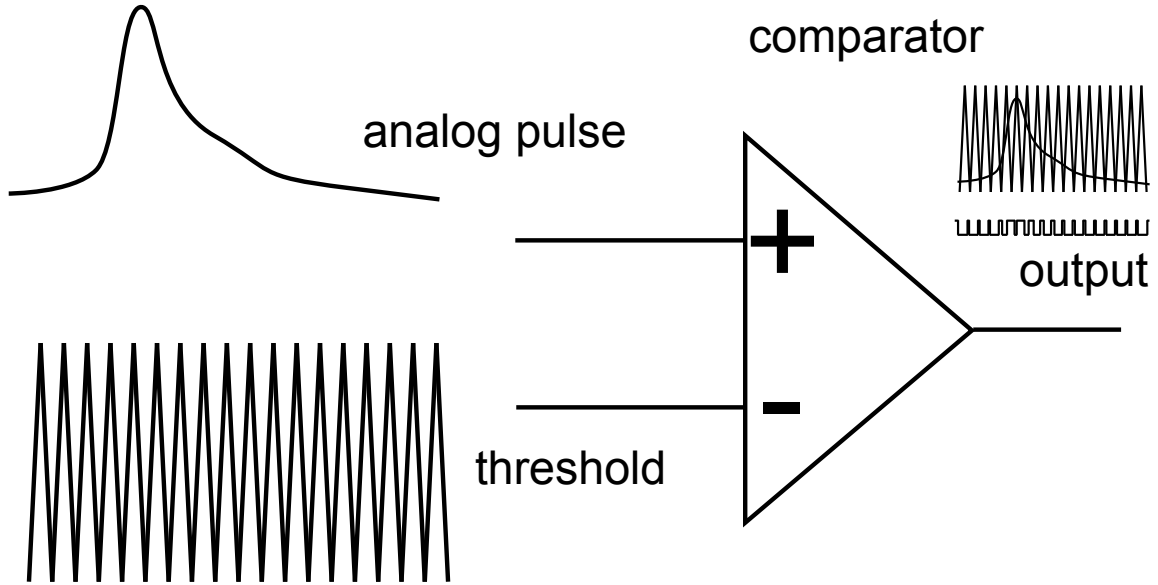
Normal usage of comparator

Threshold = **constant**



In SS-ADC

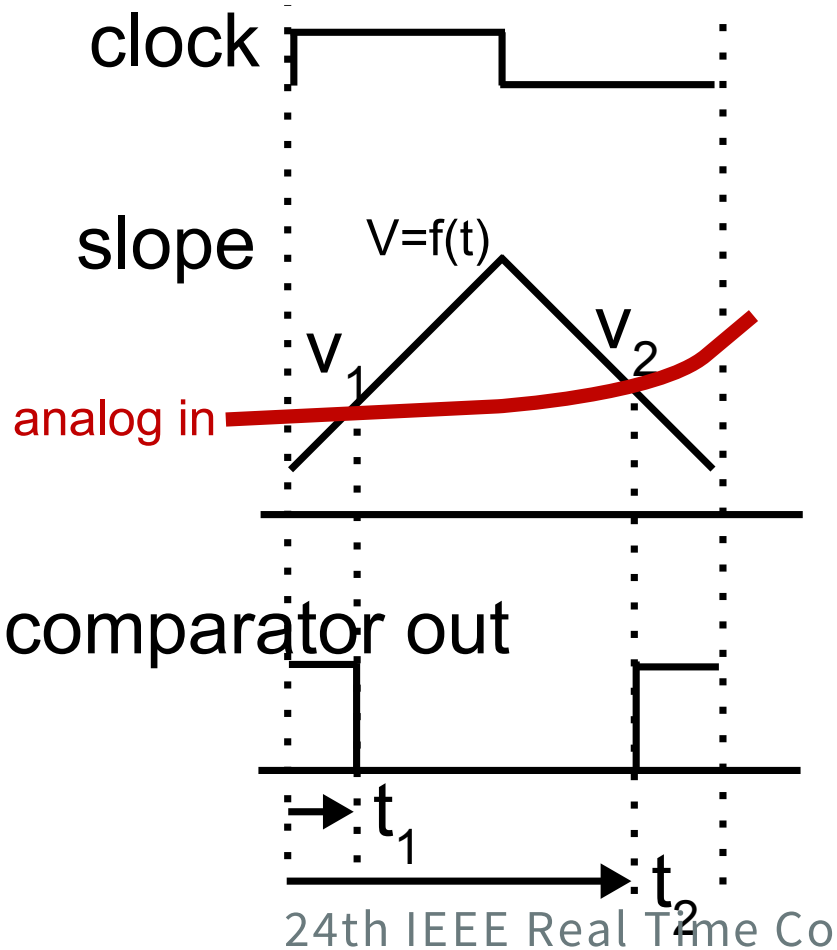
Threshold = **periodic slope**

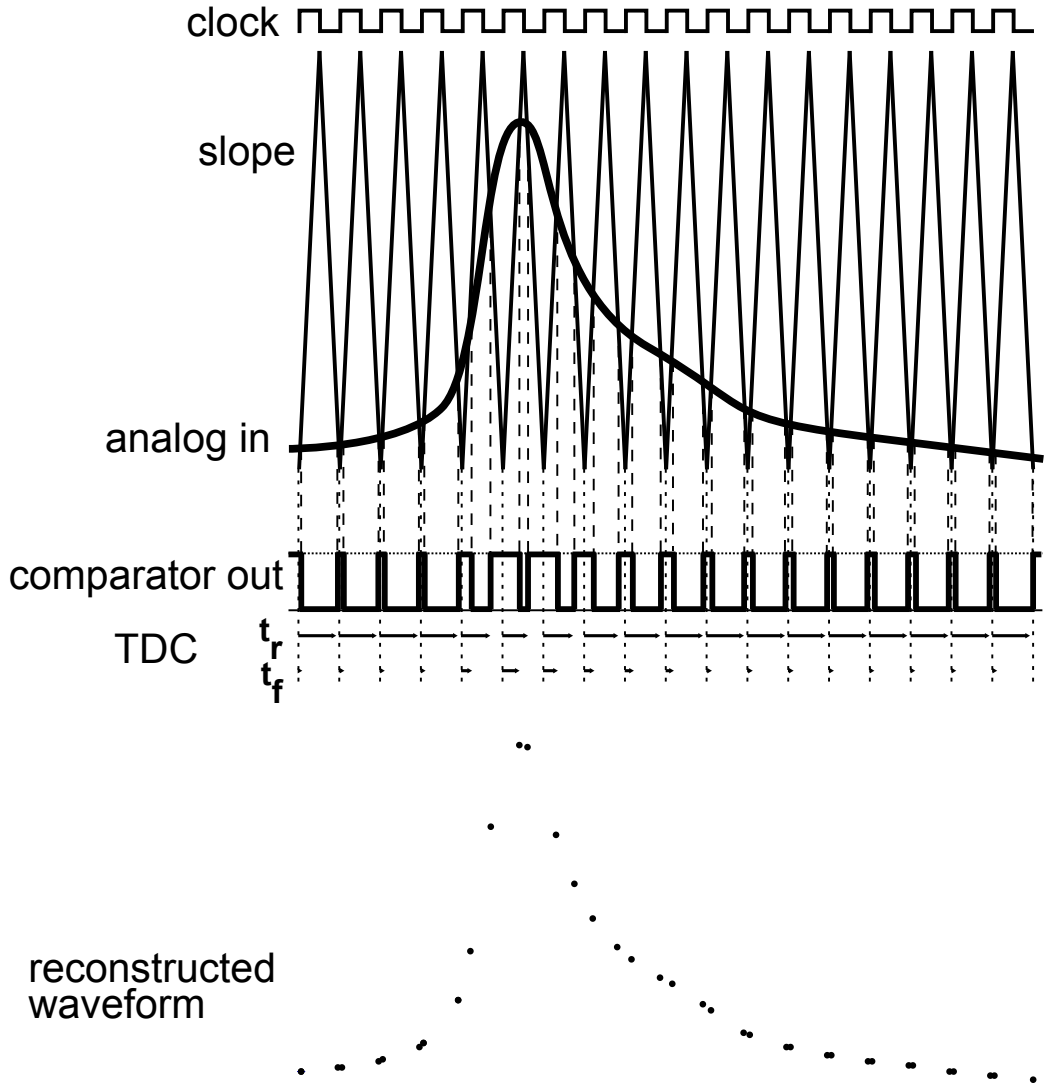


Measure the time of level-crossing points with HR-TDC

SS-ADC : Principle (2) Waveform reconstruction

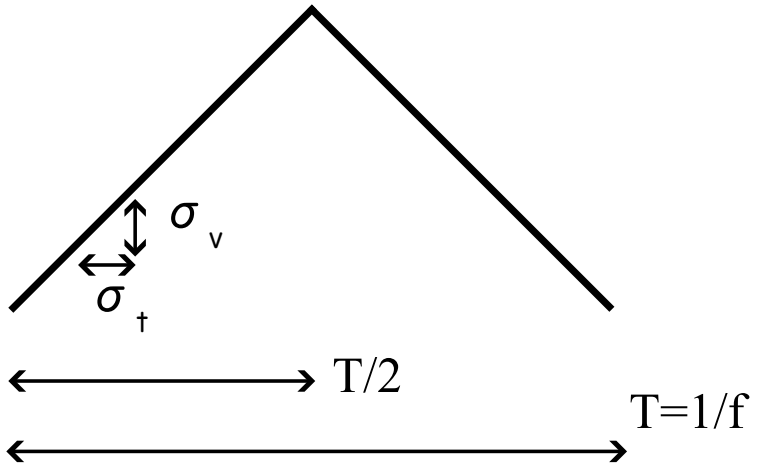
- Slope and HR-TDC clock ⇒ **synchronized**
- **Known slope shape**: $V = f(t)$





SS-ADC : Rough estimation of performance

- σ_t : TDC resolution
- f, T : slope repetition rate, period
- N bits : ADC resolution
  - $\frac{T}{2} = \frac{1}{2f} = 2^N \cdot \sigma_t, \quad \frac{\sigma_V}{\sigma_t} \sim \frac{dV}{dt}$
  - $N = \log_2 \frac{T}{2\sigma_t}$



Example :
σ_t = 10 ps, f = 500 MHz (= 1 Gsps)
$\Rightarrow N = \log_2 100 = 6.6$

ref. 600 Msps, 7-ENOB
L. Leuenberger *et al*,
doi:10.1145/3431920.3439287

In a real environment, SS-ADC performance would be affected by noise, jitter, slope shape, stability, ...

SS-ADC : Pros and Cons

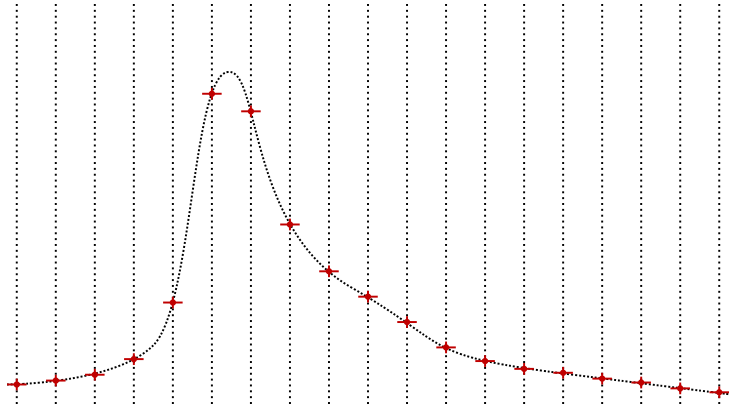
Pros

- Fast waveform sampling (100 MSps - 1 Gsps)
- Fewer external components
  - Compact, **low-cost**
  - COTS

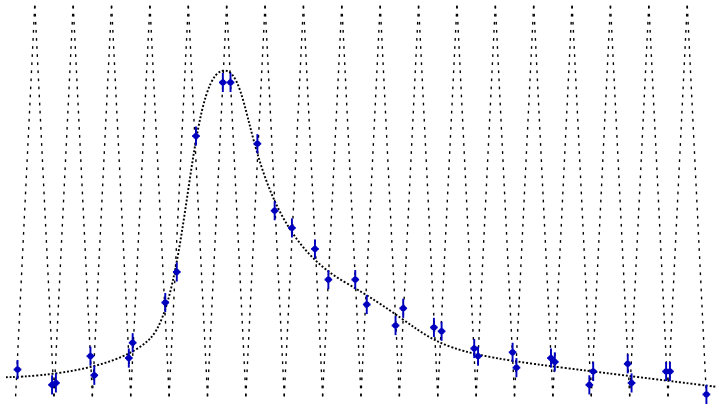
Cons

- **ADC resolution (single measurement): Low to moderate**
  - Trade-off: resolution ⇔ sampling rate
- **Unevenly-sampled signal**

Normal ADC



SS-ADC



Performance evaluation of SS-ADC

- ADC linearity, voltage range
- Time resolution, charge resolution, sampling rate
- Effect of noise, signal shape
- Effect of slope shape
  - Triangle, sinusoidal, exponential decay
- How to extract time and charge information
  - Averaging, interpolation, waveform fitting, AI, ...
- Scope of application, applicable detectors

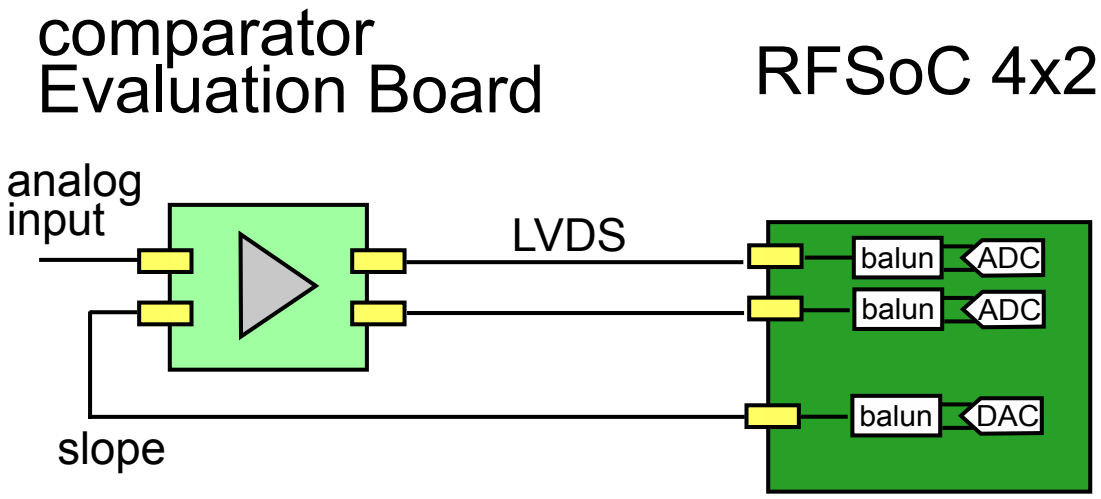
➡️ Simulation study and FPGA firmware development

Ongoing studies

Studies with hardware

- Performance evaluation of SS-ADC **independent of** ⬅️ here **FPGA-TDC implementation**
  - Commercial comparator board + high-speed DAC and ADC
- Evaluation of SS-ADC with FPGA-TDC (a few channels)
- Evaluation of SS-ADC with FPGA-TDC (multi-channel board)

SS-ADC performance evaluation without FPGA-TDC



ADC, DAC:

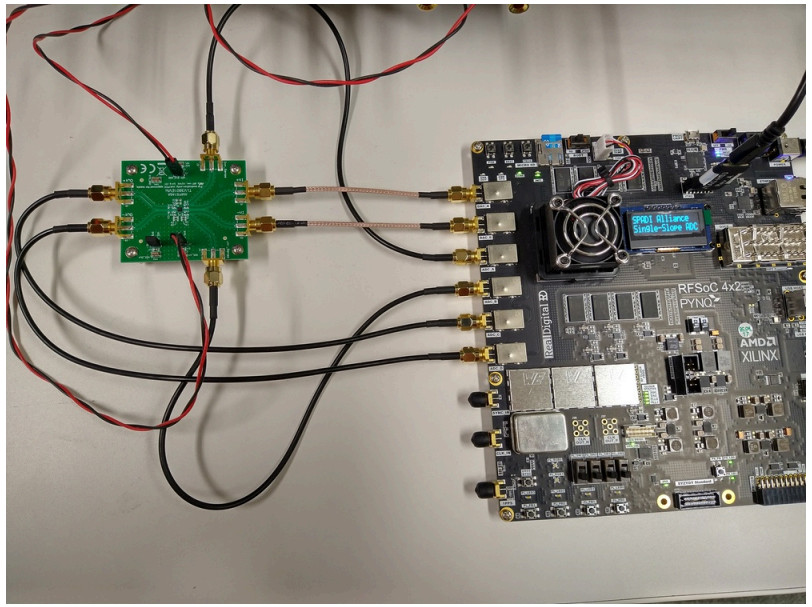
- AC coupled
- balun : 10 MHz - 10 GHz

RFSoC4x2 (Real Digital)

- DAC (14 bit, max. 9.85 Gsps)
  - **Arbitrary slope shape**
  - Analog pulse emulation
- ADC (12 bit, max. 5 Gsps)
  - Record LVDS waveform at comparator output
  - Analyze LVDS waveform
    - **HR-TDC emulation**

Test bed using RFSoC4x2 and comparator eval. board

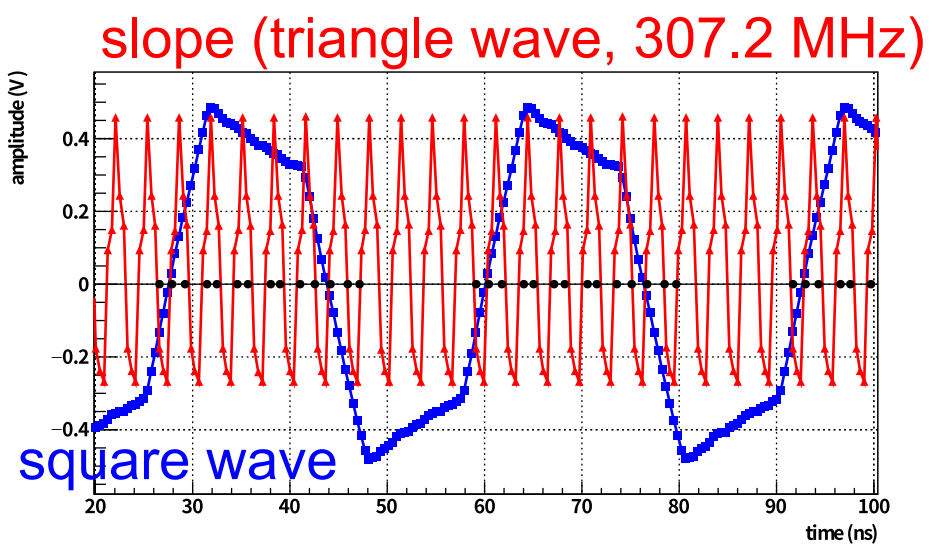
- Firmware : modified from RFSoC-PYNQ
- DAC: 4.9152 Gsps
  - Triangle wave 307.2 MHz as a slope
  - Square wave as a pulse to be measured
- ADC: 2.4576 Gsps
  - Comparator input (+, -)
  - LVDS out (+, -)

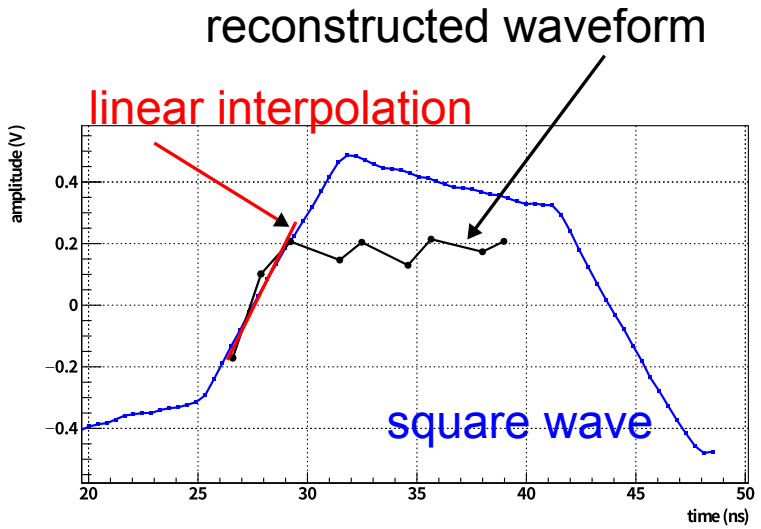


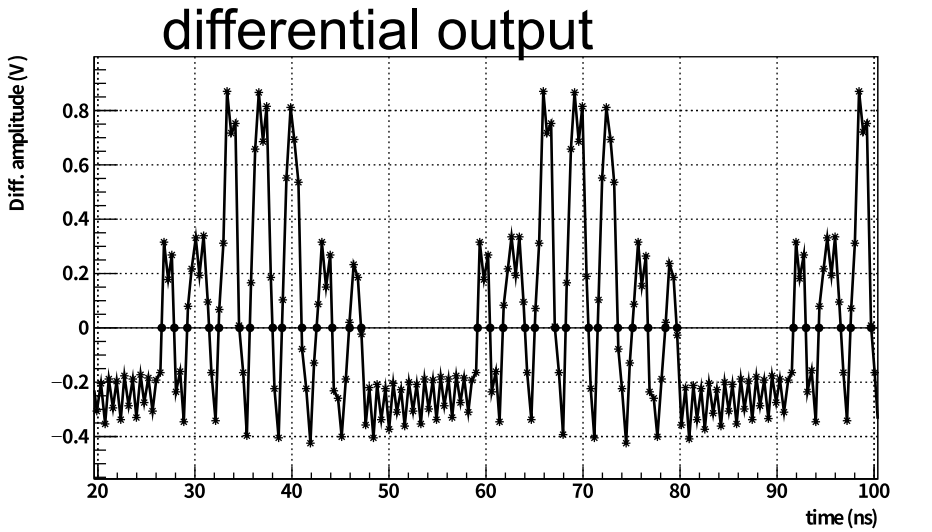
Comparator : TLV3801 (TI)

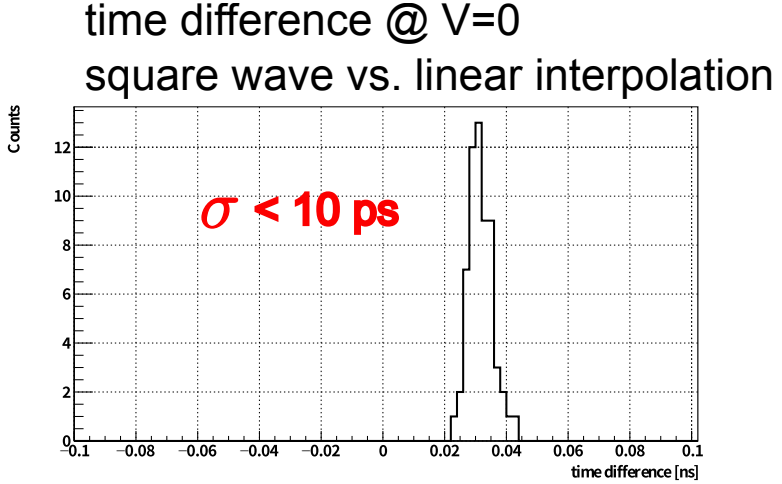
- Max input 3 GHz
- low cost : a few $/chip

Timing performance test









The timing performance is not much degraded.

Summary

Single-slope ADC

- Periodic slope + comparator + HR-TDC
- Waveform digitizer with moderate performance
  - Sampling rate : 100 Msps - 1 Gsps, ADC resolution : 5 - 8 bit
  - Need to process unevenly-sampled data points if we want to get the best performance

Ongoing studies

- Evaluation with comparator board and RFSoC
  - Independent of HR-TDC implementation
  - Input range depends on amplitude of the slope. (typ. V_{pp} = 0.5-0.7 V in this study)

Future work

- PCB design, implementation of FPGA-TDC
- Data processing method