Contribution ID: **113** Type: **Oral presentation**

Test and data acquisition software for CPV-4

Friday 26 April 2024 09:20 (20 minutes)

Abstract: Combining 3D vertical integration technology with SOI pixel process, the CPV-4 chip integrates sensing diode and analog front-end functions into the lower-tier chip, while hit information storage and read-out functions are implemented in the upper-tier chip. This reduces pixel size and power consumption, thereby enhancing the spatial resolution of the detector. Due to the complexity of the SOI-3D process, a more flexible and reliable readout system is required to test the performance of the chips. Therefore, the development of the CPV-4 chip data acquisition system is completed using the IPbus protocol as the data transmission protocol. In order to decouple the development of the data acquisition system from the chip development, an FPGA based CPV-4 upper-tier chip emulator was designed based on the real chip's specifications. The emulator was used to verify the functionality of the data acquisition system, demonstrating the reliability and stability of the data acquisition system. The DAQ system will be used to validate the chip design and fabrication process of SOI-3D, and is also applicable for testing and validation of other complex pixel chips.

Key Words: CPV-4; Pixel sensor; Data Acquisition System; IPbus.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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Session Classification: Oral presentations, CANPS Award

Track Classification: Data Acquisition and Trigger Architectures