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Assessing NI FPGA-based platform with MXIe interface for use in ITER hard real-time investment protection applications

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The ITER Interlock Control System assumes a crucial role in the tokamak operation to protect the machine against failures. Consequently, it must be developed in compliance with the most challenging requirements. The NI CompactRIO technology was chosen by ITER as the FPGA-based platform to develop and implement the investment protection functions, with strict time-constraints. This contribution focuses on the specific requirements for the ITER Advanced Protection System where the disruption mitigation control function requires a sequenced release of hydrogen ice pellets with jitter lower than 1ms.
The cRIO platform used is the NI9159, which provides an MXIe interface (using a PCIe bridge) to interface the Virtex 5 LX110 FPGA with a host computer running a Linux preempt kernel. ITER decided to improve two important requirements: the MXIe interface communication latency by redesigning the ITER NI-RIO Linux device driver; and the ability to time events in the FPGA logic by designing a specific firmware module based on the Precision Time Protocol (ITER TCN). This contribution details the design methodology followed, the firmware and software elements implemented, the performance obtained in latency and time-keeping accuracy of the approach.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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