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## General-purpose data streaming TDCs for nuclear and hadron experiments in Japan

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We have developed a trigger-less data-streaming-type high- and low-resolution TDC called Str-HR(LR)TDC using an AMD Kintex-7 FPGA to develop a general-purpose trigger-less DAQ system in Japan. The trigger-less DAQ system shows promise as a leading candidate of the next standard of the DAQ field in the particle and nuclear experiments. The developed Str-TDCs has been designed for general use, not for a specific experiment. It is implemented on the general-purpose FPGA logic module called AMANEQ [1].

The developed Str-HRTDC consists of two blocks. Timing measurement is outsourced to the FPGA on the mezzanine card of AMANEQ where CARRY4 elements realize tapped-delay-line. The FPGA on AMANEQ collects data from two mezzanine cards and transfers it to a PC via 10-Gbps TCP/IP utilizing SiTCP-XG. For module synchronization, we have adopted the MIKUMARI-link technology [1]. The MIKUMARI is responsible for synchronizing the clock signal frequency and providing the reference timing for TDCs. In addition to its use for the FPGA on AMANEQ, it is also used for the synchronization between AMANEQ and the mezzanine cards. We tested Str-HRTDC by feeding the same input pulse to two synchronized AMANEQs. The obtained timing resolution was 24 ps ( $\sigma$ ).

In this contribution, we will present the technical specifications of Str-HRTDC, including its performances, the timing resolution, and the data transfer speed. We will also outline the implementation plan for incorporating Str-TDCs into other front-end electronics as a future prospect.

[1] R. Honda, IEEE TNS, 70 (6), 1102 (2023).

### Minioral

No

### IEEE Member

No

### Are you a student?

No

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