Development of a Fast Timing ASIC for Large-area SiPM Array Readout

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TRIDENT Collaboration

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Real Time Conference 2024, April 22

Outline

- Introduction
- Design of the SiPM array readout ASIC
- Status and plans
- Summary

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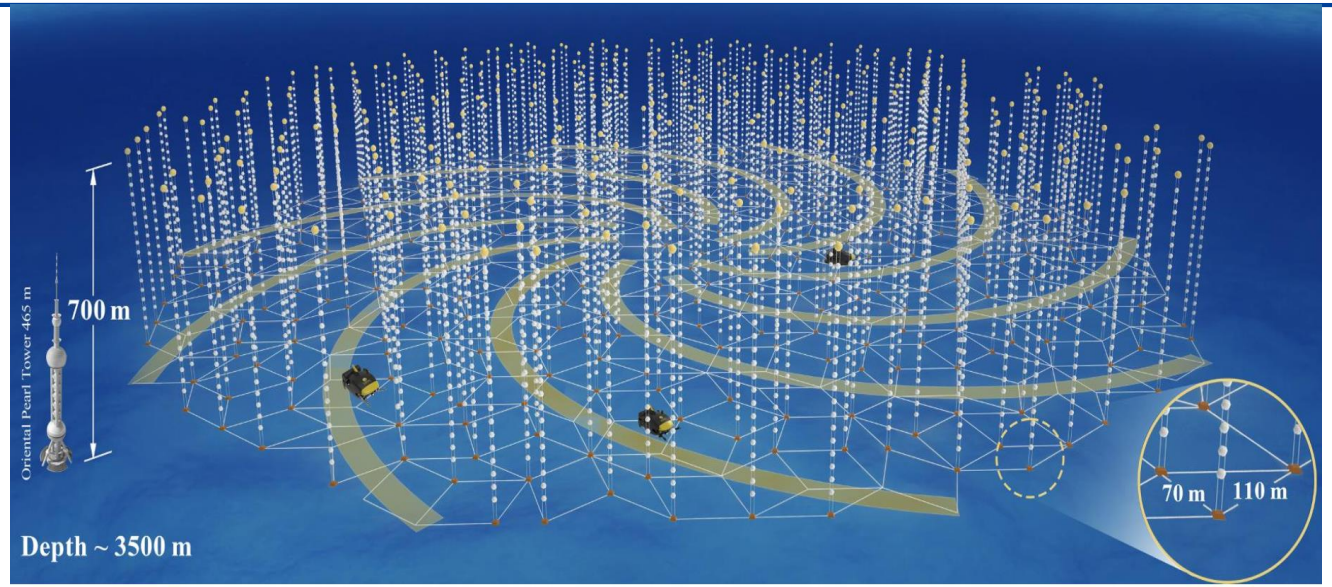
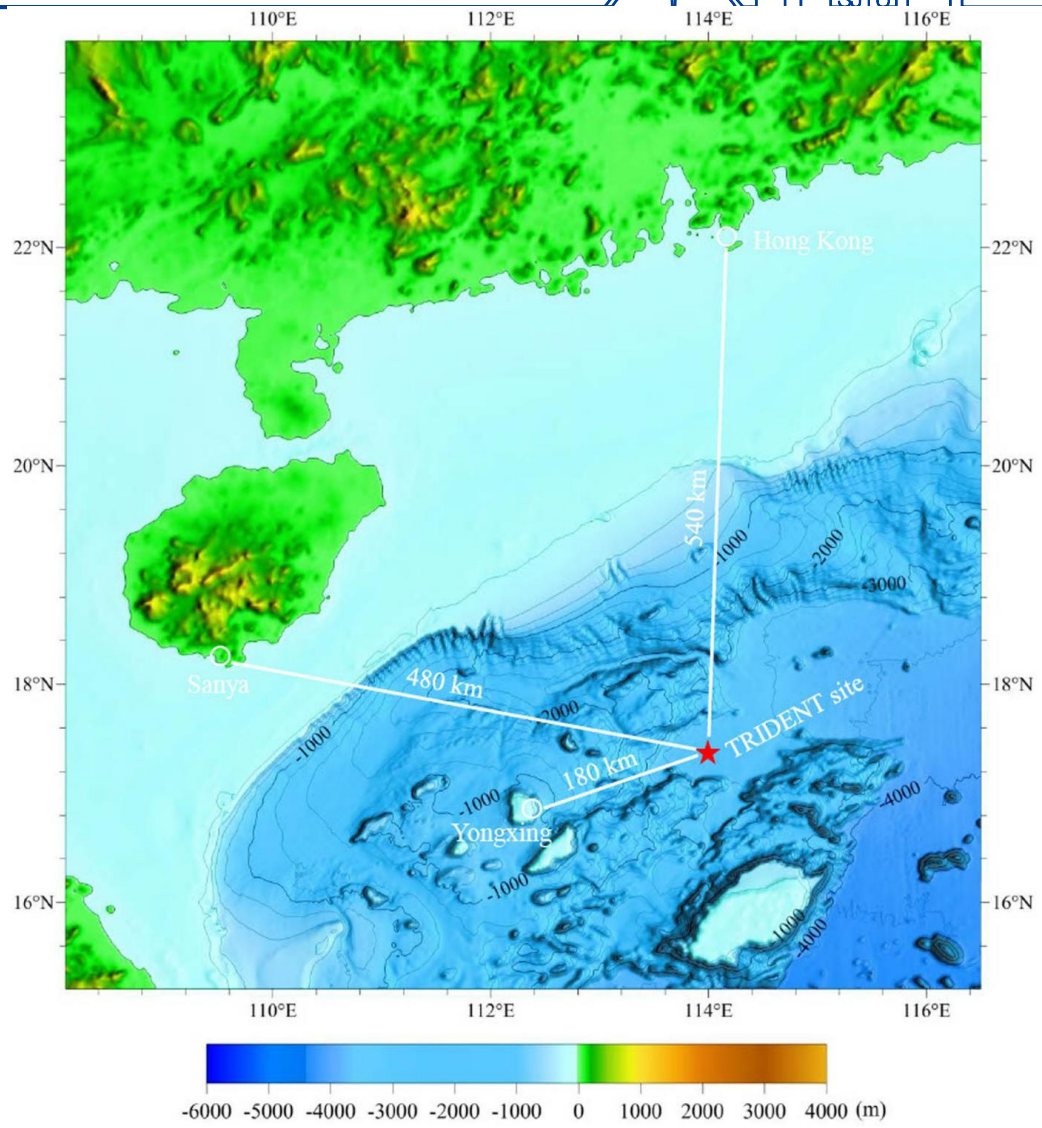
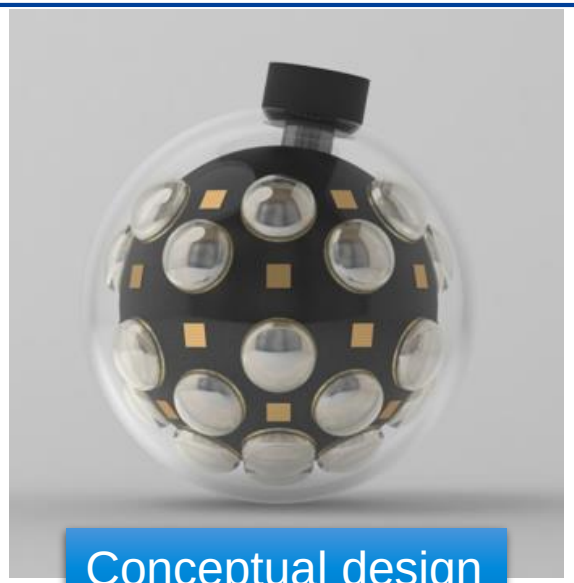
TRopIcal DEep-sea Neutrino Telescope





- **TRIDENT:** a next-generation multi-cubic-kilometer neutrino telescope
  - ~1200 strings, ~20 DOMs / string
- **TRIDENT pathfinder experiment** was completed in 2021.
  - The details of the pathfinder experiment are presented in *Nat. Astro. 10.1038/s41550-023-02087-6 (2023).*
- **TRIDENT phase-1** has started since 2022.

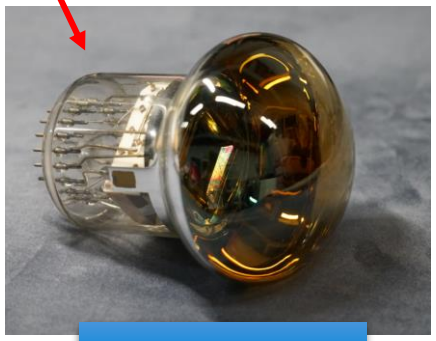
TRIDENT Hybrid Optical Module



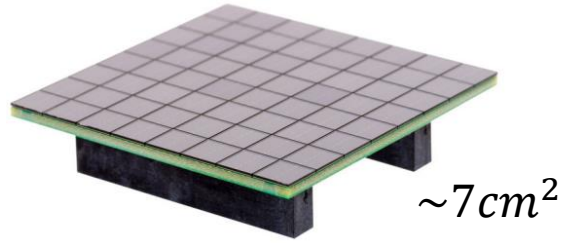
Conceptual design

Prototypes in progress

- **hDOM:** hybrid PMT + SiPM optical module
  - 31 3-inch PMTs: waveform
  - 24 SiPM arrays: hit time
- Large photon collection area + high-precision time resolution



3-inch PMT



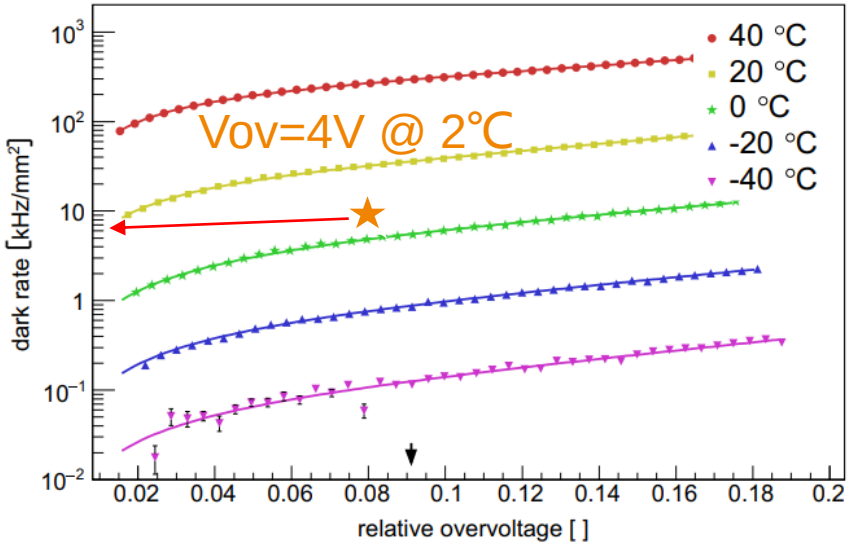
SiPM array

F. Hu, et al., PoS (ICRC2021) 1043

W. Zhi, et al., PoS (ICRC2023) 1213

Challenges of High-precision Time Measurement for SiPM Arrays

- Dark rate: $\sim 5\ kHz\ /\ mm^2$ @ 2 ~ 4 ℃
  - Reduced by an order at deep sea
  - Trigger scheme with PMTs
- Time walk correction
  - Time-over-Threshold (ToT) method
  - Correction with PMT data
  - …



Hamamatsu S13360-3050CS

$$RelativeOvervoltage = \frac{BiasVoltage - BreakdownVoltage}{BreakdownVoltage}$$

$$\sigma_{tot}^2 = \sigma_{jitter}^2 + \sigma_{walk}^2 + \sigma_{digitizer}^2$$

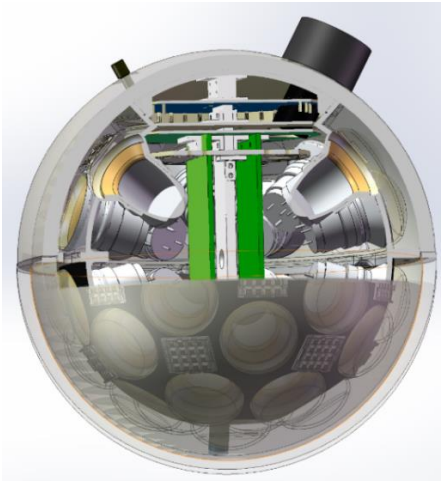
A. N. Otte, et al., NIM A (2017)

Challenges of High-precision Time Measurement for SiPM Arrays

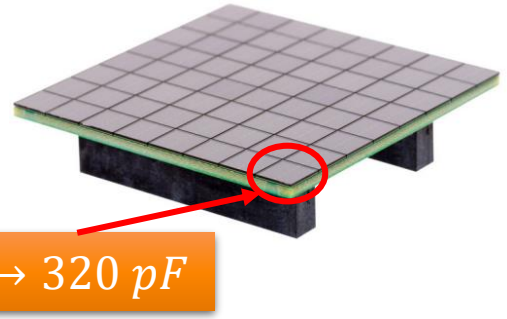
- Trade-off between signal-to-noise ratio and dark rate
- Small number of Cherenkov photons
  - Single photon detection sensitivity → limited amplitude
- Large input capacitance (~20 nF)
  - Limited bandwidth and rise time
- Limited space and power supply
  - Cost of submarine cables

$$\sigma_t \approx \frac{RiseTime \times NoiseRMS}{Amplitude}$$

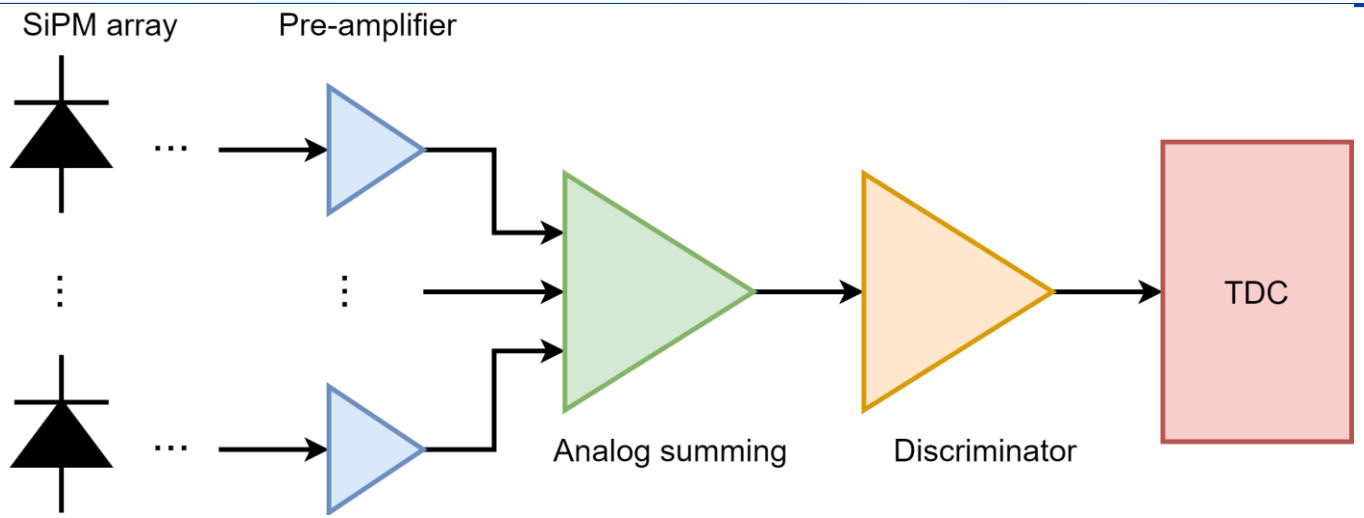
$$\sigma_{tot}^2 = \sigma_{jitter}^2 + \sigma_{walk}^2 + \sigma_{digitizer}^2$$



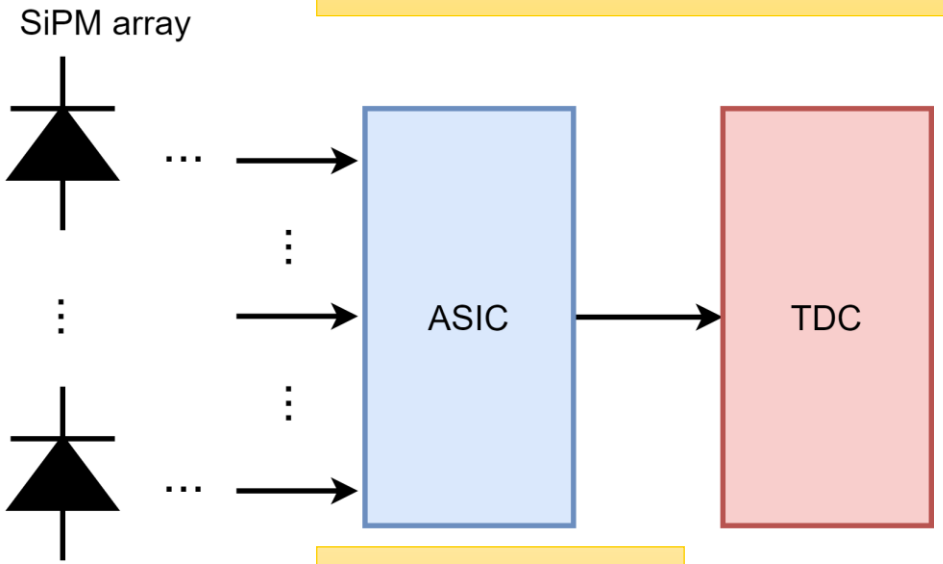
CAD model of hDOM



SiPM Array Readout Scheme



Commercial discrete device approach



ASIC approach

- The commercial discrete device approach is detailed in *arXiv:2403.02948.*
  - The single photon time resolution (SPTR) of a 4 × 4 SiPM (Hamamatsu S13360-3050PE) array (12 × 12 mm^2) is ~300 ps full width at half maximum (FWHM) with a power consumption of ~100 mW.
- Compared to the discrete device approach, this ASIC has the advantages of **higher integration and lower power consumption.**

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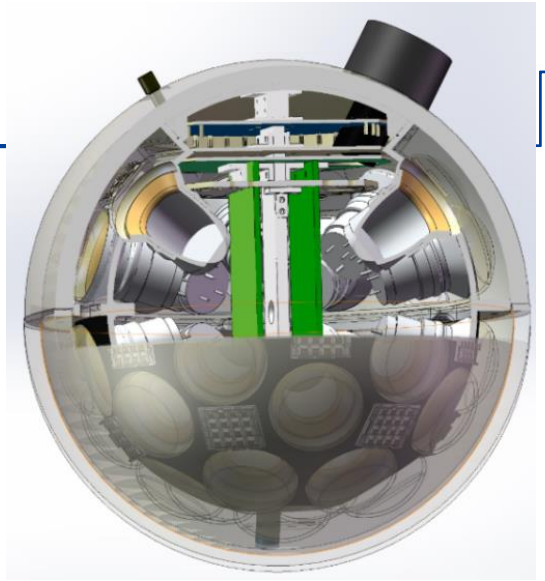
Requirements for the ASIC



- SPTR < 300 ps FWHM
- Input channel number: 16
- Number of wires connected to the FPGA: as few as possible
  - Limited space and number of IOs
- Power consumption: < 10 mW/channel

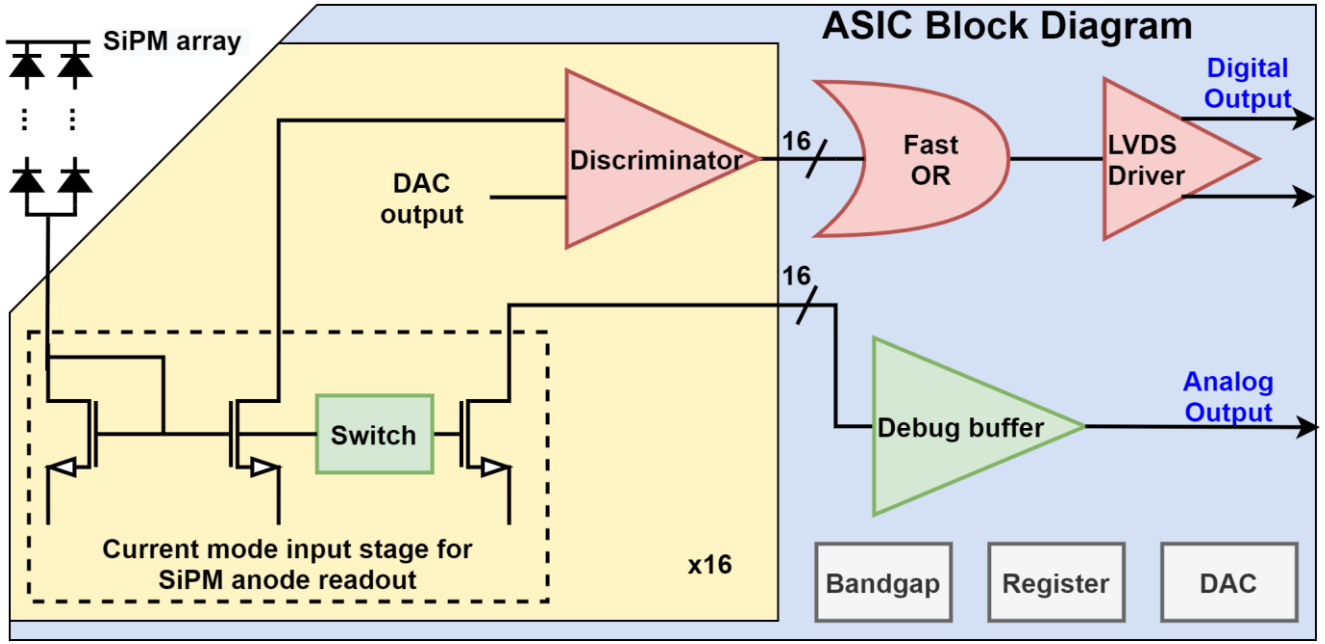
Some SiPM Readout ASICs

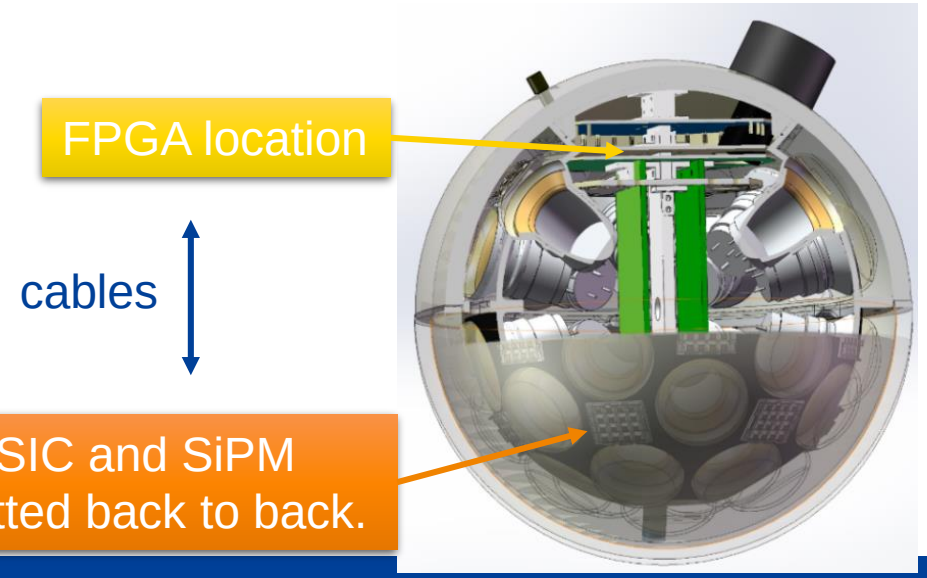
ASIC	SPTR in ps FWHM	Power in mW/ch	Input conditions
NINO	160	27	S13360-3050CS，Vov=10V
HRFlexToT	263	3.5	S13360-3050CS，Vov=4V
FlexToT	390	11	S13360-3050CS，Vov=4V
PETIROC2A	190	6	S13360-3050CS，Vov=7V
STiC3	150	25	S13360-1350CS
TOFPET2	306	8.2	S13361-3050AE-04，Vov=4V
DIET	~94 (3 PE input)	3.3	ARRAYJ-30020-64P，Vov=5V

- These ASICs are not fully applicable to deep-water neutrino telescope experiments.
  - High power consumption: NINO, etc.
  - Readout dead time: PETIROC2A, TOFPET2, etc.
  - Insufficient timing performance: FlexToT, etc.

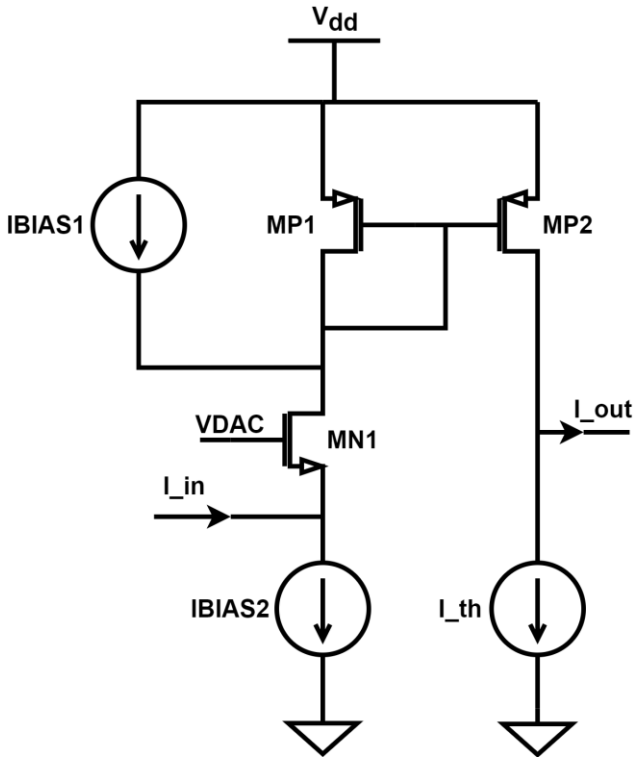
ASIC Concept

- Each input channel is connected to a small SiPM array (e.g. 2p4s).
- SiPM HV tuning
- Core modules are optimized for fast timing.
- Summing: one OR gate combines discriminator outputs.
  - Reduced readout channel number
- CMOS 180 nm technology, VDD = 1.8 V
- This presentation focuses on prototyping and comparing different schemes.
  - Input stage, discriminator, etc.

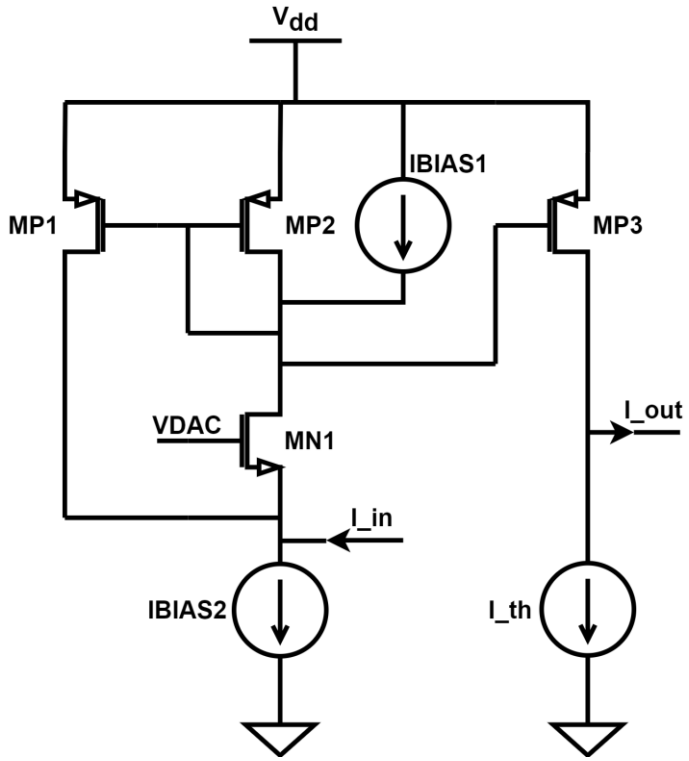




Core Module – Input Stage



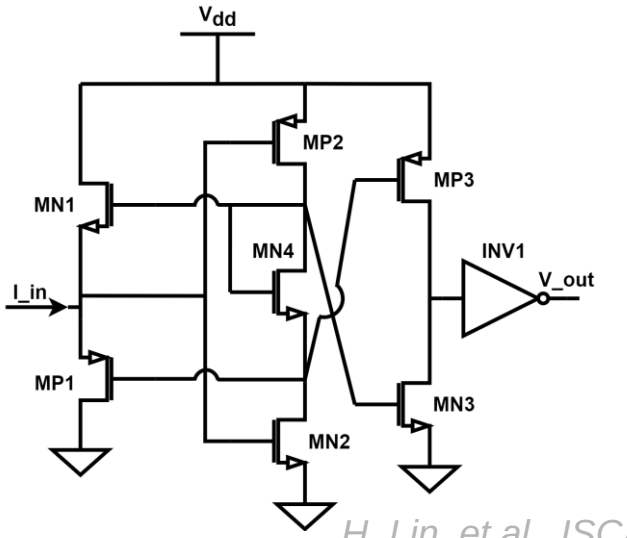
Common gate stage



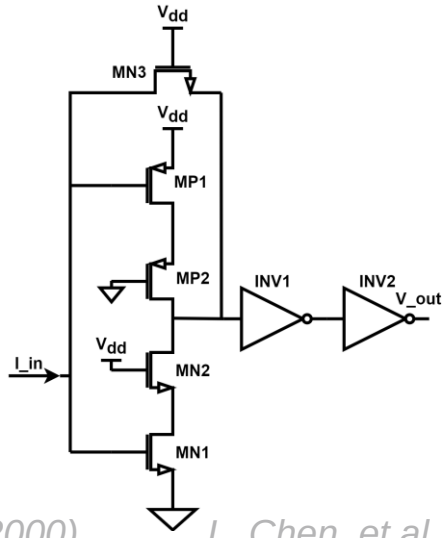
Negative feedback common gate stage

- 2 current buffer architectures are designed.
- CG has better time performance.
- NFBCG has lower input resistance.
  - Alleviate the pile-up effect
- VDAC – SiPM bias voltage tuning
- Power consumption: ~3 mW

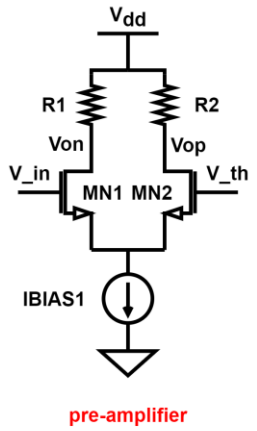
Core Module – Discriminator

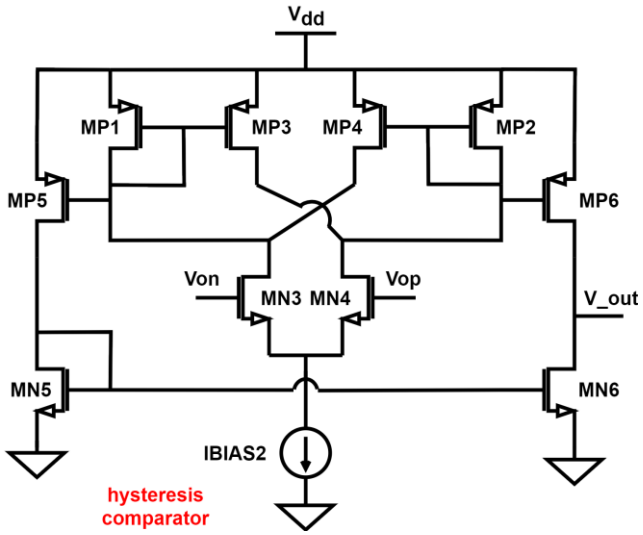


H. Lin, et al., ISCAS (2000)



L. Chen, et al., AICSP (2001)





(a) Current discriminator I

(b) Current discriminator II

(c) Voltage discriminator

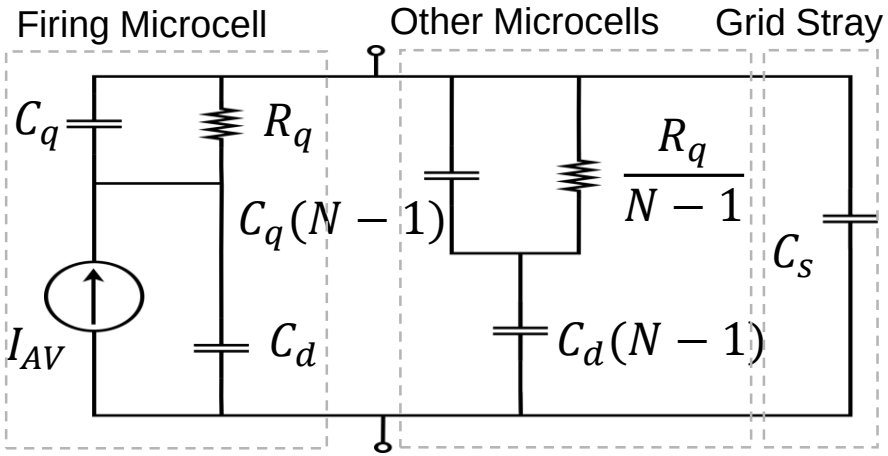
Three-stage pre-amplifier + hysteresis comparator

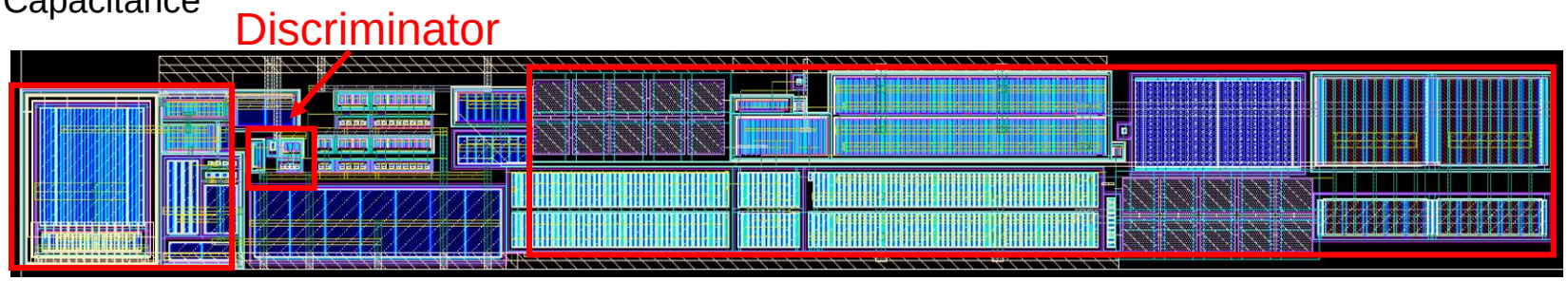
Feature	(a)	(b)	(c)
Input connection	DC coupling		AC coupling
Propagation delay	0.56 ns	0.47 ns	1.9 ns
Static power consumption	0.6 mW	0.4 mW	3.1 mW
Area	187 um^2	336 um^2	6000 um^2

Pre-simulation results @ 27℃, TT corner, Vdd=1.8V

The voltage discriminator is less affected by process-voltage-temperature variations but has higher area and power consumption.

ASIC Performance (simulation results)



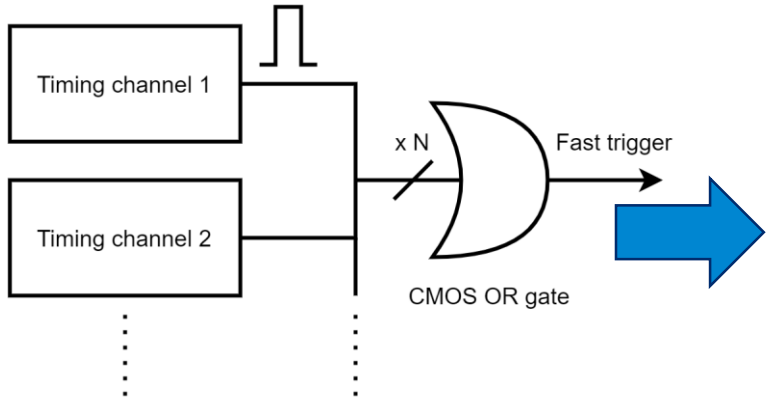


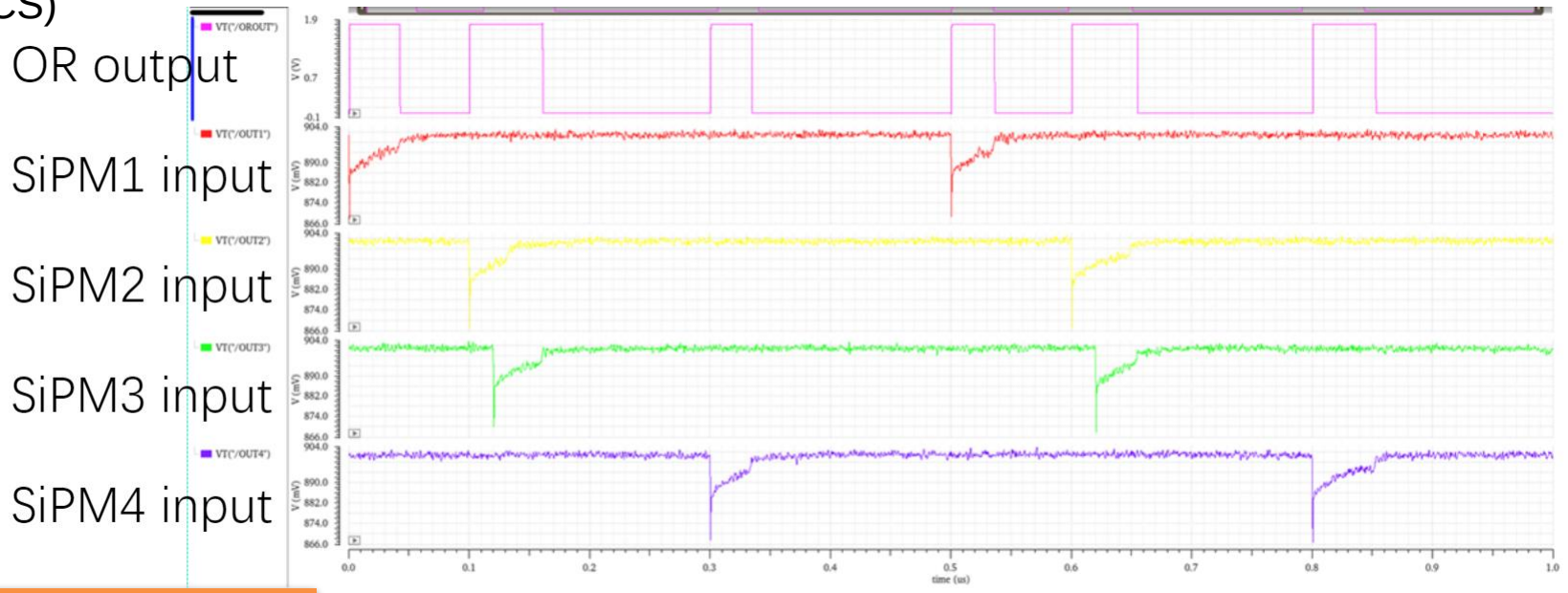
Layout of timing channel with LVDS driver (470um×64um)

Electrical model for the SiPM (S13360-3050CS)

C_{TOT}	C_d	R_q	C_q	C_s	Q	N
320 pF	80 fF	160 kΩ	7 fF	6.8 pF	200 fC	3600

A. Francesco, et al., JINST C03042 (2016)



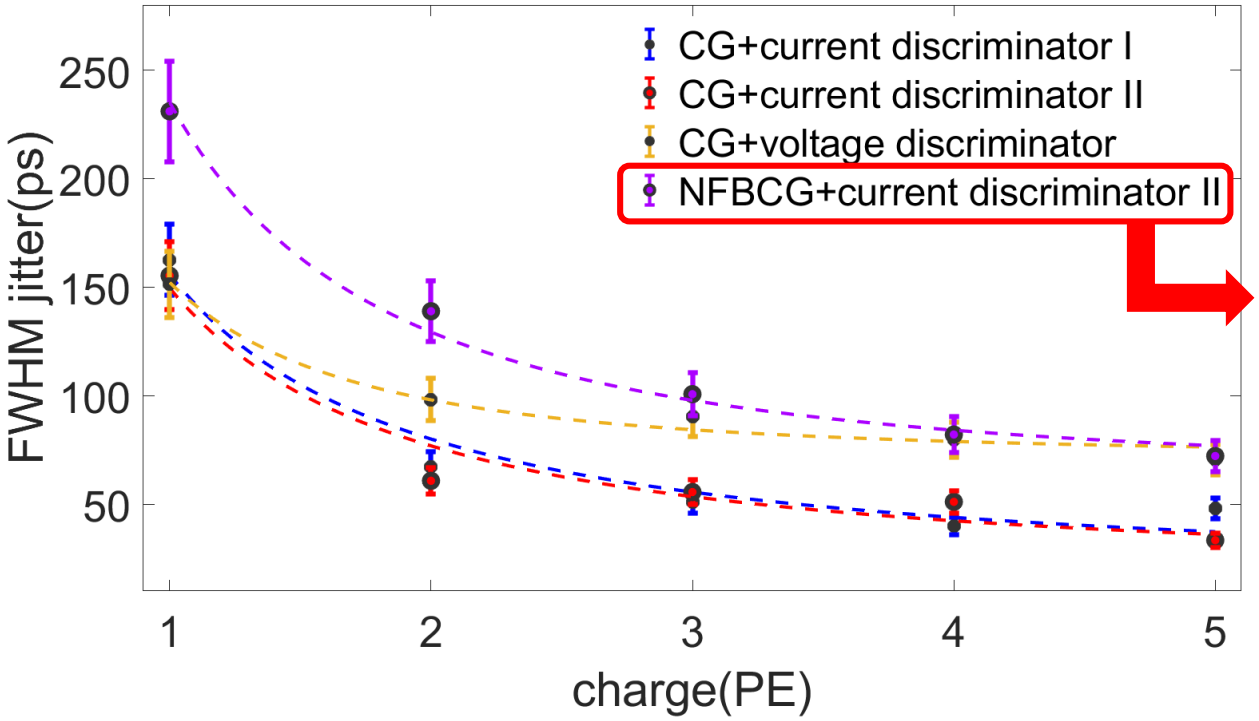


4-channel OR post-simulation waveform

The digital logic has little effect on time measurement.

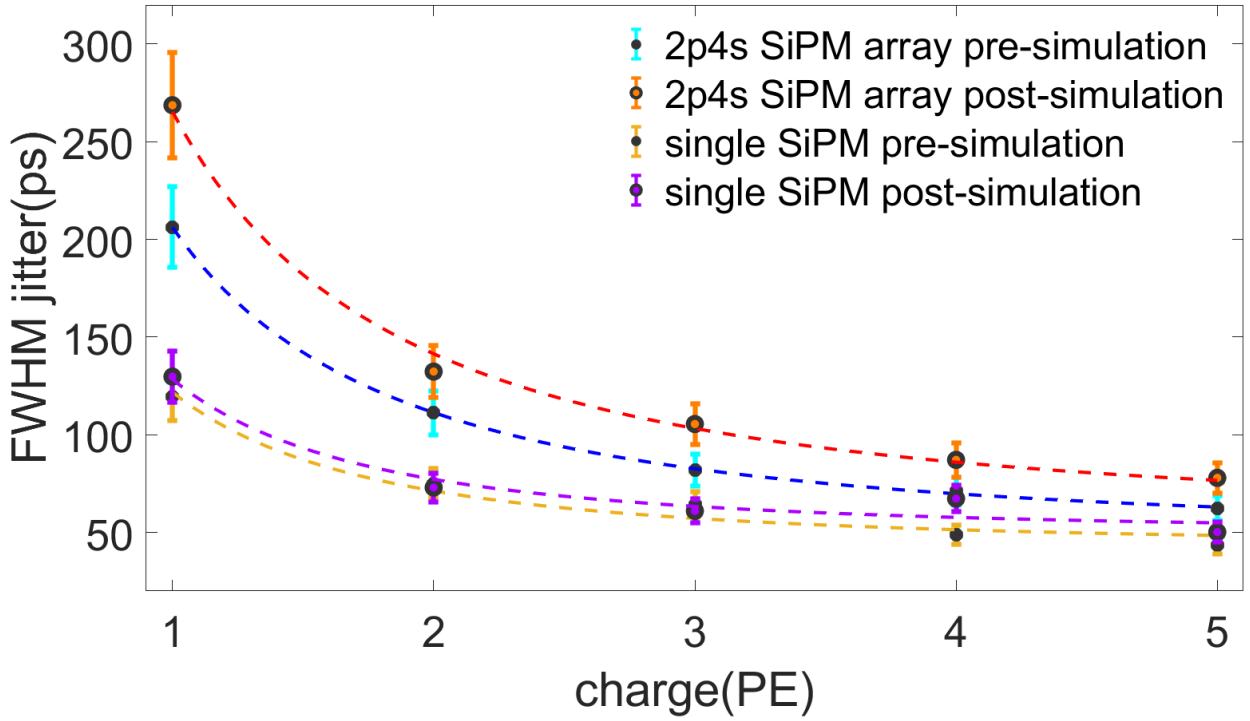
ASIC Performance (simulation results)

Post-simulation results of the timing channels
(TT corner,room temperature)



Input: 200 fC/PE (Vov ~ 2.3V),
single SiPM (S13360-3050CS)

Simulation results of the timing channel
(TT corner,room temperature)



NFBCG + current discriminator II
Input: 360 fC/PE (Vov = 4V)

The timing jitter of single SiPM is **less than**

200 ps FWHM with the single PE signal input.

The timing jitter of SiPM array is **less than**

300 ps FWHM with the single PE signal input.

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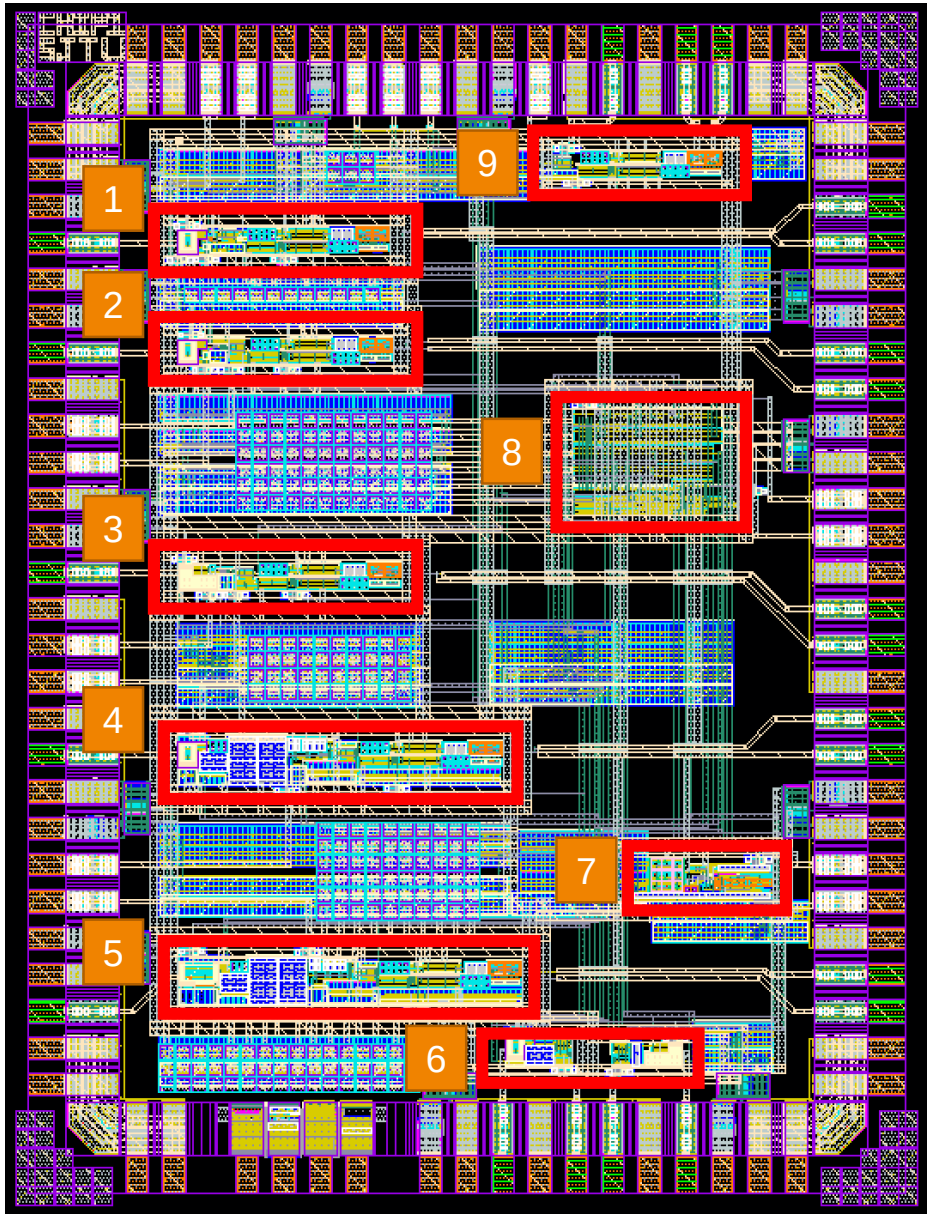
Chip 1 Layout

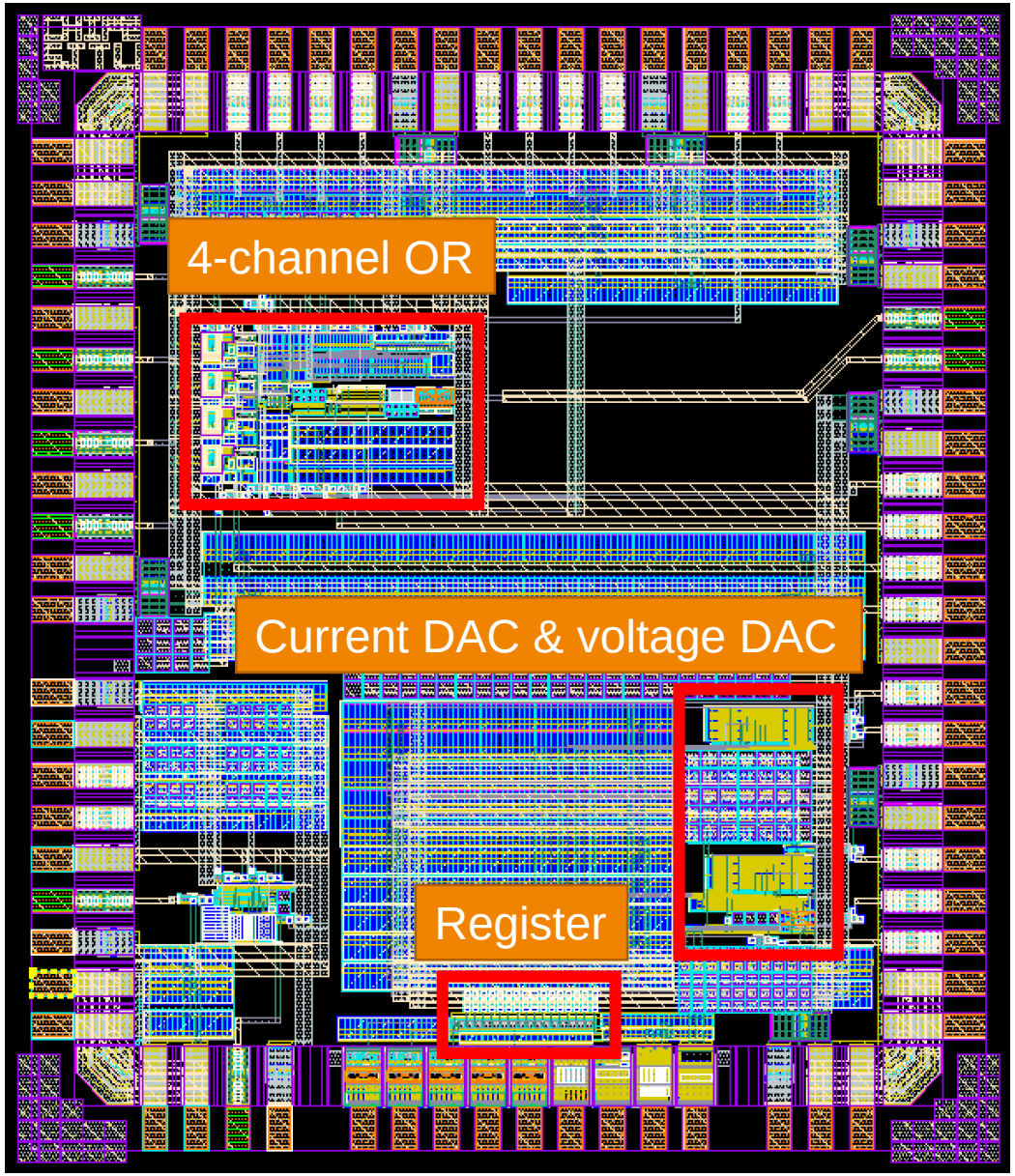
- Chip 1 has 84 pins, $1.92 \times 2.56mm^2$
  - (1) CG + current discriminator I + LVDS driver
  - (2) CG + current discriminator II + LVDS driver
  - (3) NFBCG + current discriminator II + LVDS driver
  - (4) CG + voltage discriminator + LVDS driver
  - (5) CG (ESD modified version) + voltage discriminator + LVDS driver
  - (6) Input stages + debug buffer
  - (7) Bandgap
  - (8) Bias
  - (9) Standalone LVDS driver



Chip 2 Layout

- Chip 2 has 72 pins, $1.84 \times 2.16 mm^2$
  - 4 timing channels + fast OR + LVDS driver
  - 8-bit current DAC
  - 8-bit voltage DAC
  - Registers related to DAC configuration

- 2 ASICs for prototype verification have been designed and will be fabricated in May, 2024.



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Summary

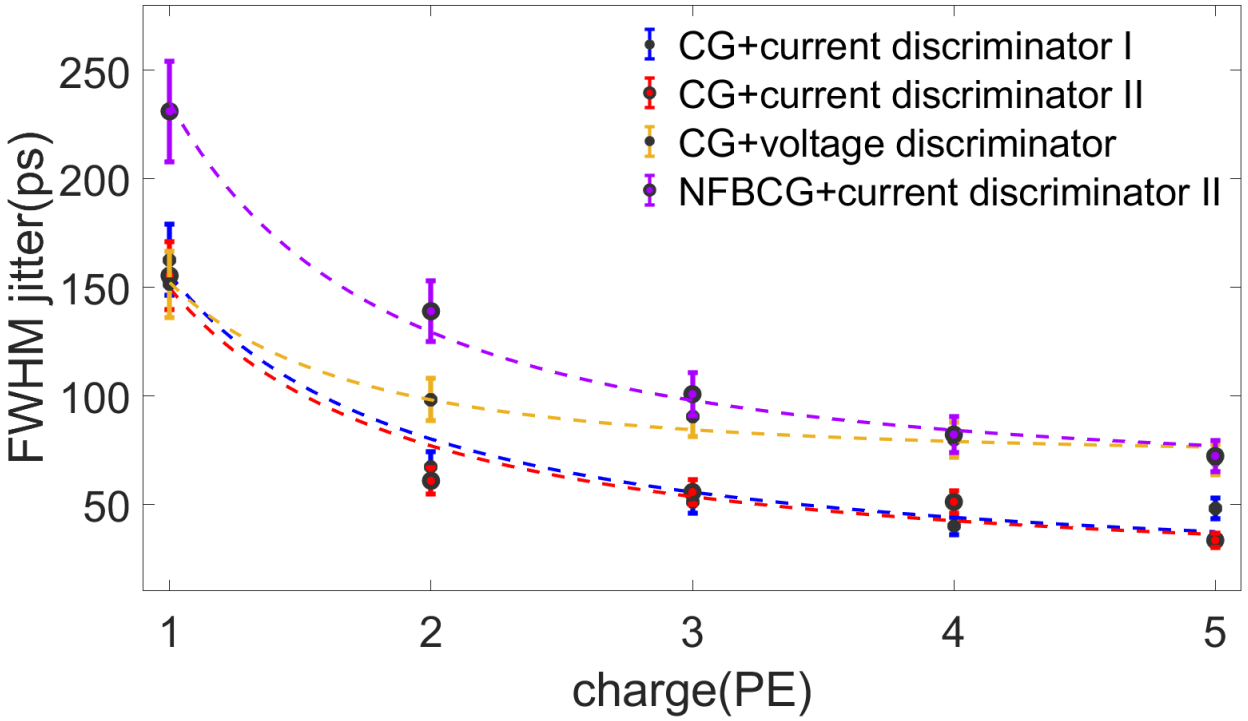
- TRIDENT is a next-generation neutrino telescope planned to be constructed in the South China Sea.
- A fast timing ASIC for SiPM array readout is under development.
- The first version of the prototype ASIC has been designed and will be fabricated in May, 2024.
- Post-simulations show that the timing jitter is less than 200 ps FWHM @ Single PE input, with power consumption < 10 mW/channel.

Thanks !

Backup

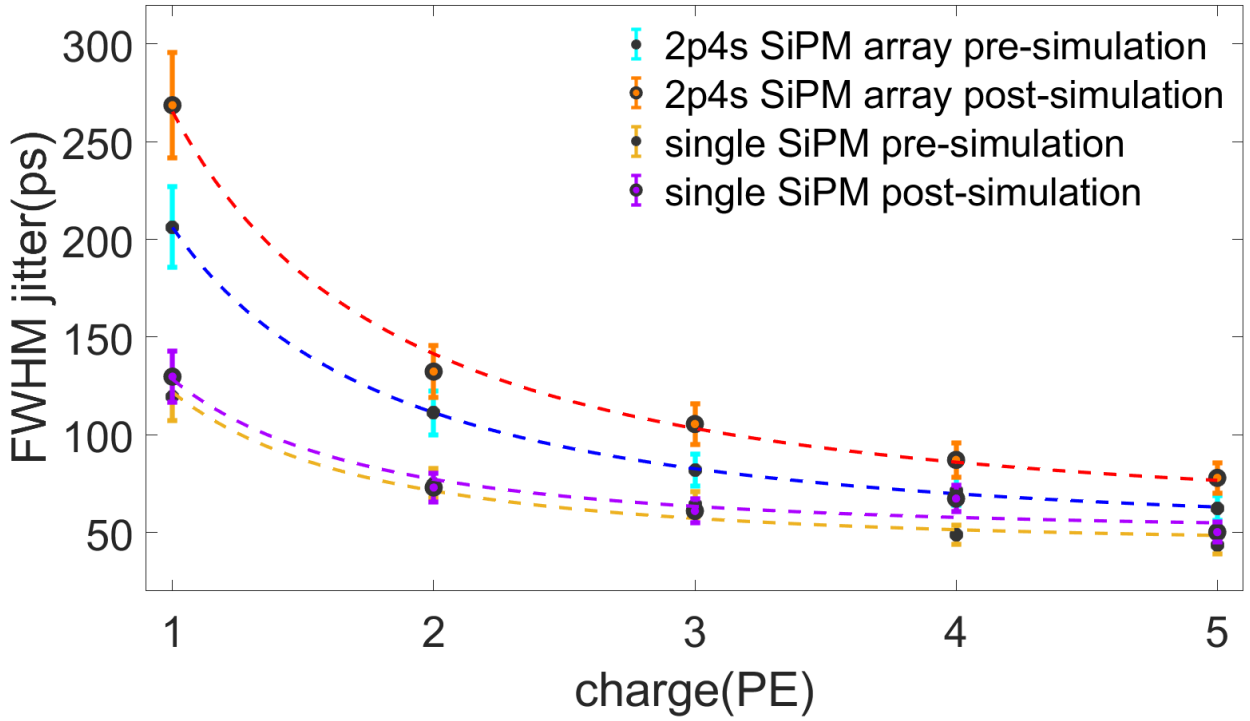
ASIC Performance (simulation results)

Post-simulation results of the timing channels
(TT corner,room temperature)



Input: 200 fC/PE, single SiPM (S13360-3050CS)

Simulation results of the timing channel
(TT corner,room temperature)



NFBCG + current discriminator II
Input: 360 fC/PE (Vov = 4V)

2p4s SiPM array post-simulation input: 360 fC (SPE)	CG + current discriminator I	CG + current discriminator II	CG + voltage discriminator
FWHM jitter (ps)	186	264	281