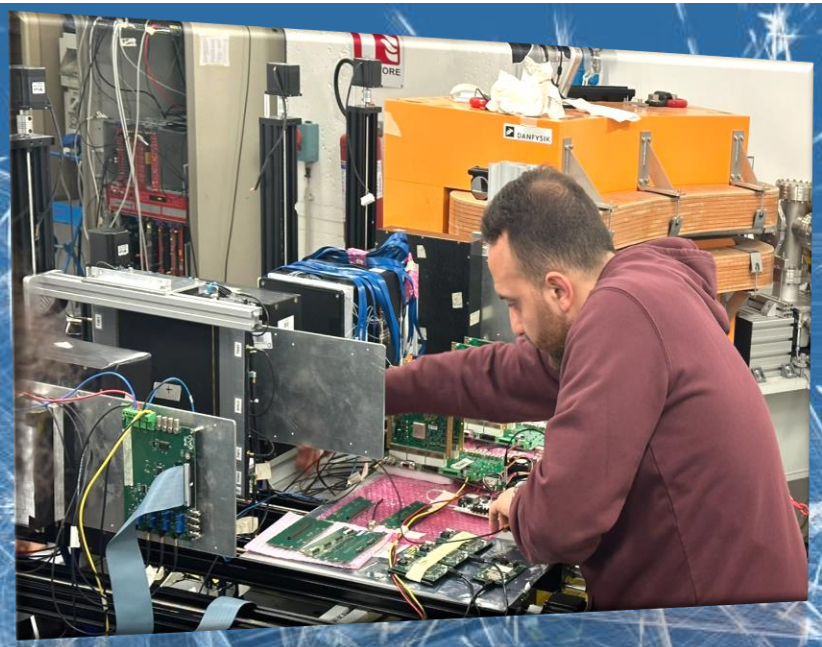
SCI-COMPILER

Simplified Firmware Development for Open FPGA Platforms in DAQ Systems using Sci-Compiler



A. Abba
F. Caponio
V. Arosio
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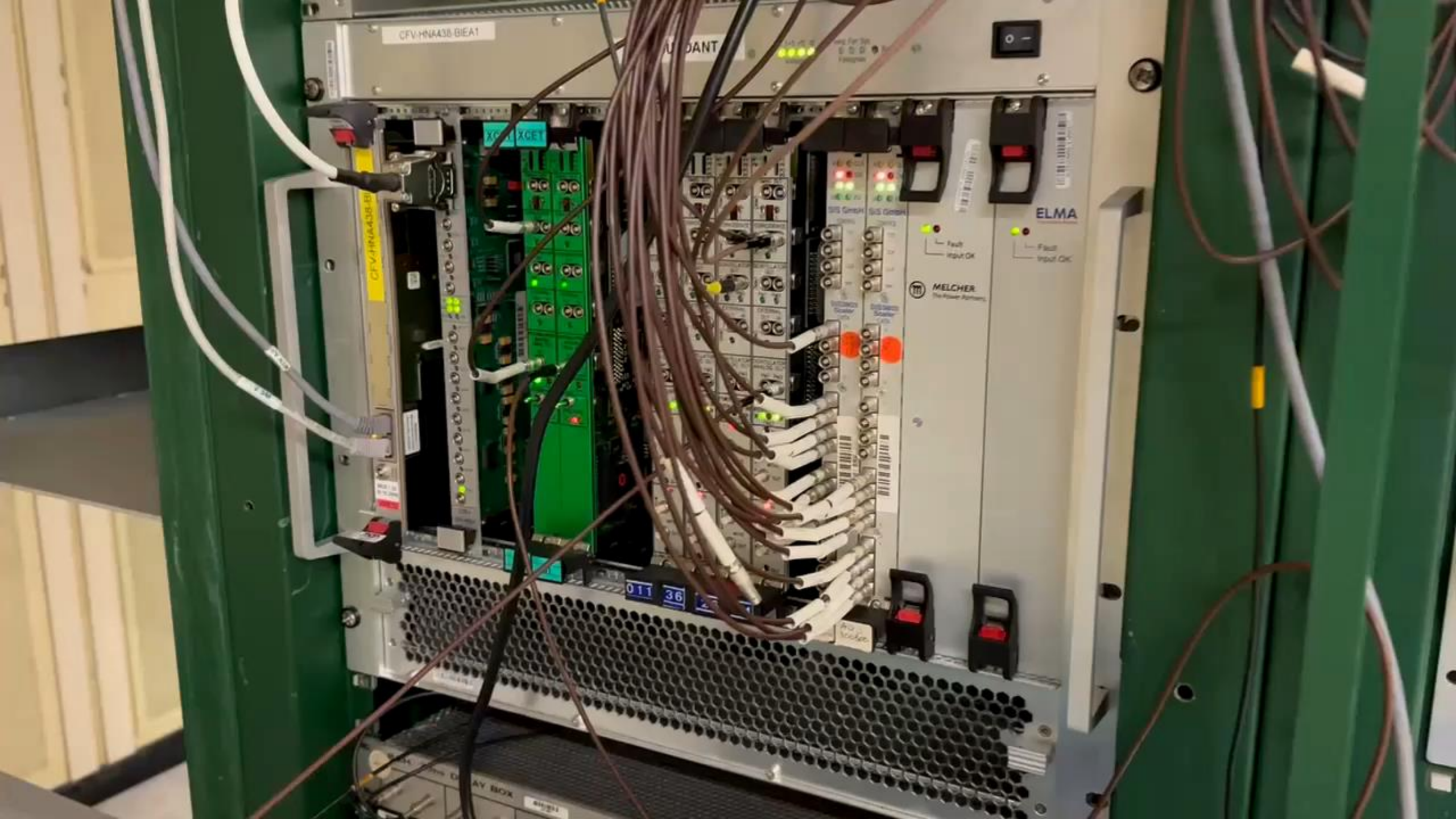
M. Petruzzo
Y. Venturini
A. Cusimano
L. Ferrentino
M. Venaruzzo

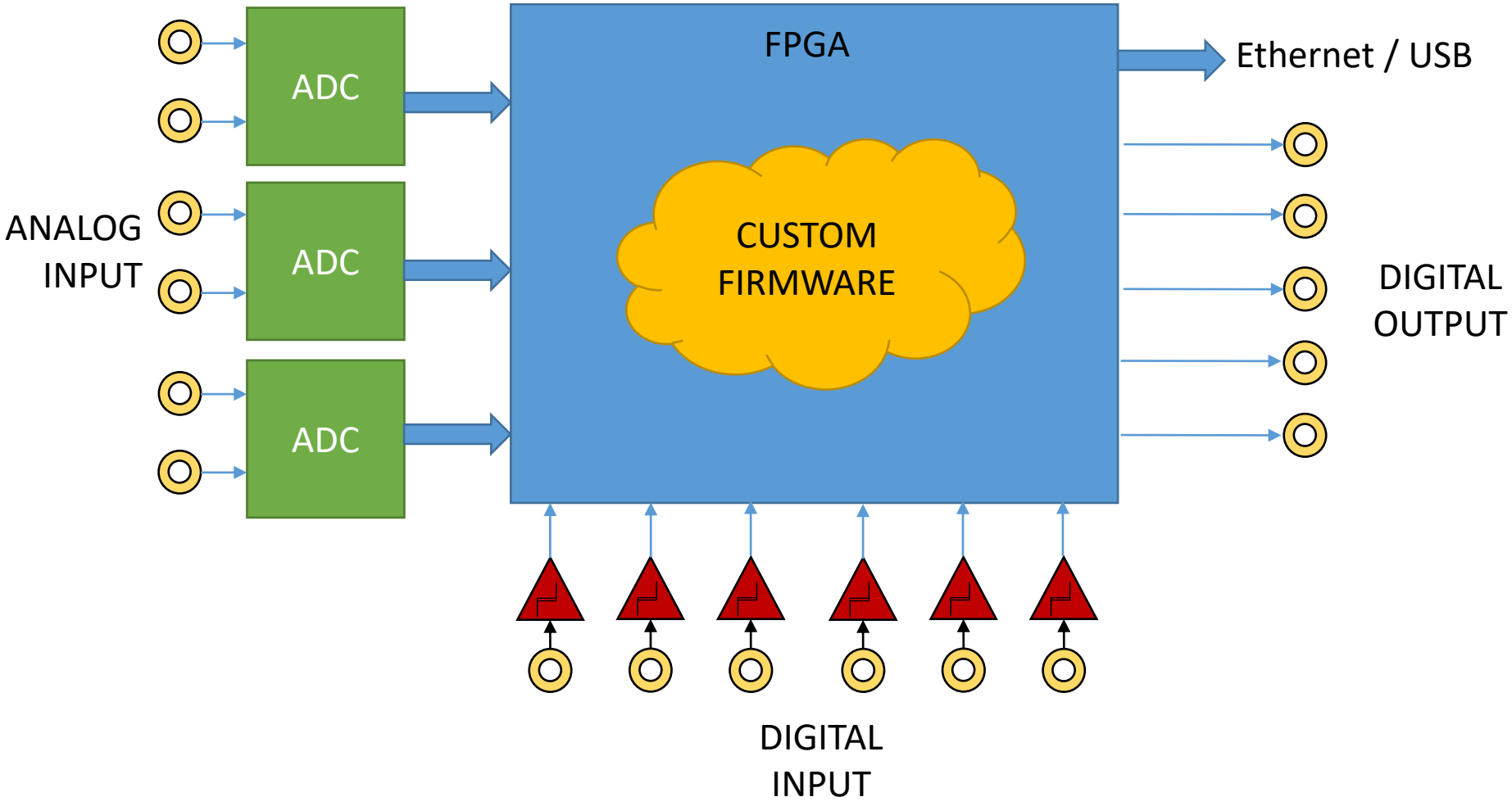
designed for CAEN digital acquisition systems

CAEN
Tools for Discovery

Nuclear Instruments

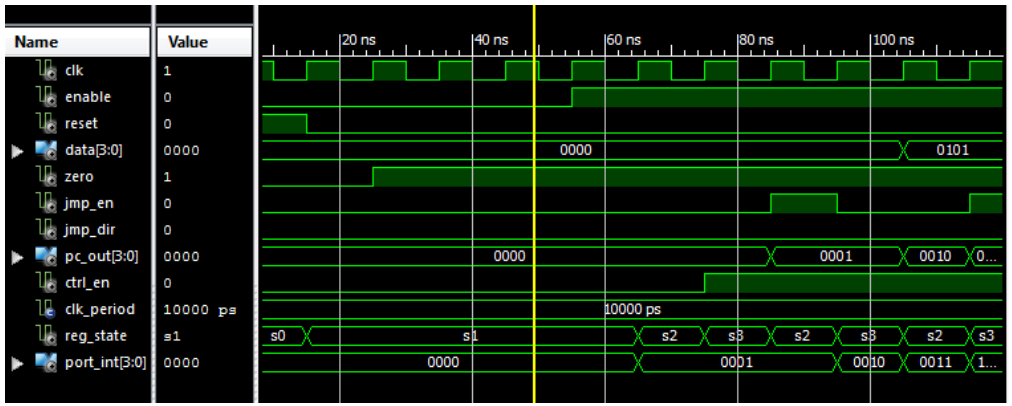

CFV-HNA438 BIEA1
XCET
ELMA
Fault
Input OK
MELCHER

Replace modular Electronics with FPGA



Developing in VHDL/Verilog is hard and time consuming.

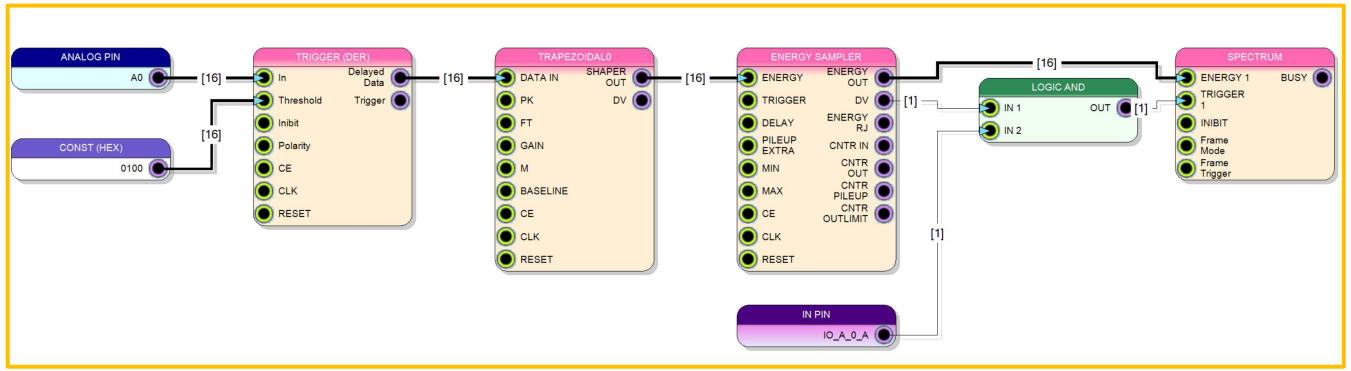
```
18  architecture Counter_Arch of AAC2M2P1 is begin
19
20      count_proc : process(CP,SR,PE,CEP,CET) begin
21
22          if (SR='0') then Q <= "0000";
23
24          elsif rising_edge(CP) then
25
26              if PE = '0' then Q <= P; --load
27
28              elsif CET = '1' and CEP = '1' then Q <= Q+1; -- count
29
30              end if;
31
32              if CET = '1' and Q = "1111" then TC <= '1'; -- Terminal count
33
34              else TC <= '0';
35
36
37              end if;
38
39          end if;
40
41      end process count_proc;
```

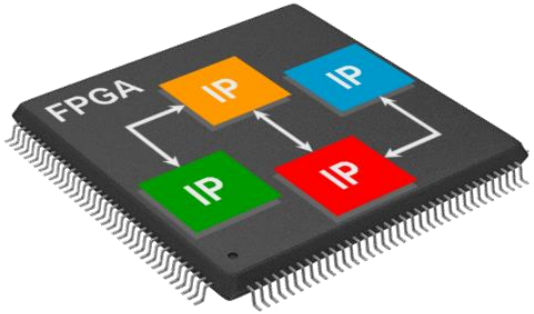


VHDL or Verilog programming skills

CAEN Solution: OpenFPGA digitizers + SciCompiler firmware generator

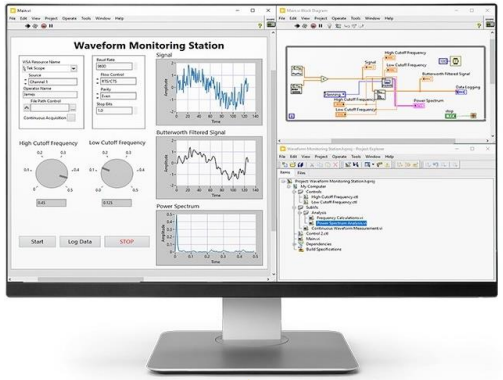
OpenFPGA Digitizers





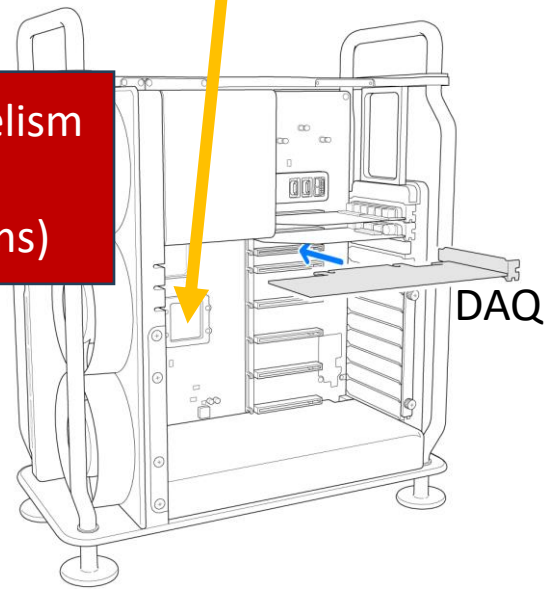
SCI-COMPILER

Sci-Compiler generates firmware



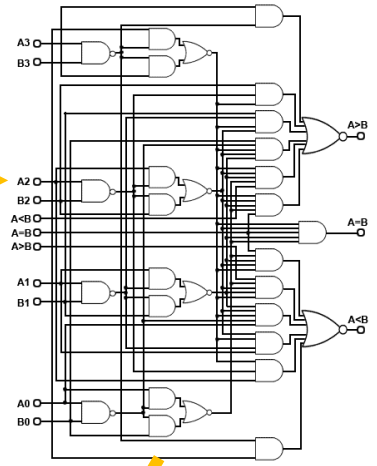
Limited parallelism

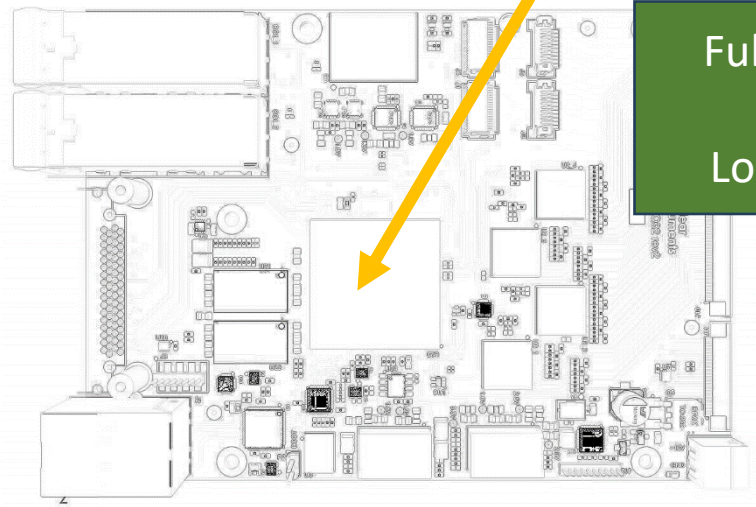
High delay (ms)



DAQ

Other VPL (like Labview) generate code for CPU running inside DAQ computer



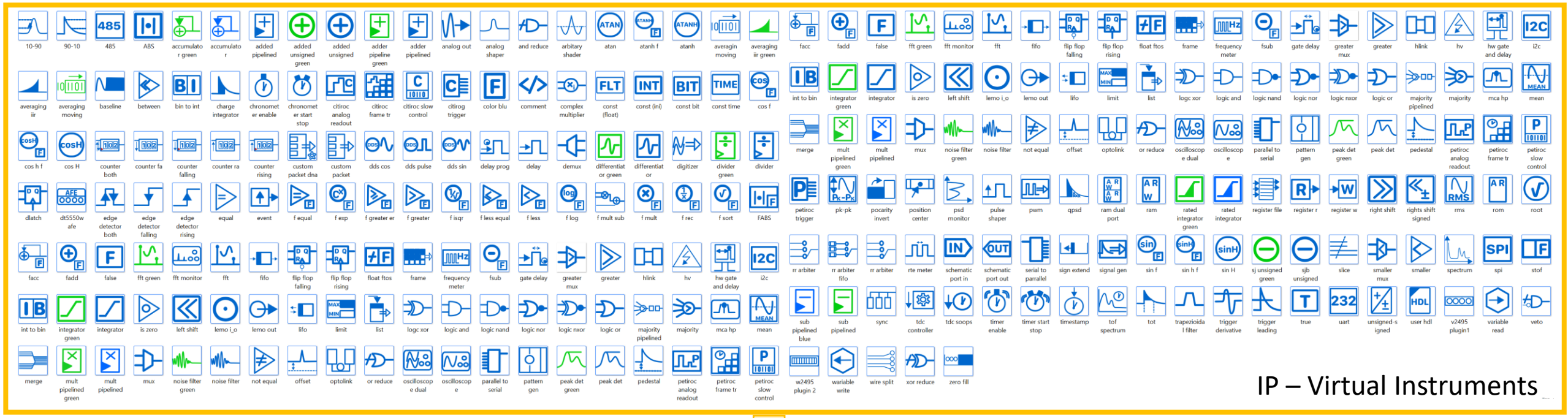


Full parallelism

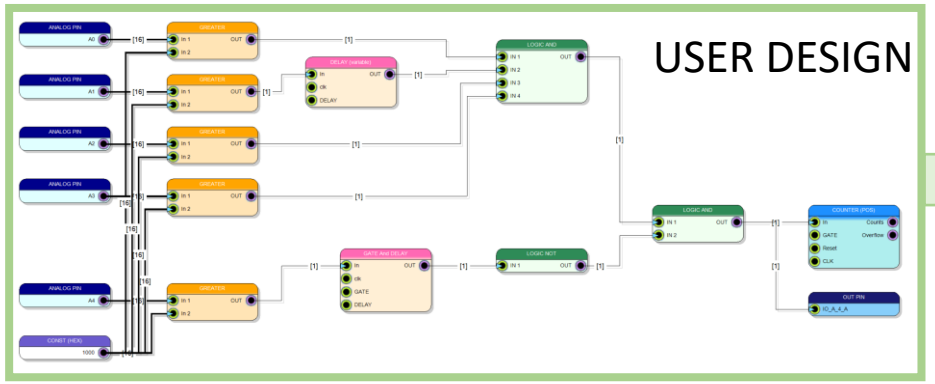
Low delay (ns)

Generate FPGA firmware that «runs» directly inside the DAQ

SciCompiler: ip integrator software



IP – Virtual Instruments



USER DESIGN

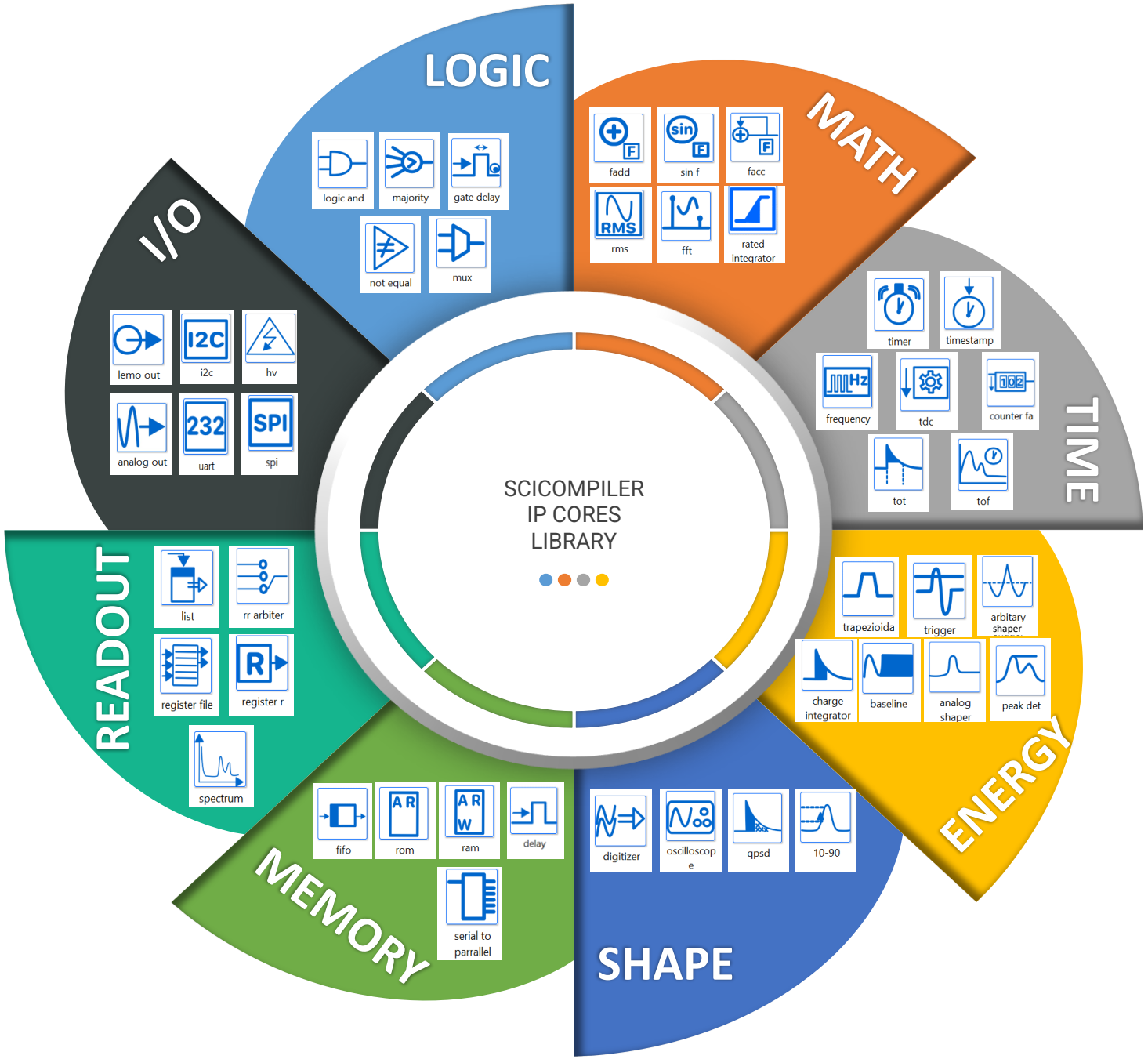
BUILDER ENGINE

```
architecture Counter_Arch of AAC2M2P1 is begin

    count_proc : process(CP,SR,PE,CEP,CET) begin

        if (SR='0') then Q <= "0000";

        elsif rising_edge(CP) then

            if PE = '0' then Q <= P; --Load

            elsif CET = '1' and CEP = '1' then Q <= Q+1; -- count

            end if;

            if CET = '1' and Q = "1111" then TC <= '1'; -- Terminal count

            else TC <= '0';

            end if;

        end if;

    end process count_proc;
```

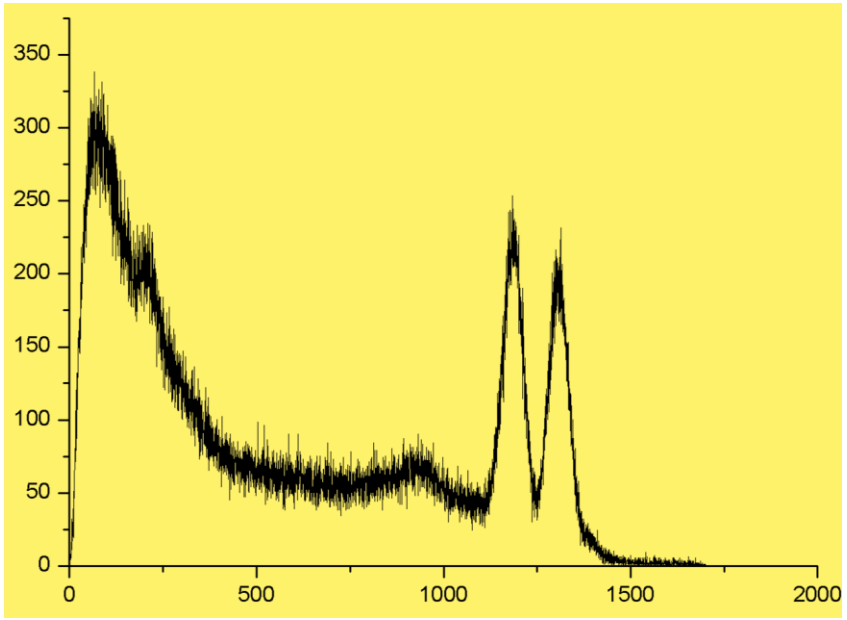
Nuclear Instruments

CAEN Tools for Discovery

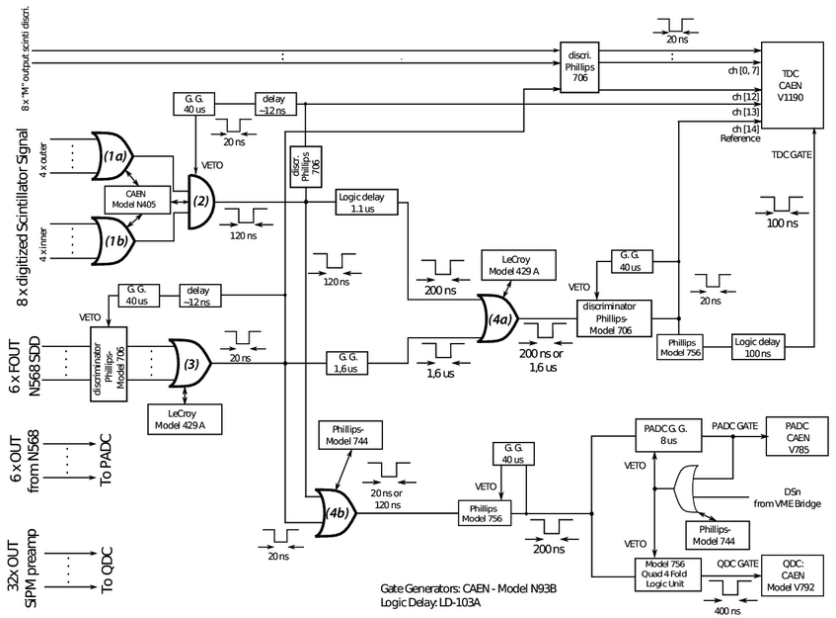
www.sci-compiler.com


LOGIC
logic and
majority
gate delay
not equal
mux
MATH
fadd
sin f
facc
rms
fft
rated integrator
TIME
timer
timestamp
frequency
tdc
counter fa
tot
tof
ENERGY
trapezioida
trigger
arbitary shaper
charge integrator
baseline
analog shaper
peak det
SHAPE
digitizer
oscilloscop e
qpsd
10-90
MEMORY
fifo
rom
ram
delay
serial to parrallel
READOUT
list
rr arbiter
register file
register r
spectrum
I/O
lemo out
i2c
hv
analog out
uart
spi
SCICOMPILER
IP CORES
LIBRARY

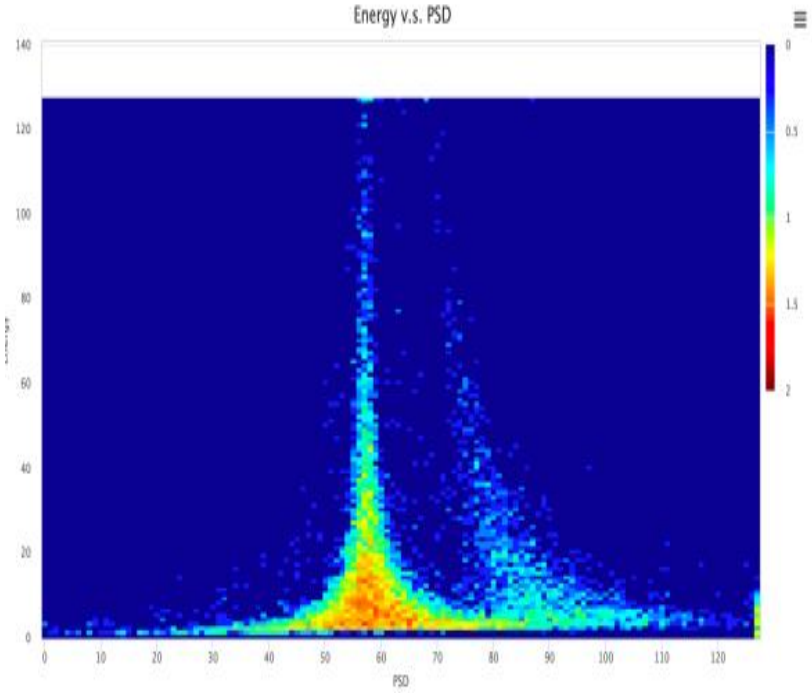
Examples of what you can do with Sci-Compiler



PHA with trapezoidal filter, charge integration, peak detector, or user custom algorithm

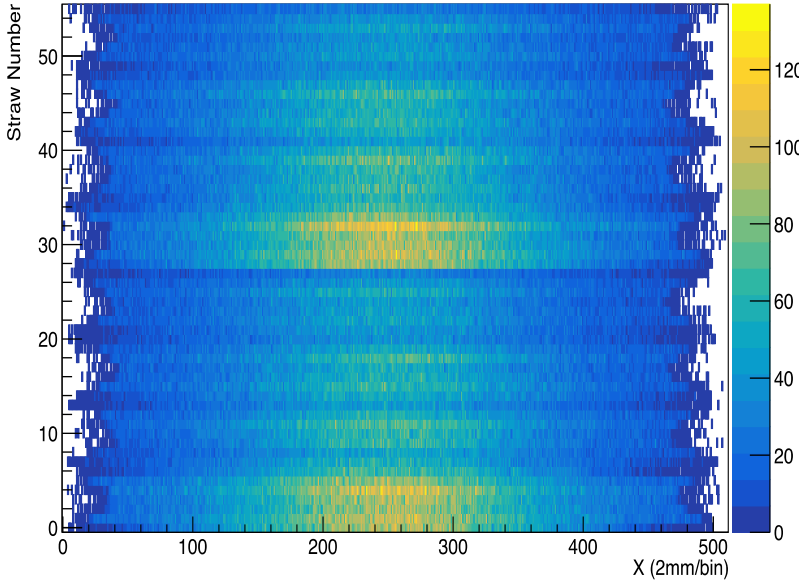


Convert any complex trigger logic into a single board, diagram based design

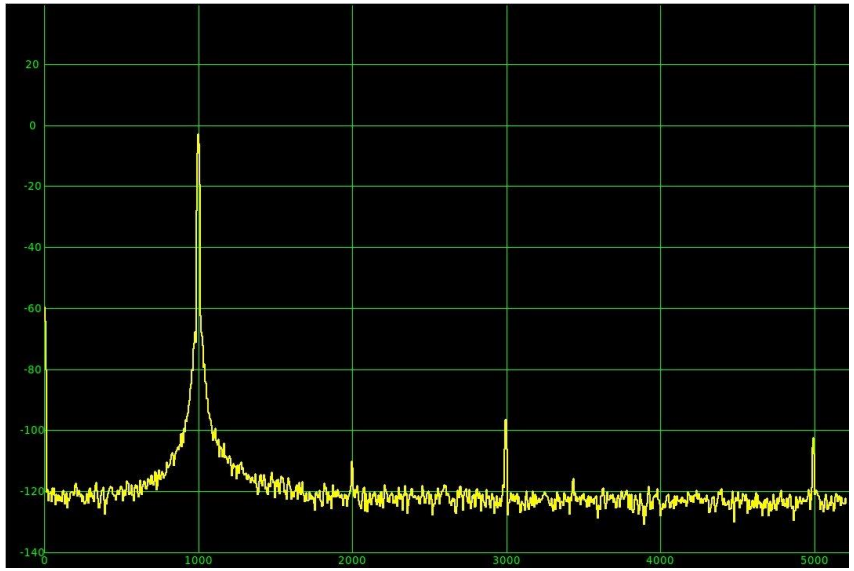


Realtime calculation of PSD using several algorithms operating on both exponential shape (for scintillators) or rise time (for He3)

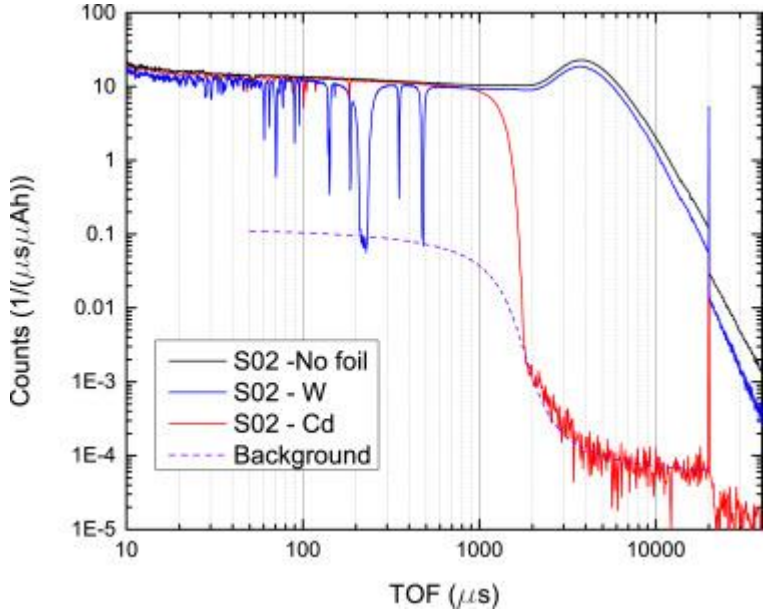
Examples of what you can do with Sci-Compiler



Reconstruction of interaction point in position sense detector

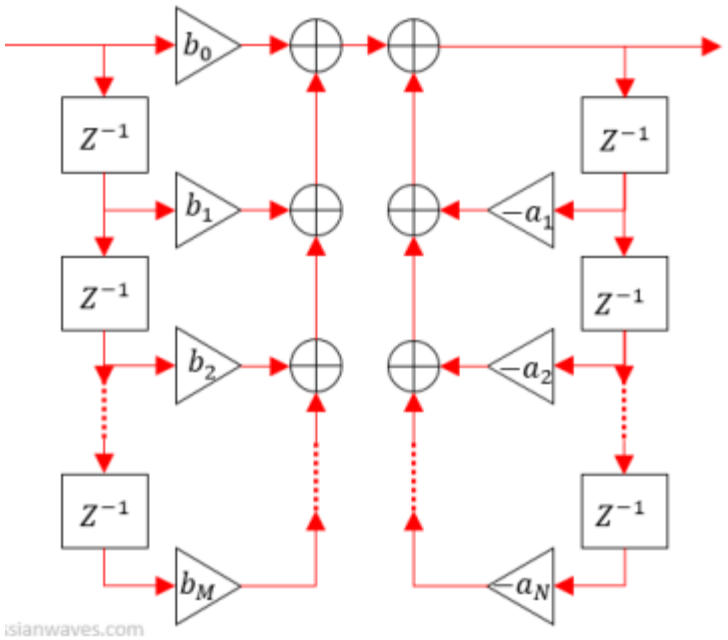


Realtime calculation of FFT with no deadtime (can be used to implement trigger)

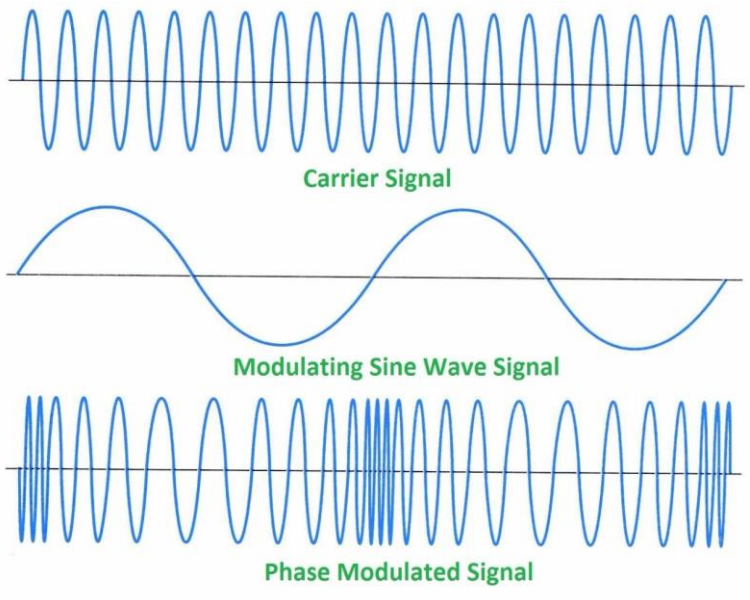


Time of flight spectroscopy, high resolution multichannel TDC

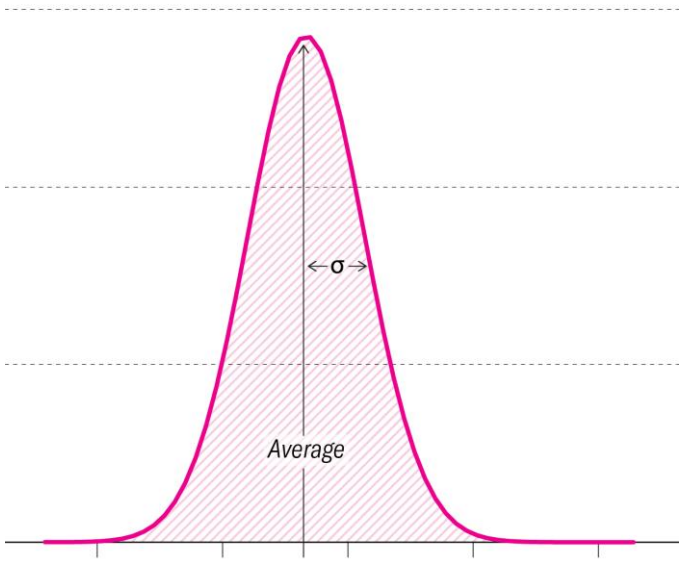
Examples of what you can do with Sci-Compiler



Implementation of any custom filter, digital conversion of analog filter, advanced fixed and floating point math

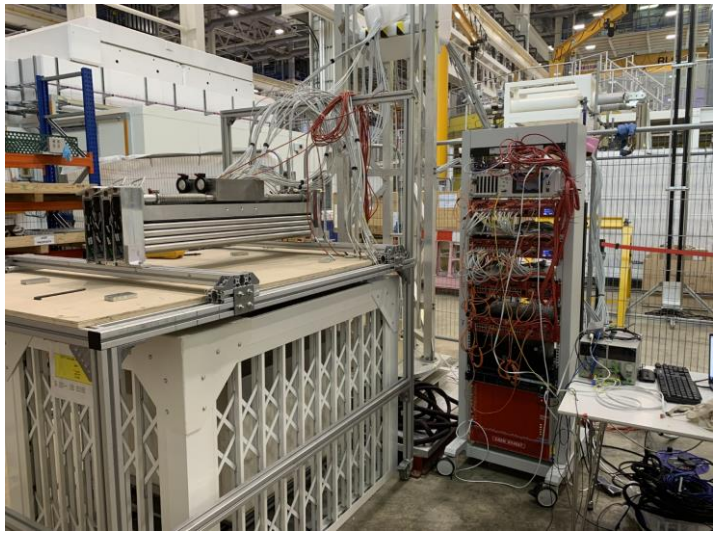


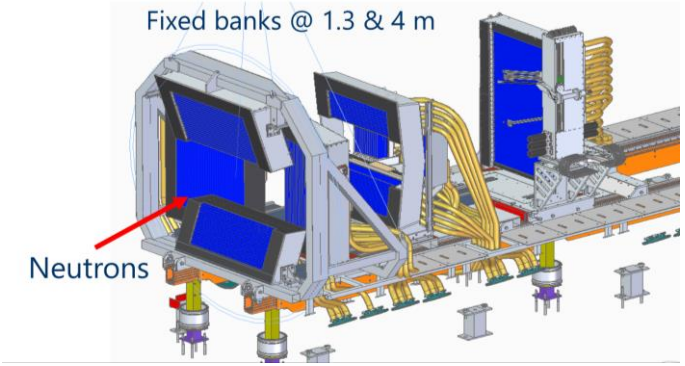
Analog signal generation with DDS, Cordic or LUT based

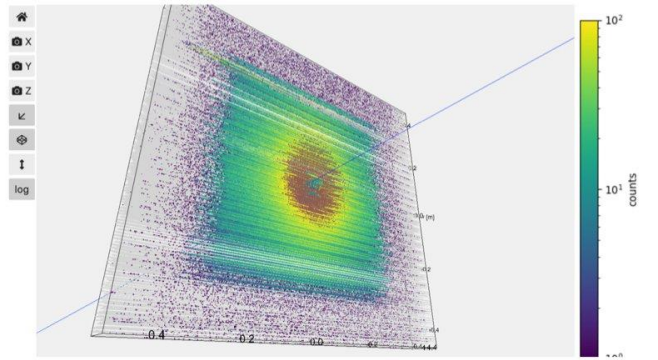


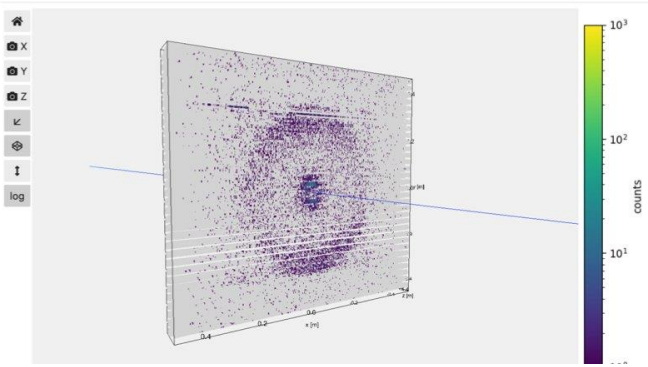
Realtime calculation of signal statistical parameter

(ESS) LOKI, BIFROST, MIRACLES, CSPEC, VESPA more than 10K channels





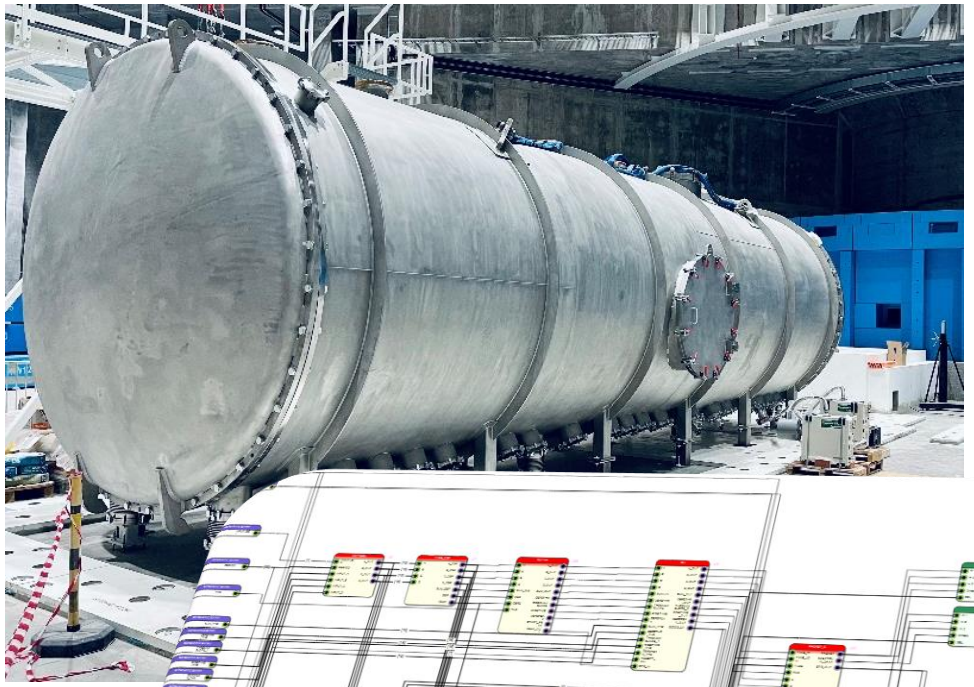


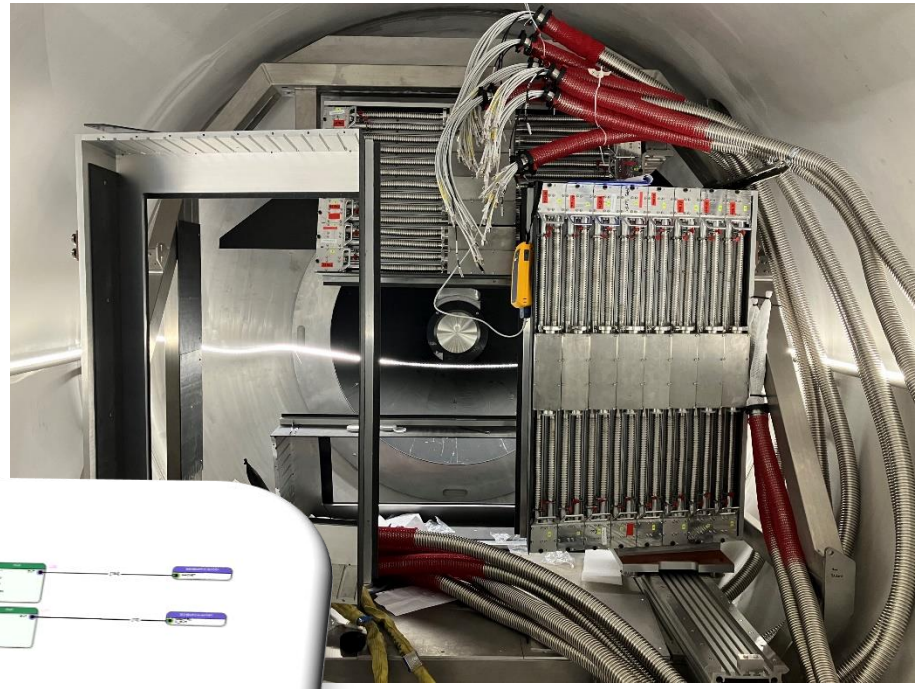


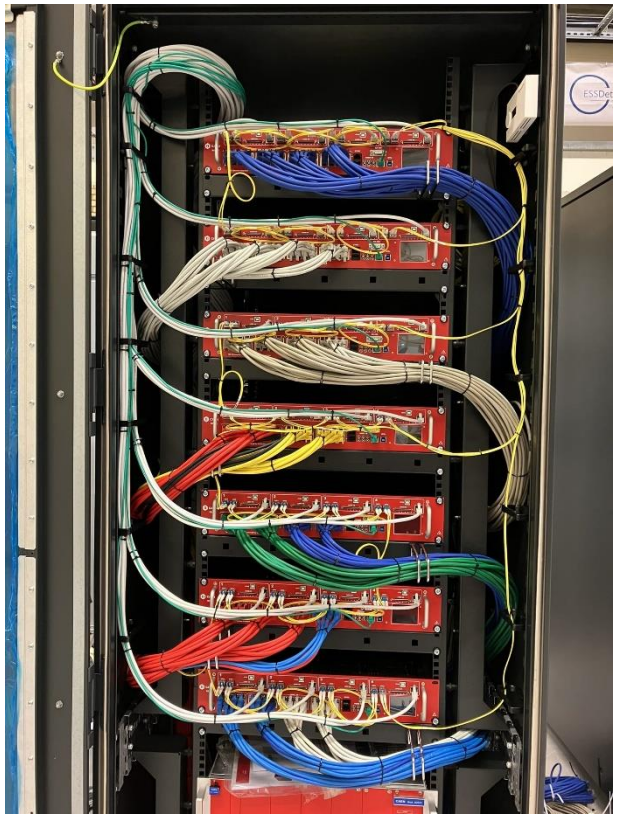
Real time processing from 5000 channels to readout straw tubes for LOKI experiment @ ESS.
ESS BIFROST, MIRACLES and VESPA, CSPEC are using R5560 and SciCompiler for readout

Davide Raspino - ISIS

(ESS) LOKI, BIFROST, MIRACLES, CSPEC, VESPA more than 10K channels







EUROPEAN SPALLATION SOURCE

Science and Technology Facilities Council

NEUTRONS FOR SOCIETY

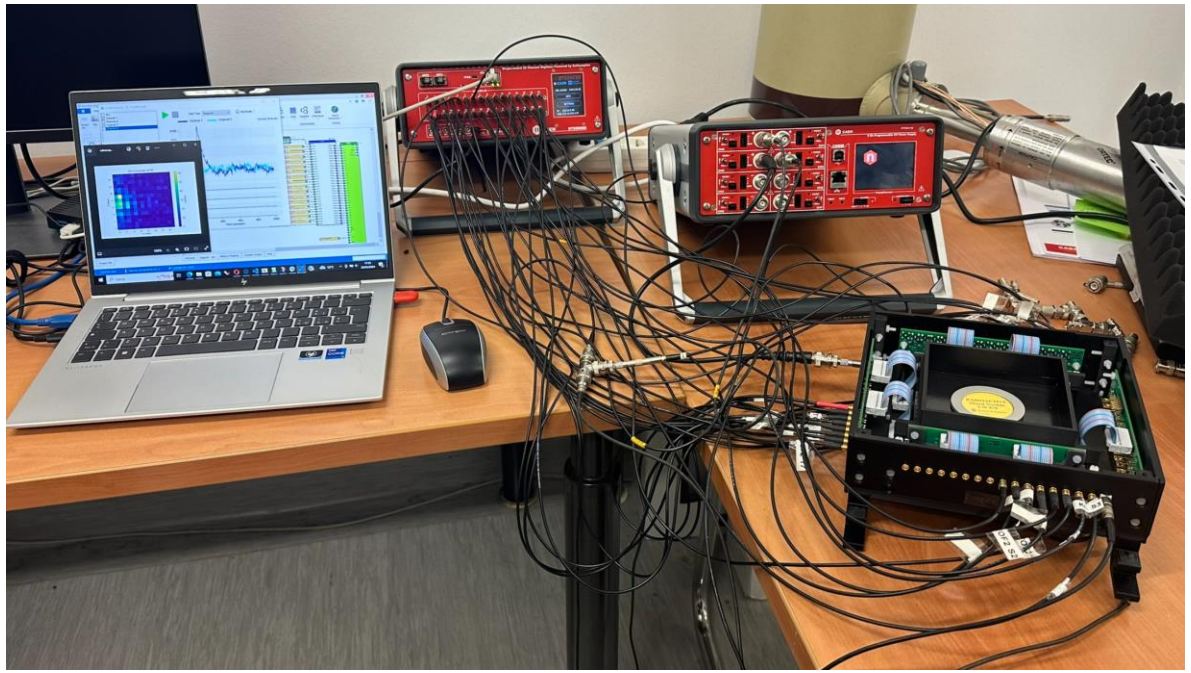
ESS bilbao

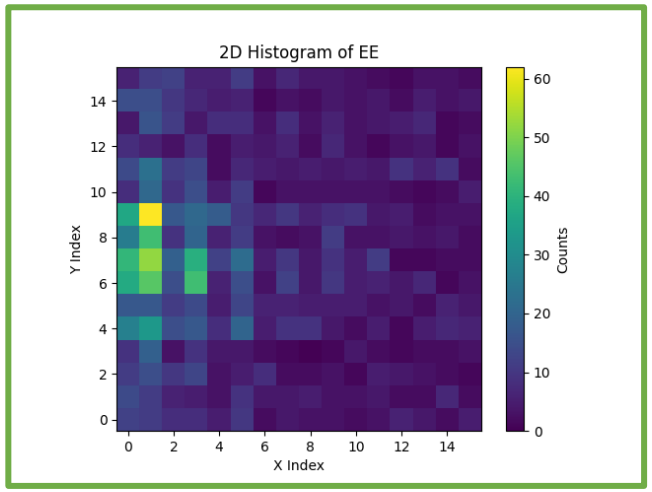
Years of ISIS Neutron and Muon Source

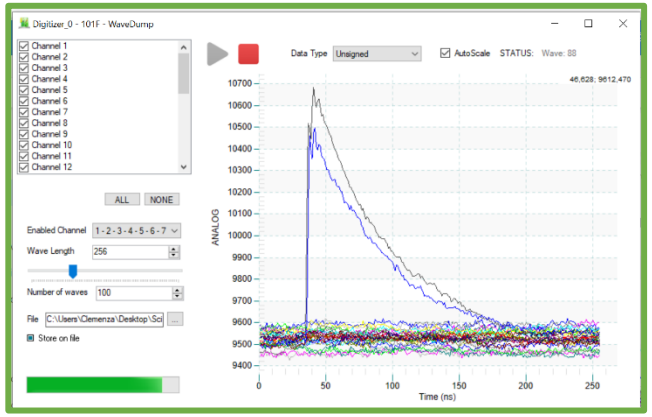
(UNIMIB) Fiber Hodoscope CHNET MAXI

- 32X + 32Y scintillating fiber
- Readout using DT5560 digitizer, with PHA and coincidence trigger
- Real time image reconstruction using SciSDK and Python
- Will be installed and test on CRONOS ISIS detector in May 2024

Massimiliano Clemenza - UNIMIB



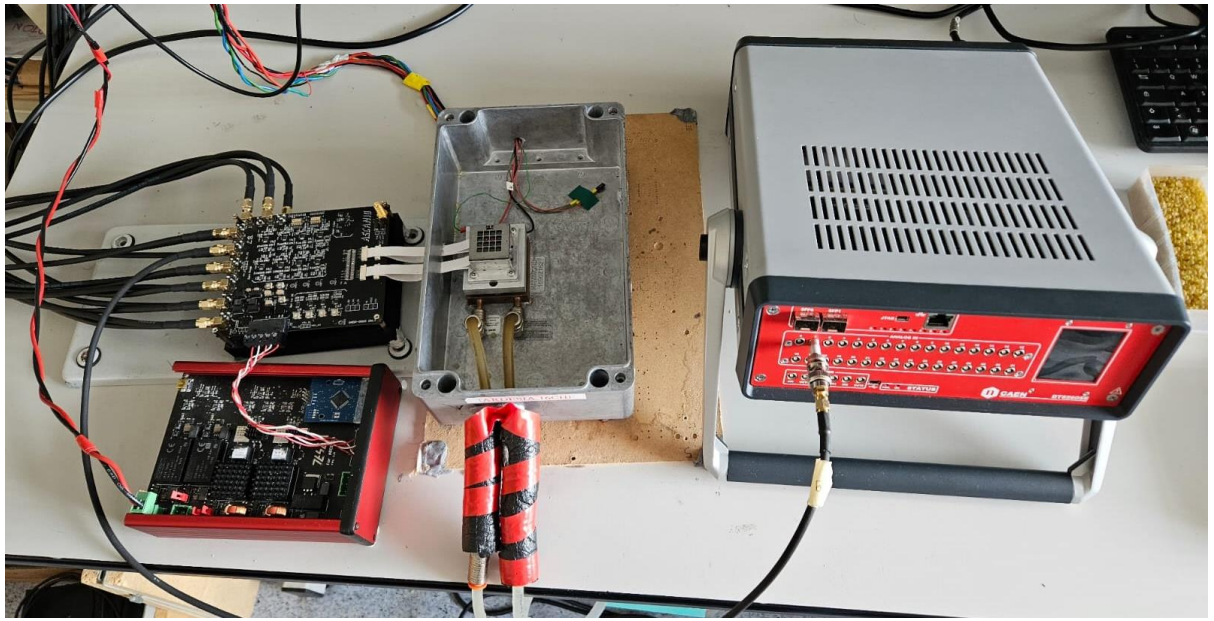


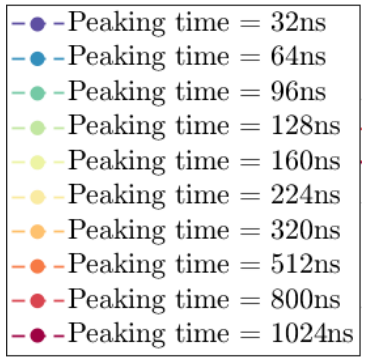


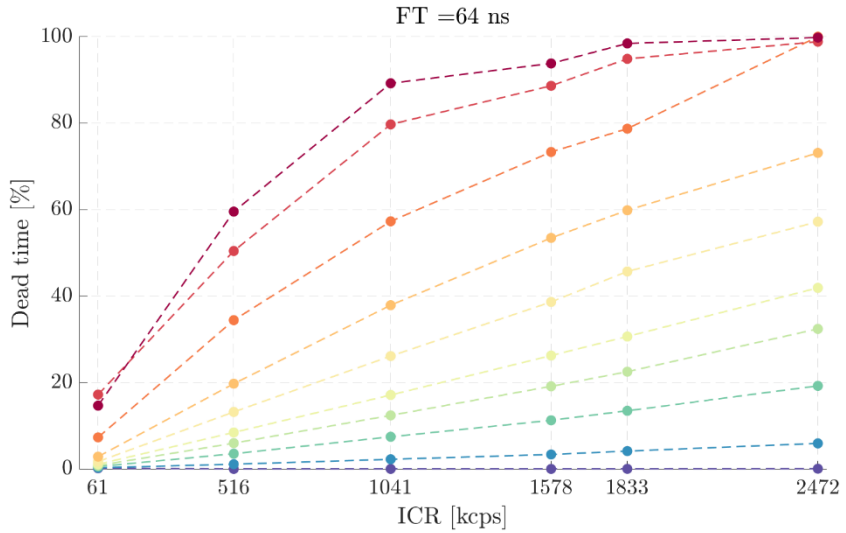
INFN · Università degli Studi di Milano Bicocca · uniss Università degli Studi di Sassari · Università di Pavia · 40 Years of ISIS Neutron and Muon Source

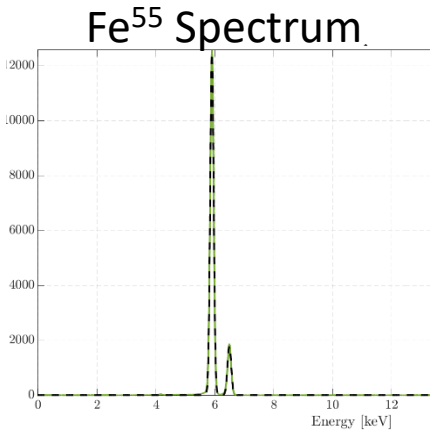
(POLIMI) Ardesia 16 channels SDD read-out

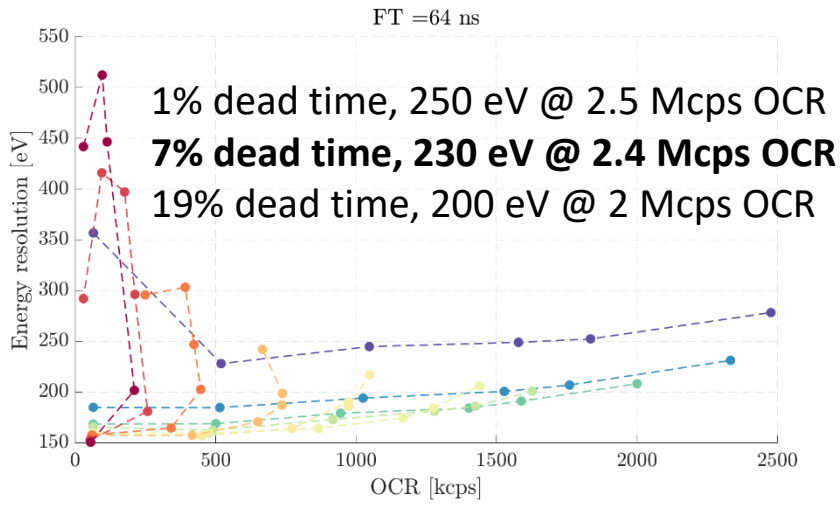
- SDD matrix 4x4 detector
- Front end: 4 channel Cube ASIC designed at PoliMI
- Achieving high throughput with minimal dead time
- Good energy resolution.











1% dead time, 250 eV @ 2.5 Mcps OCR

7% dead time, 230 eV @ 2.4 Mcps OCR

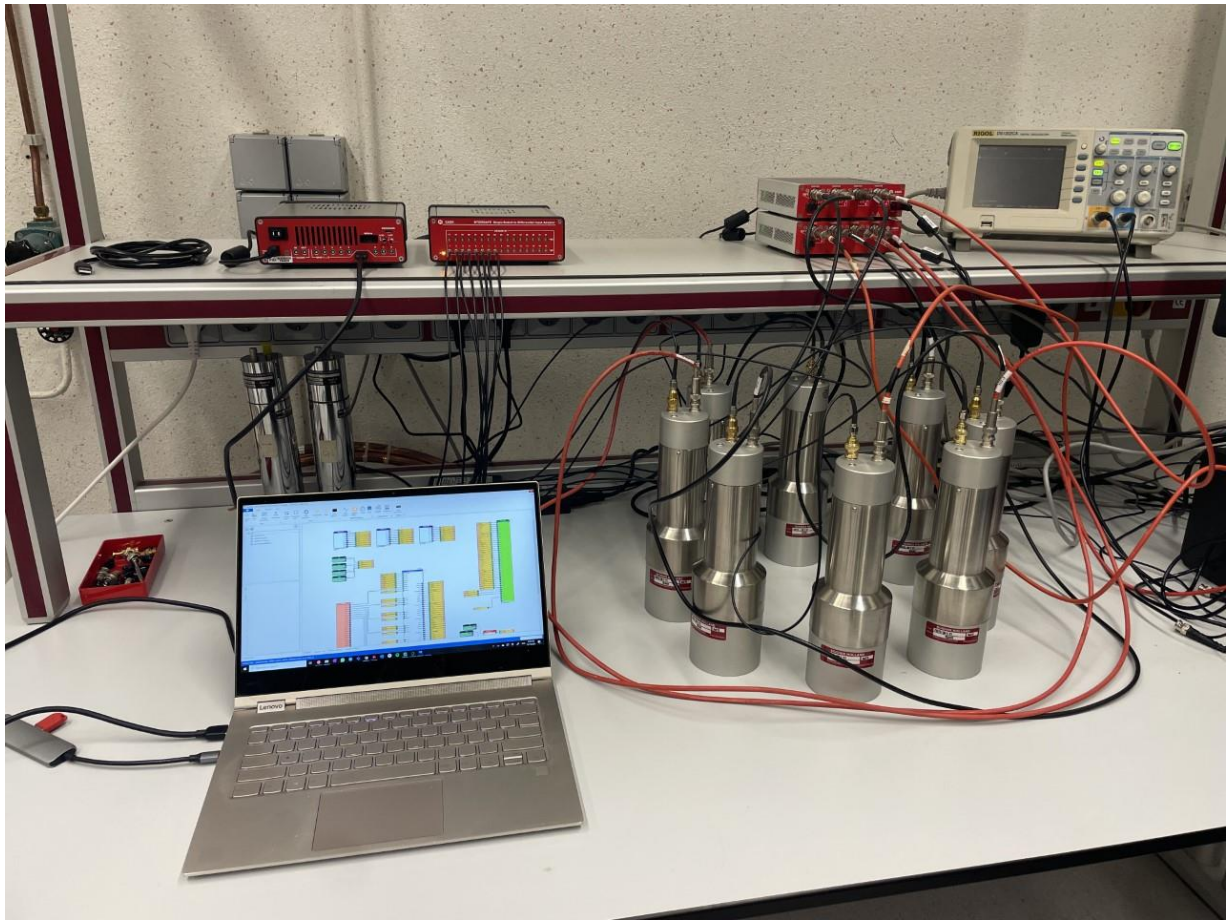
19% dead time, 200 eV @ 2 Mcps OCR

Evaluation of the Maximum Throughput of ARDESIA-16 with Different Digital Pulse Processors – *B. Pedretti*

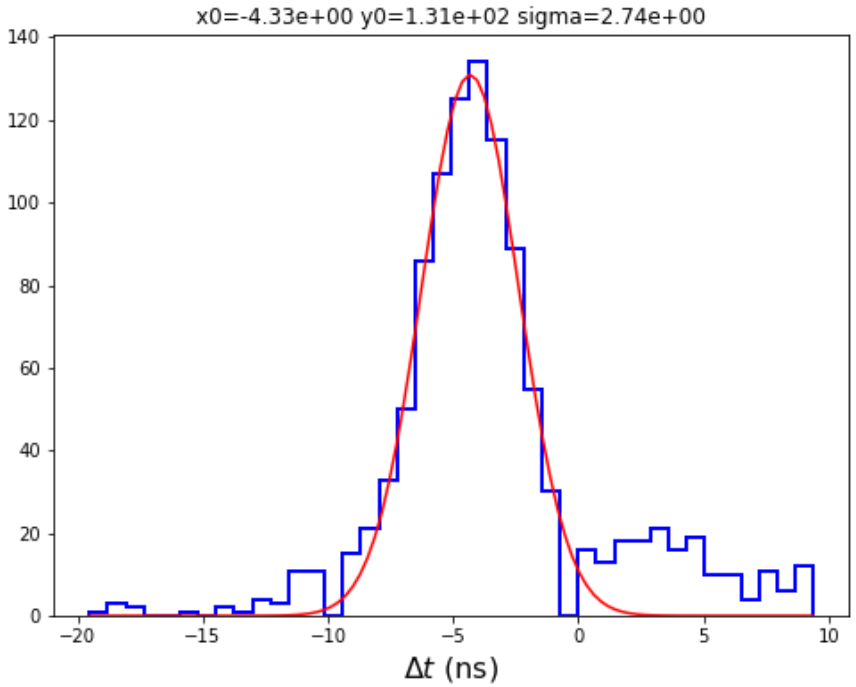
POLITECNICO MILANO 1863

DEIB

(NIKHEF) Sub-ns Time of flight measurament with DCFD



Sub-ns time of flight of correlated gamma measurement using DT5550, PMTs and a custom firmware developed using SciCompiler

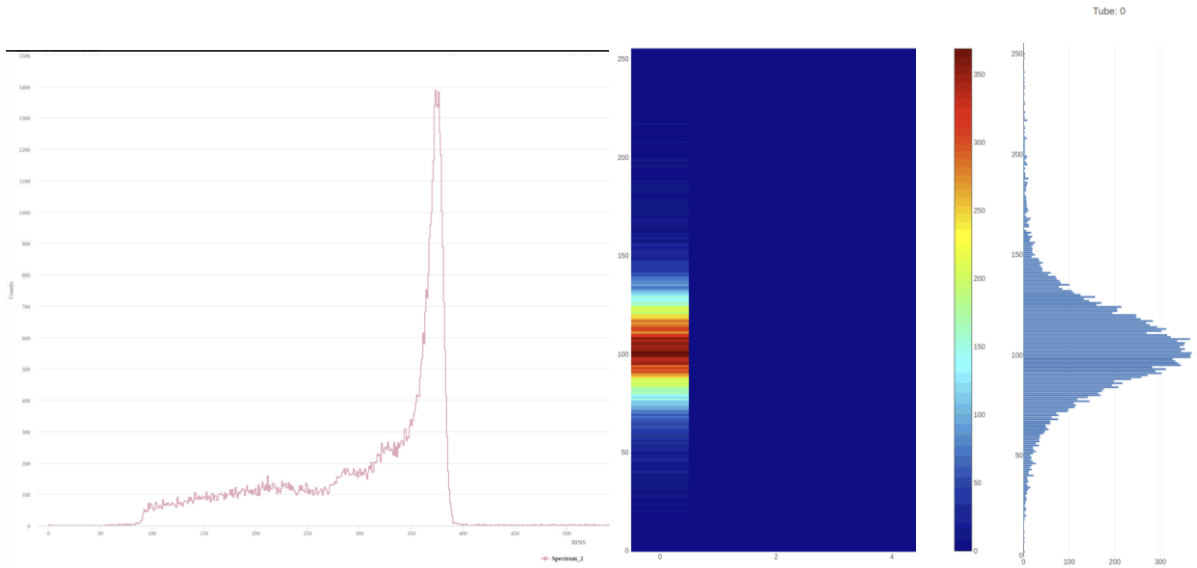


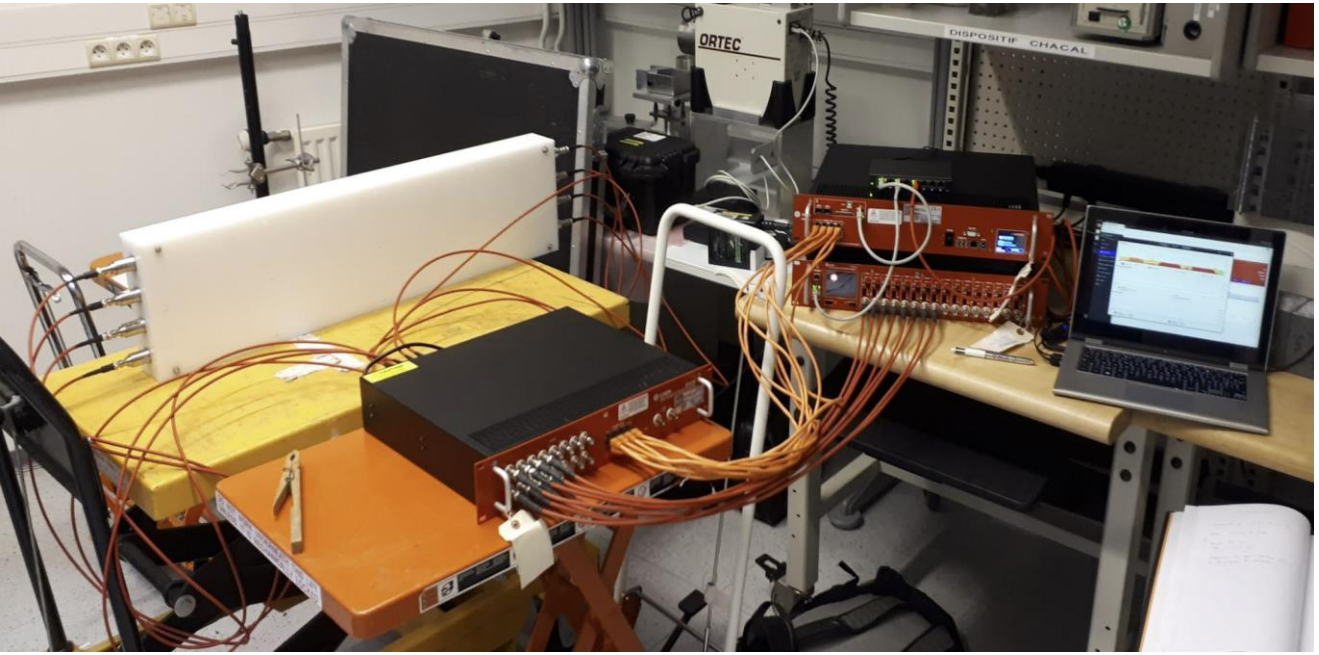
Nikhef

Auke Colijn - Nikhef

(IRSN) Position sense He3 tube

Real time calculation of neutron interaction point using He3 tubes. 32 channels realtime center of mass and energy spectrum calculation.



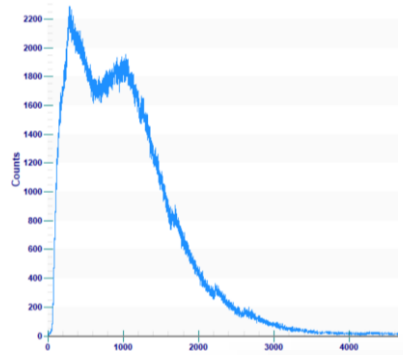


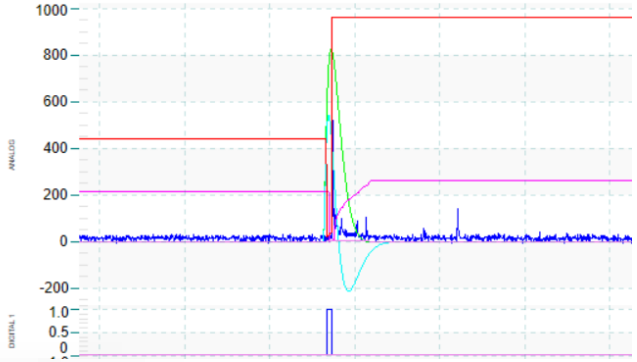
picture from IRSN

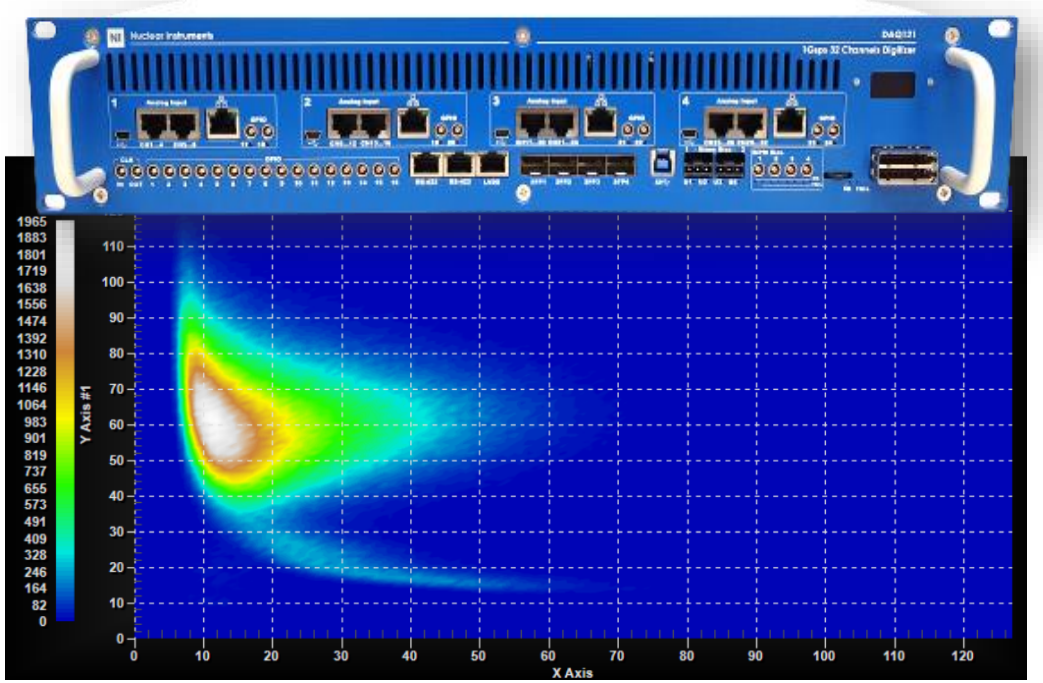
IRSN
INSTITUT DE RADIOPROTECTION
ET DE SÛRETÉ NUCLÉAIRE

(ISIS) Realtime PSD on GS20 scintillator and Nanoparticles detectors

- DAQ 121, 1 GSPS 14 bit Advanced DSP
- Innovative Neutron detectors test beam with good gamma/neutron separation
- Reatime PSD SciCompiler Firmware







Science and Technology Facilities Council

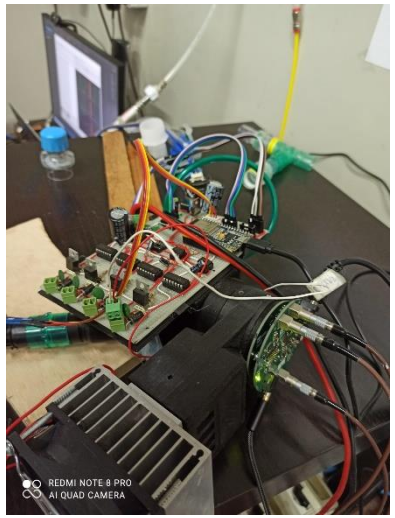
Years of ISIS Neutro and Muon Source

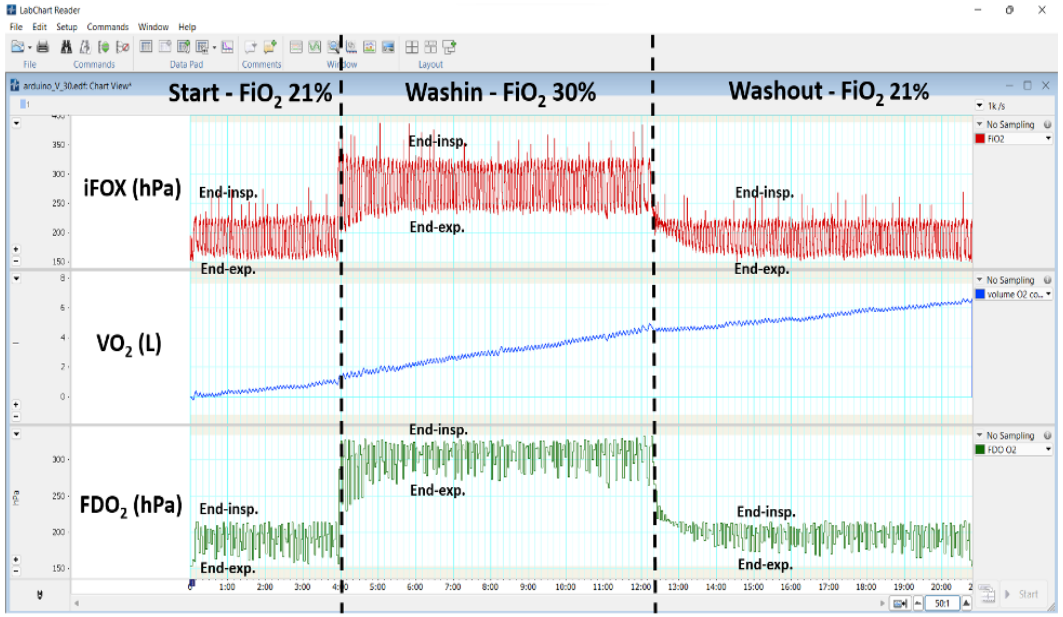
University of BRISTOL

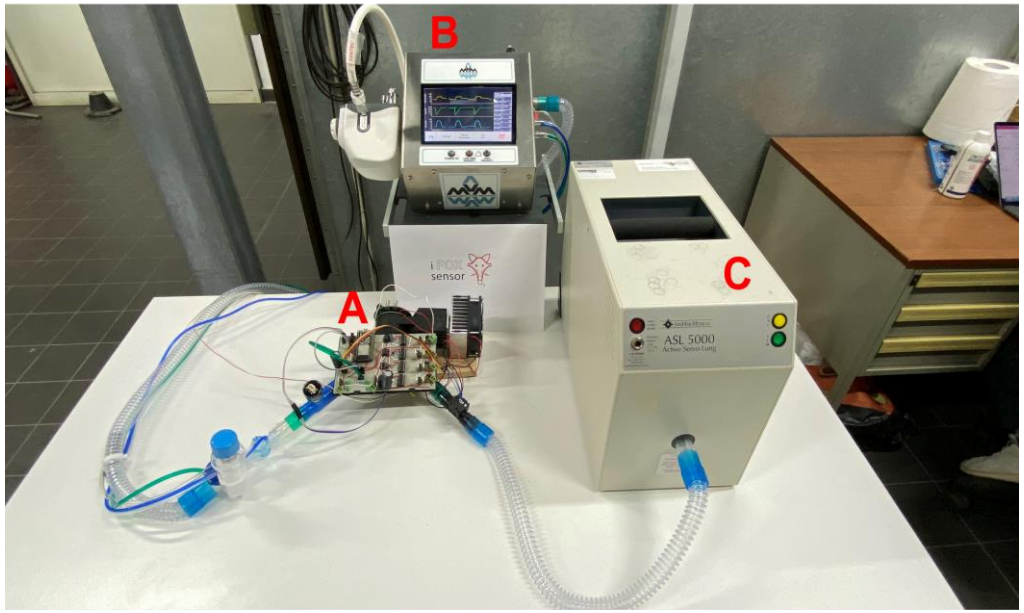
EMAM

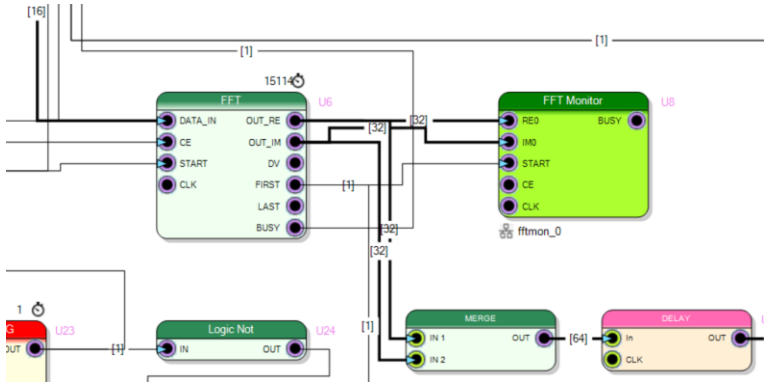
Nuclear Instruments

(CNR) IFOX Sensor – Italian Fast Oxygen Sensor









Set up of the preclinical study by using the iFOX sensor (A), the Mechanical Ventilator Milano (MVM) (B) and the lung simulator ASL 5000 (C).

IFOx SENSOR

Marchio registrato numero 302022000044975

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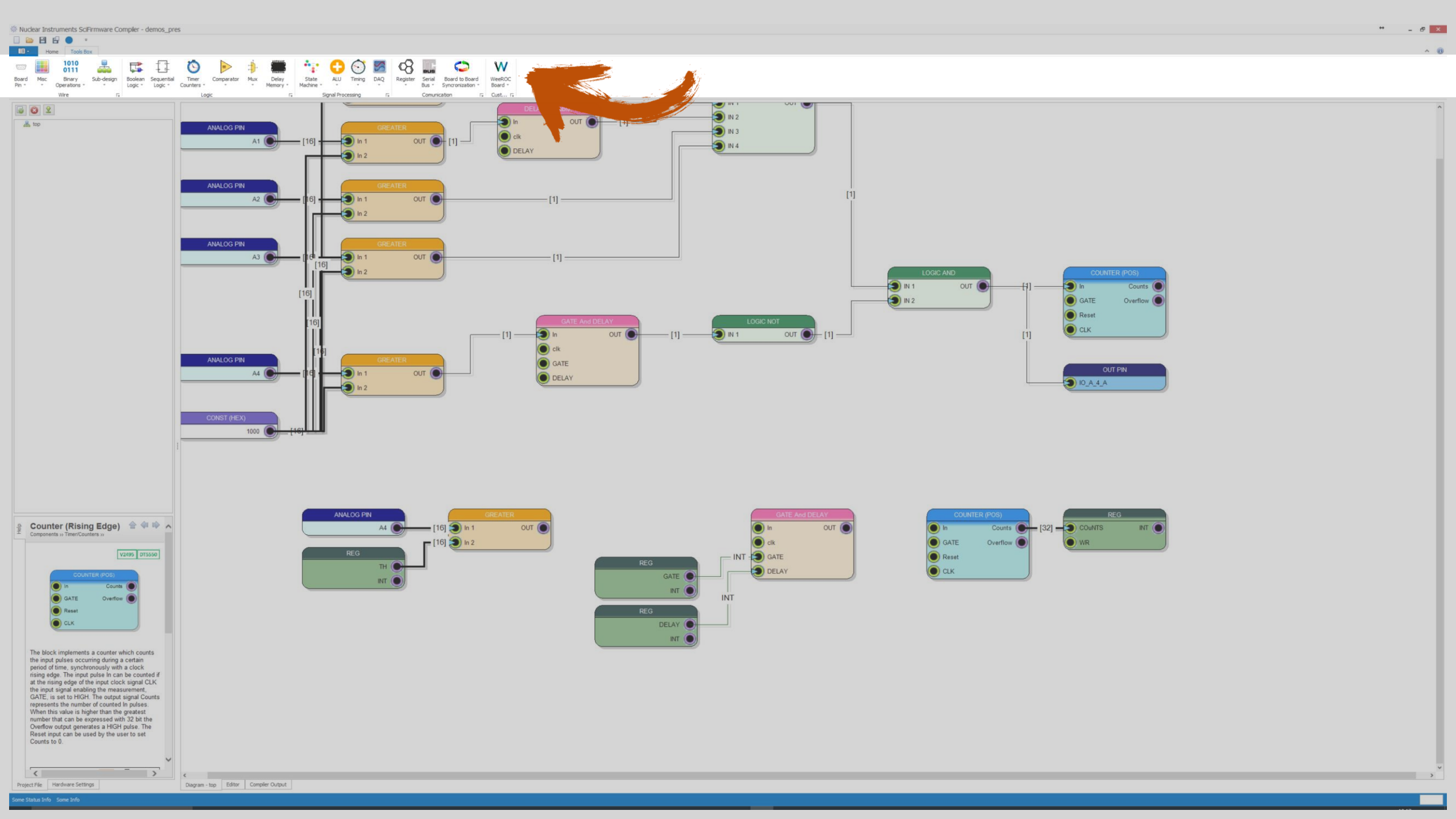
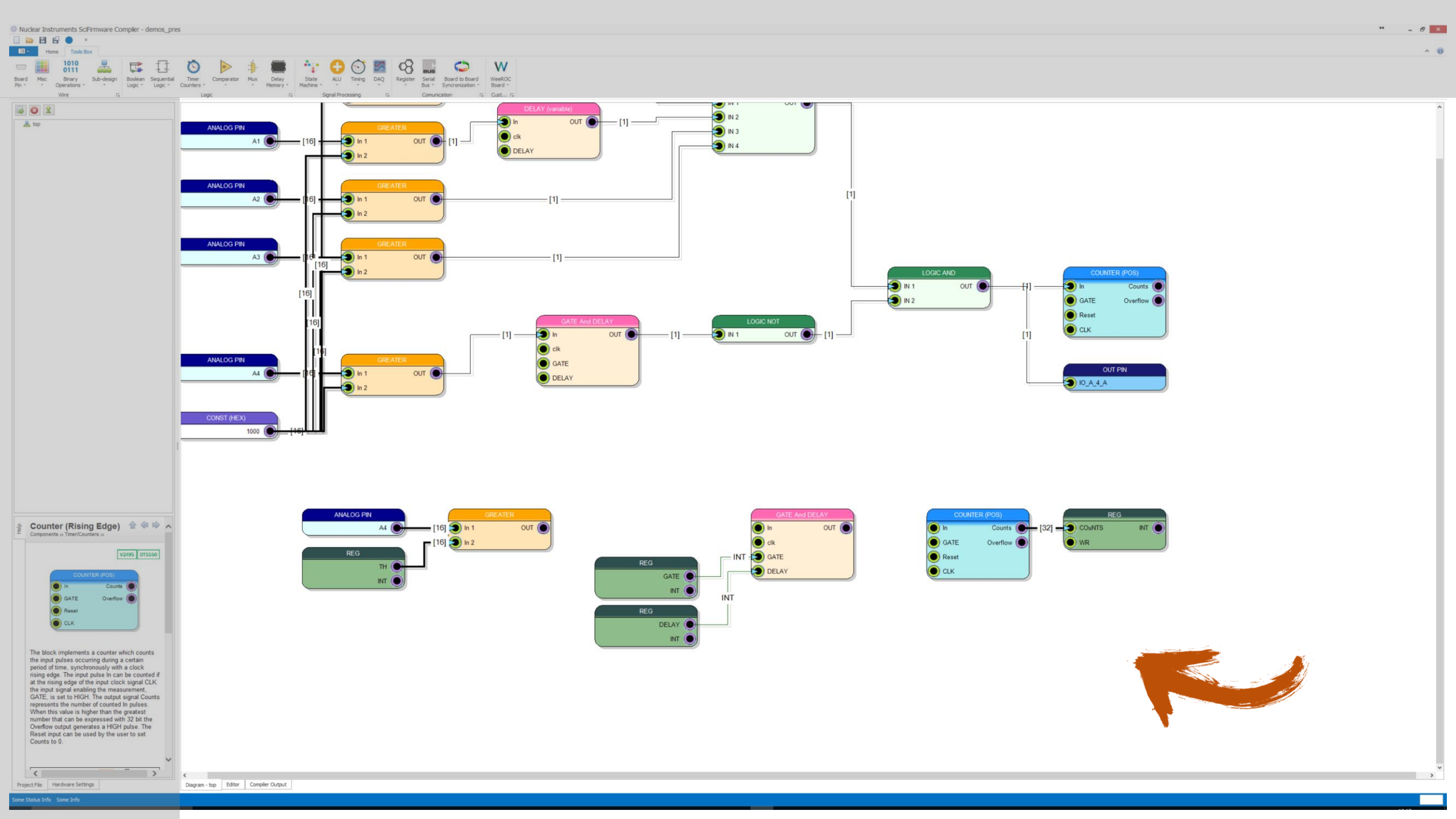
UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA

ISTP ISTITUTO PER LA SCIENZA E TECNOLOGIA DEI PLASMI
Consiglio Nazionale delle Ricerche


Nuclear Instruments SciFirmware Compiler - demos_pres
Home
Tools Box
Board Pin
Misc
Binary Operations
Sub-design
Boolean Logic
Sequential Logic
Timer Counters
Comparator
Mux
Delay Memory
State Machine
ALU
Timing
DAQ
Register
Serial Bus
Board to Board Syncronization
WeeROC Board
Wire
Logic
Signal Processing
Comunication
top
ANALOG PIN
A1
A2
A3
A4
GREATER
In 1
In 2
OUT
[16]
[1]
CONST (HEX)
1000
GATE And DELAY
In
clk
GATE
DELAY
LOGIC NOT
LOGIC AND
IN 1
IN 2
IN 3
IN 4
COUNTER (POS)
Counts
Overflow
Reset
CLK
OUT PIN
IO_A_4_A
REG
TH
INT
COuNTS
WR
[32]
Counter (Rising Edge)
Components ›› Timer/Counters ››
V2495
DT5550
The block implements a counter which counts the input pulses occurring during a certain period of time, synchronously with a clock rising edge. The input pulse In can be counted if at the rising edge of the input clock signal CLK the input signal enabling the measurement, GATE, is set to HIGH. The output signal Counts represents the number of counted In pulses. When this value is higher than the greatest number that can be expressed with 32 bit the Overflow output generates a HIGH pulse. The Reset input can be used by the user to set Counts to 0.
Help
Project File
Hardware Settings
Diagram - top
Editor
Compiler Output
Some Status Info
Some Info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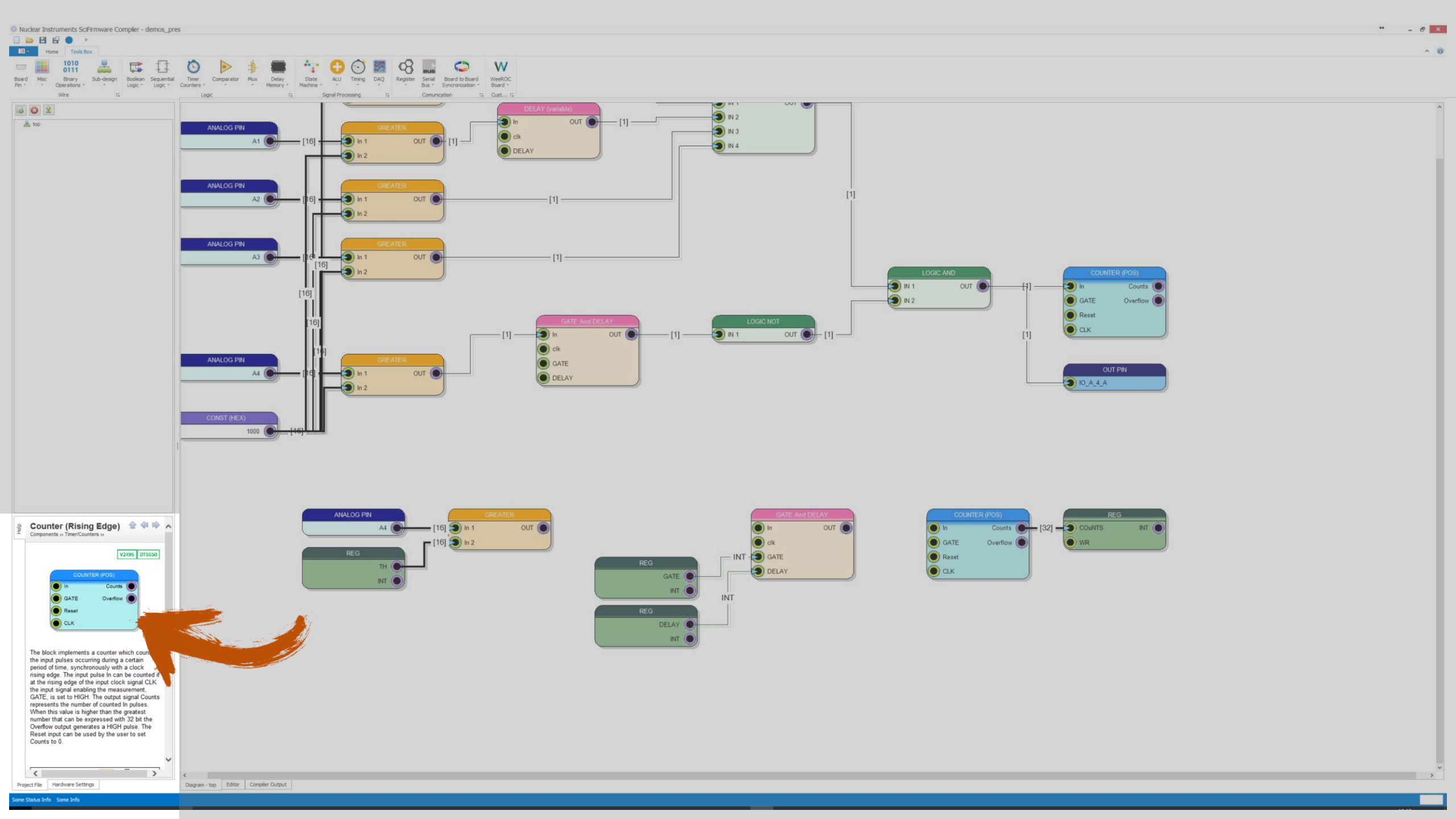
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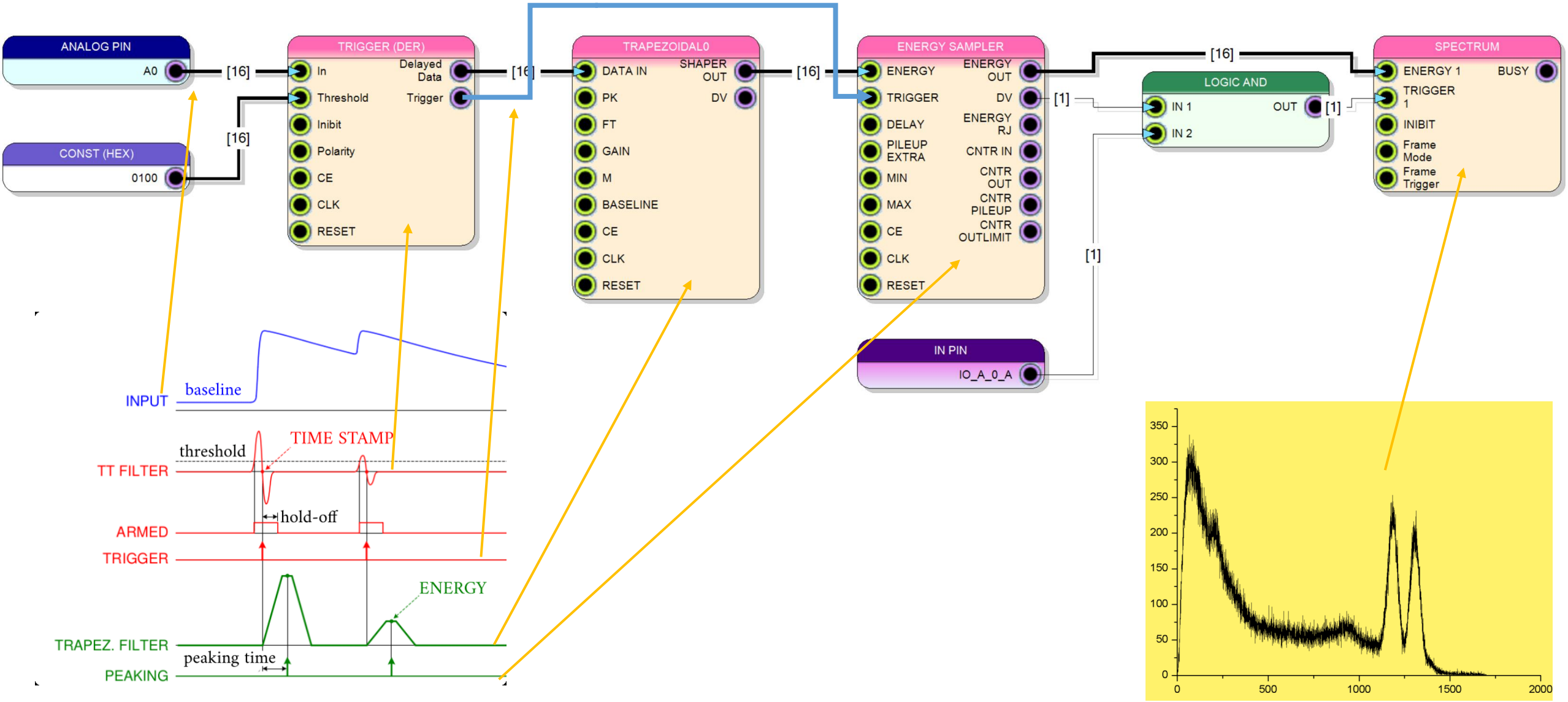
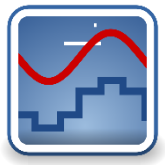
Implementation of PHA



Open-FPGA Board architecture

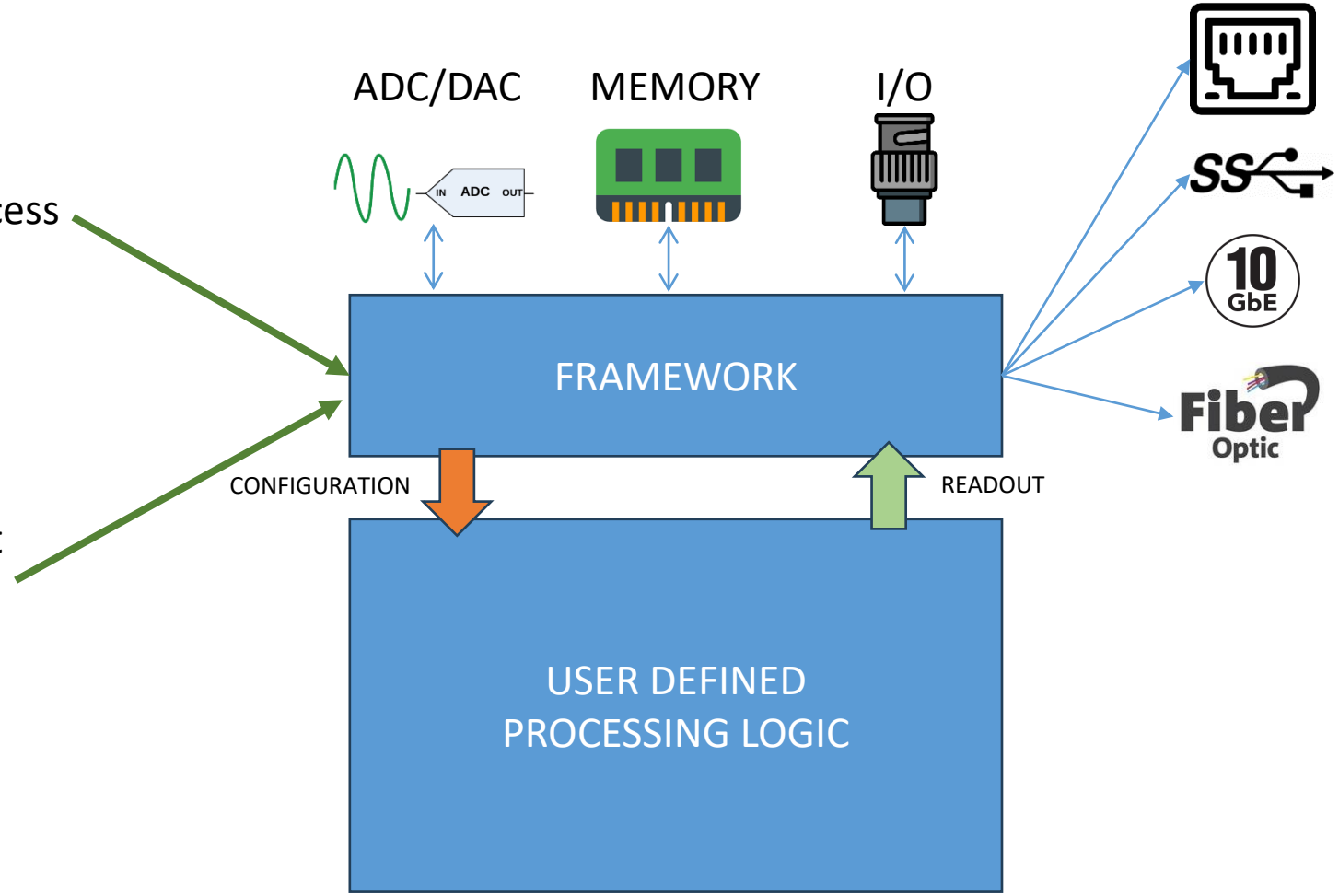
Primary function of a firmware:



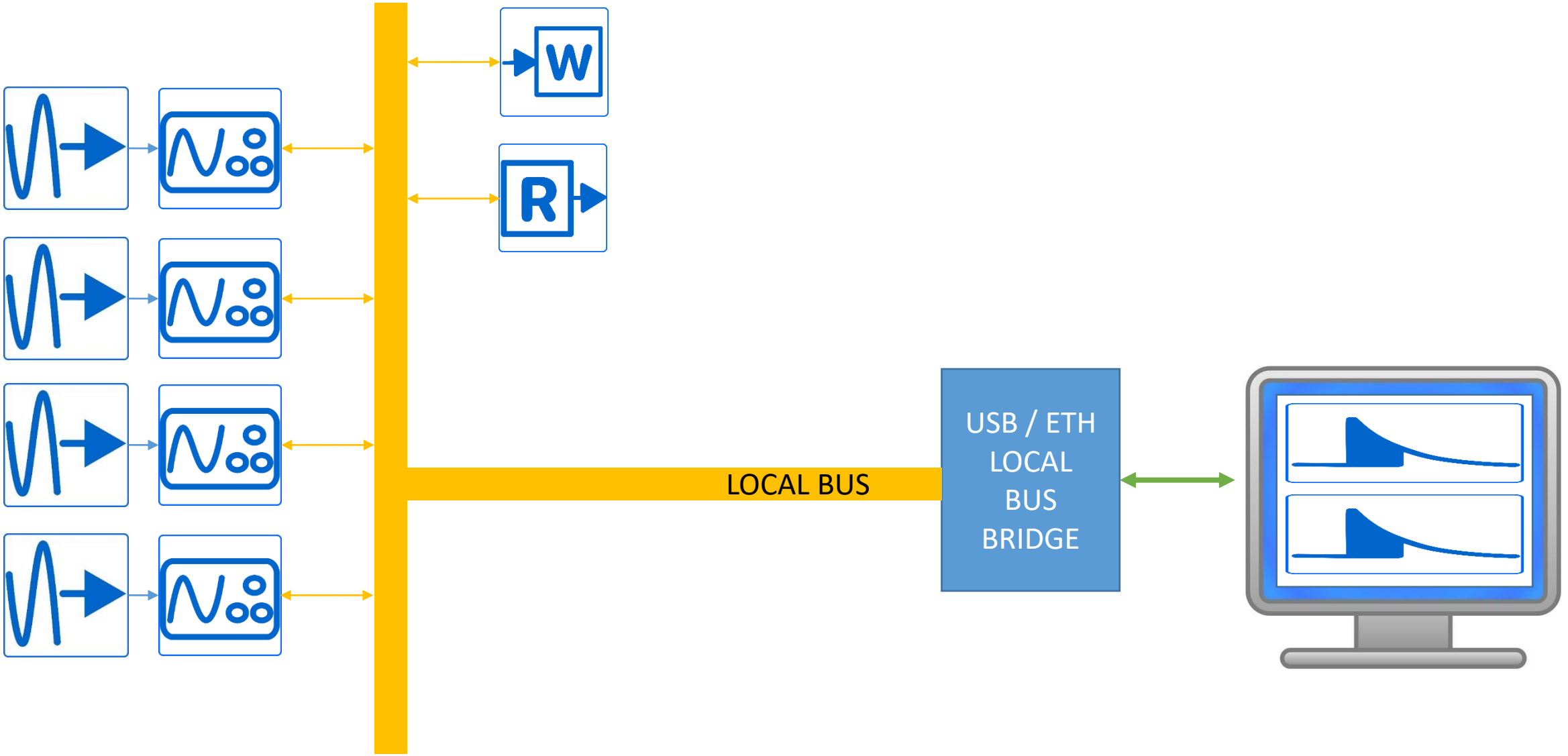
Control the board acquisition process

Processing data

Transfer data to and from readout PC/Server



Data readout



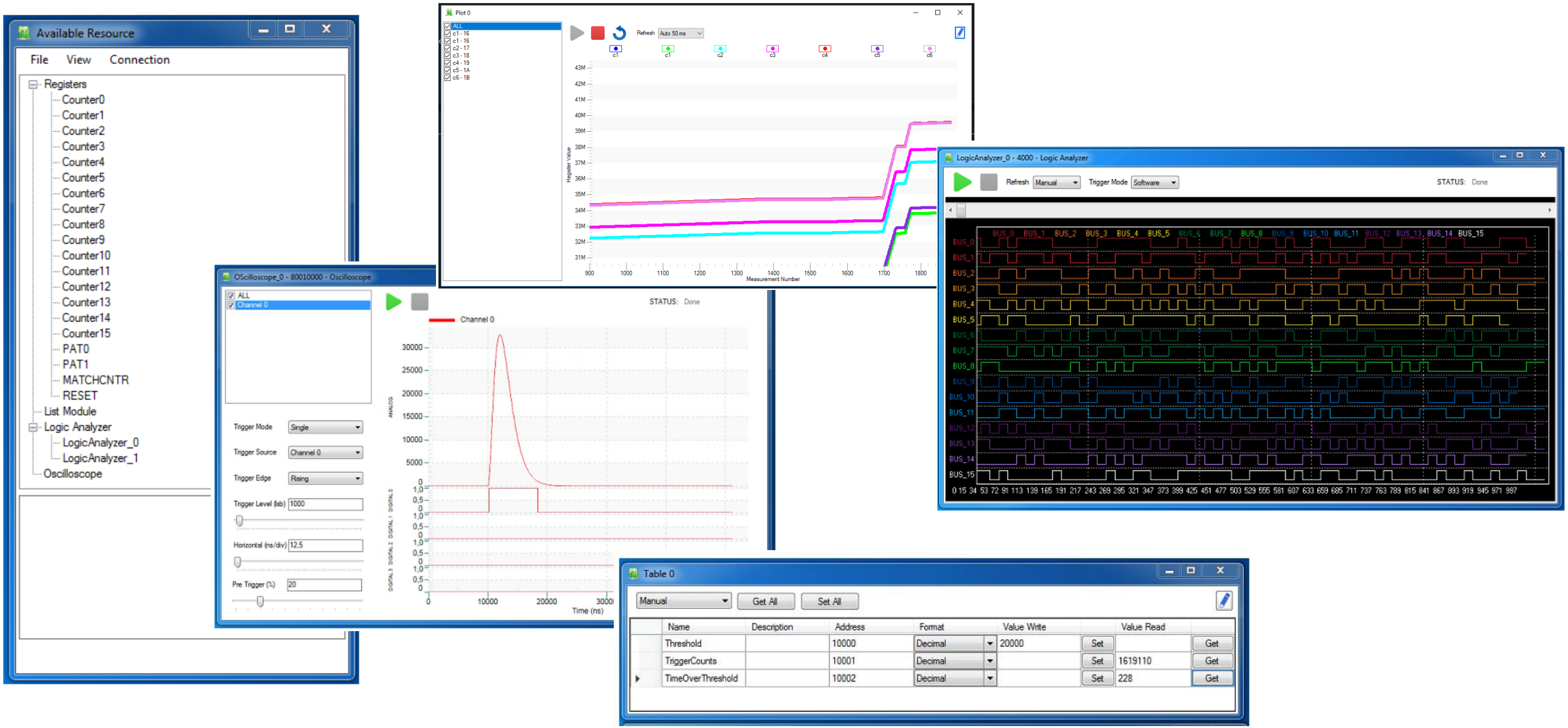
Data readout

SCI-COMPILER → Generate Firmware

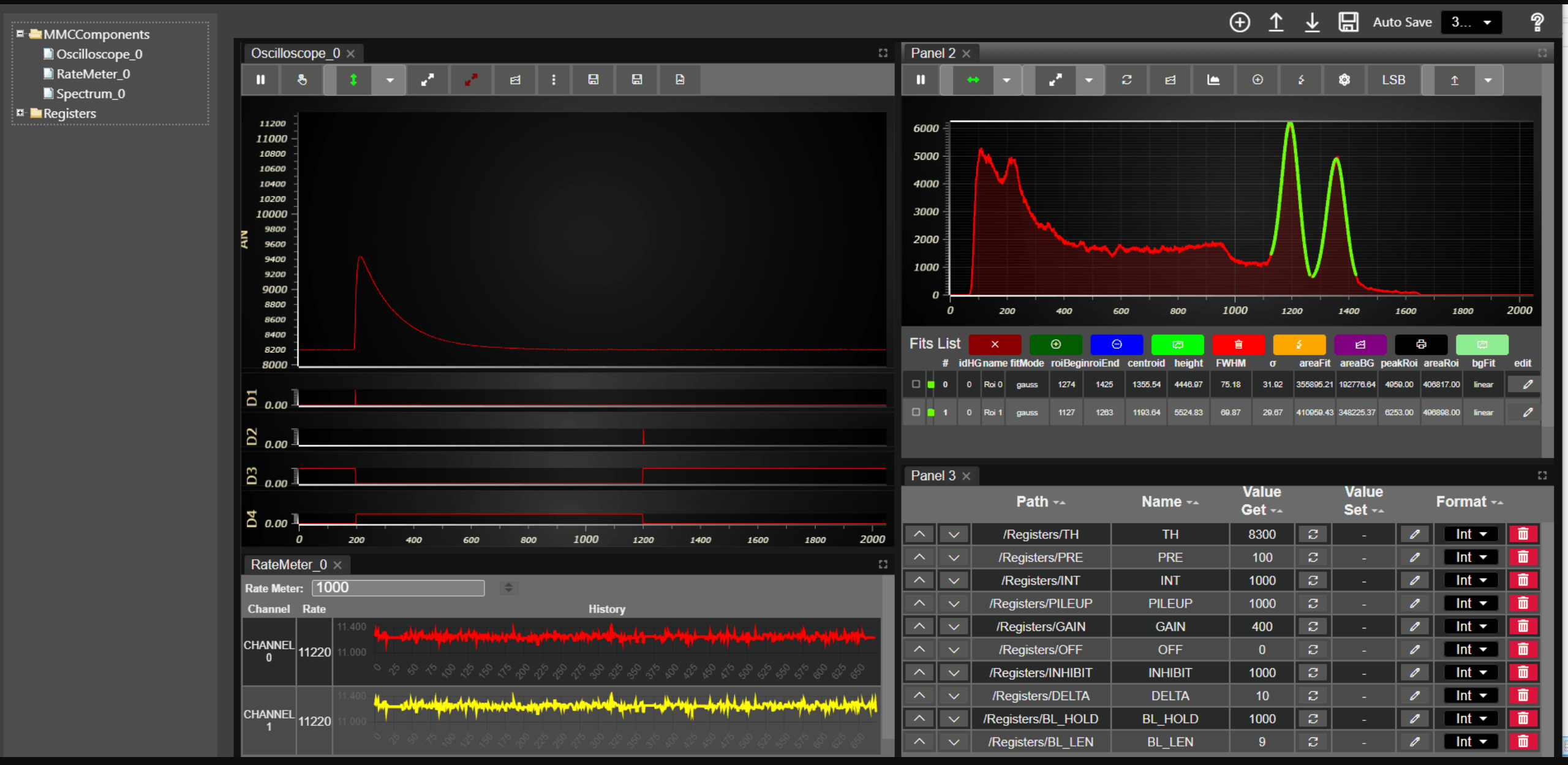
RESOURCE EXPLORER → Visual Firmware Debug

SCI-SDK → Data Readout

Data readout – Resource explorer and SDK



Web Interface available on all new instruments



Data readout – Resource explorer and SDK

Available open source on GitHUB

https://github.com/NuclearInstruments/SCISDK

SCI-SDK

Works on: Windows, Linux
Compatible with Raspberry PI

Available on: PIP, NPM, and APT (for Ubuntu) and ANT (java)

Works inside Jupyter Lab, pre installed on new instruments

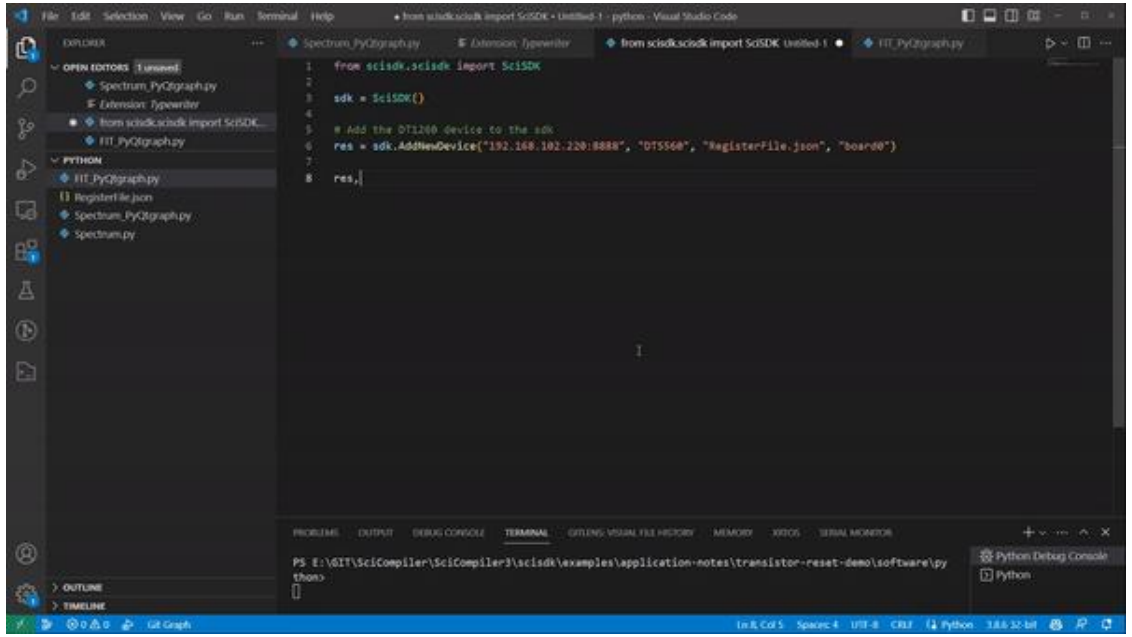
Documentation and examples available here:
https://nuclearinstruments.github.io/SCISDK/

```
int main()
{
    SCISDK_OSCILLOSCOPE *osc_data;

    sdk.AddNewDevice("usb:0006", "dt1
    sdk.StrobeRegister("Registers/res

    sdk.SetParameter("Oscilloscope_0/
    sdk.SetParameter("Oscilloscope_0/trigg
    sdk.SetParameter("Oscilloscope_0/acq_m
    sdk.SetParameter("Oscilloscope_0/data_p
                                    essing

    sdk.ExecuteCommand("Oscilloscope_0", "start");

    sdk.AllocateBuffer("Oscilloscope_0", "decoded_buffer", (void **) &osc_data);

    for (int i = 0; i < 10; i++) {
        sdk.ReadData("Oscilloscope_0", osc_data);
        dump_to_file(osc_data);
    }

    return 0;
```

SDK Software Development Kit

python™ C C++ LabVIEW VB.NET C# node JS Java ROOT Data Analysis Framework MATLAB

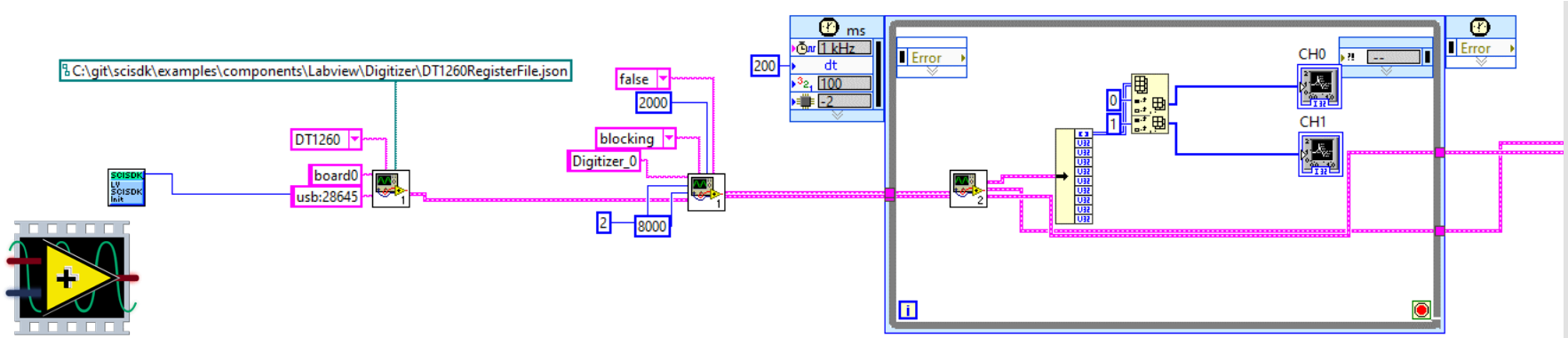
Data readout – Resource explorer and SDK



python™

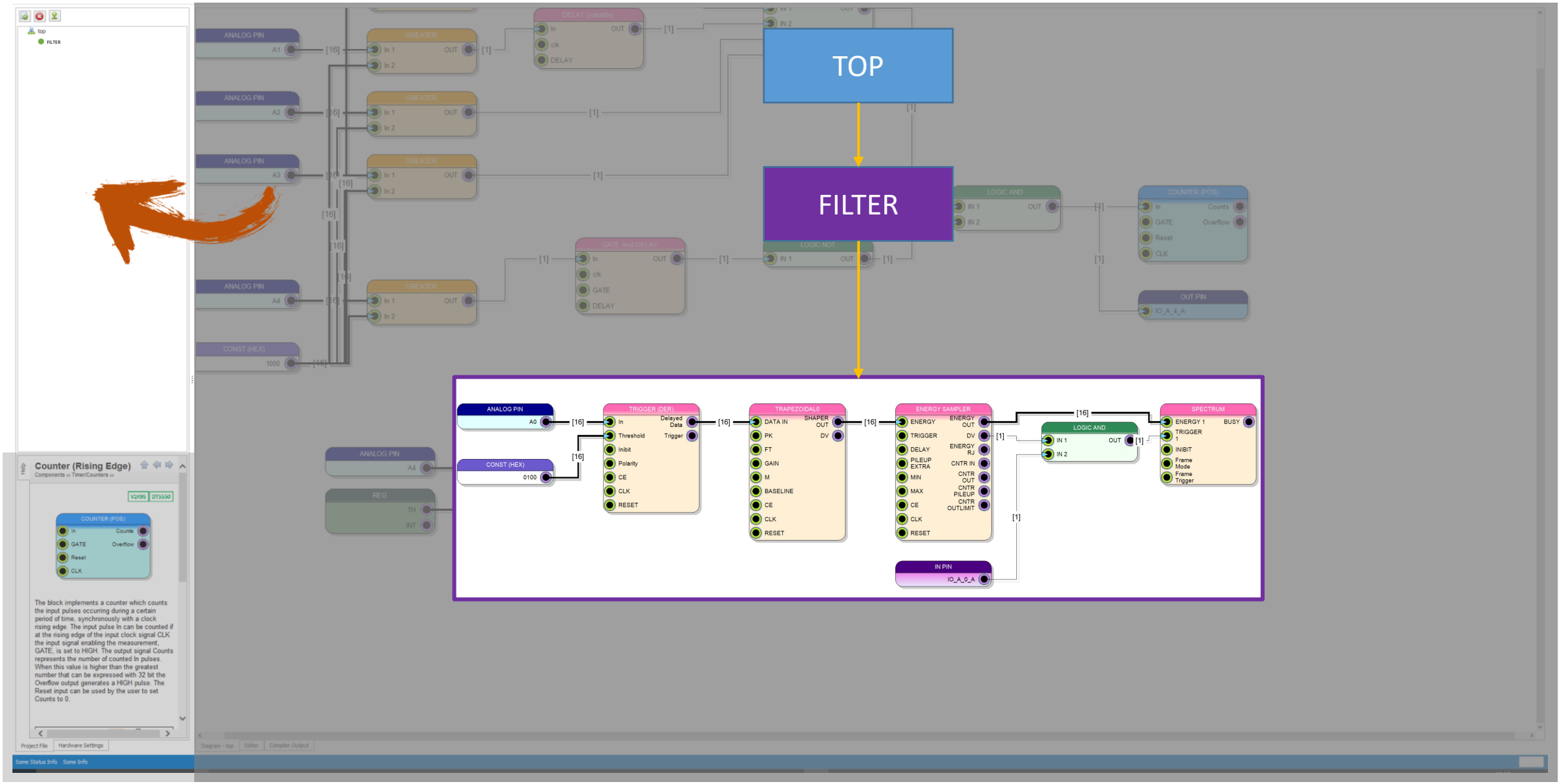
Just enter in your terminal to start using SciSDK

pip install scisdk

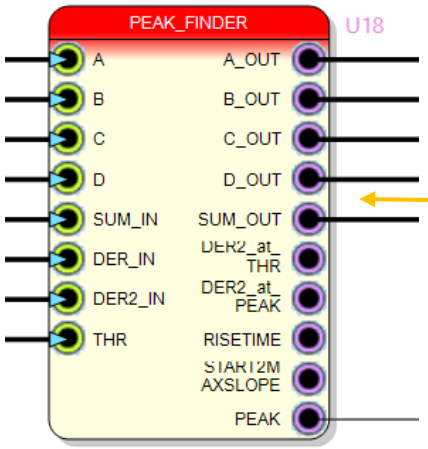


LabVIEW

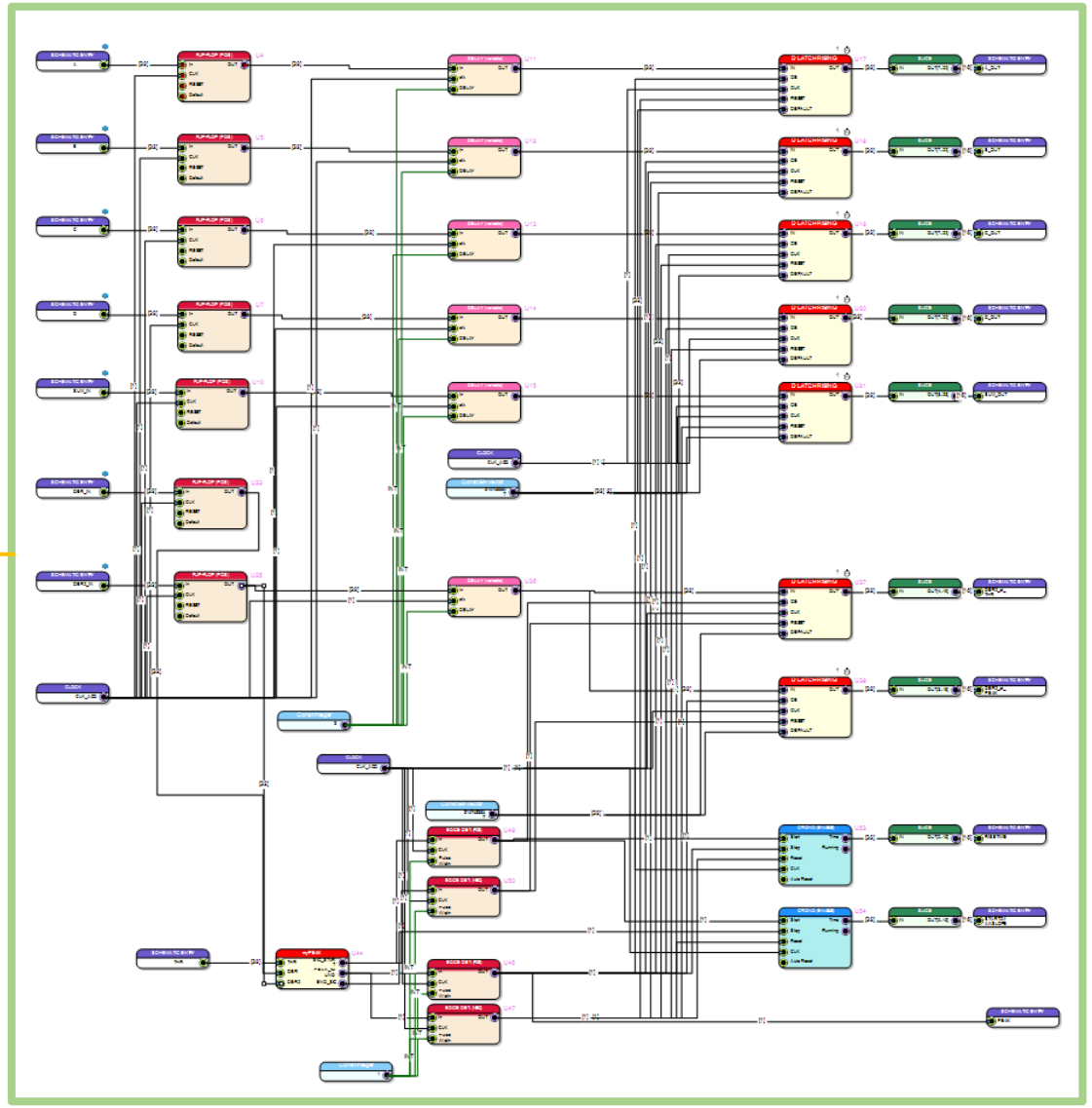
Heirarchical design



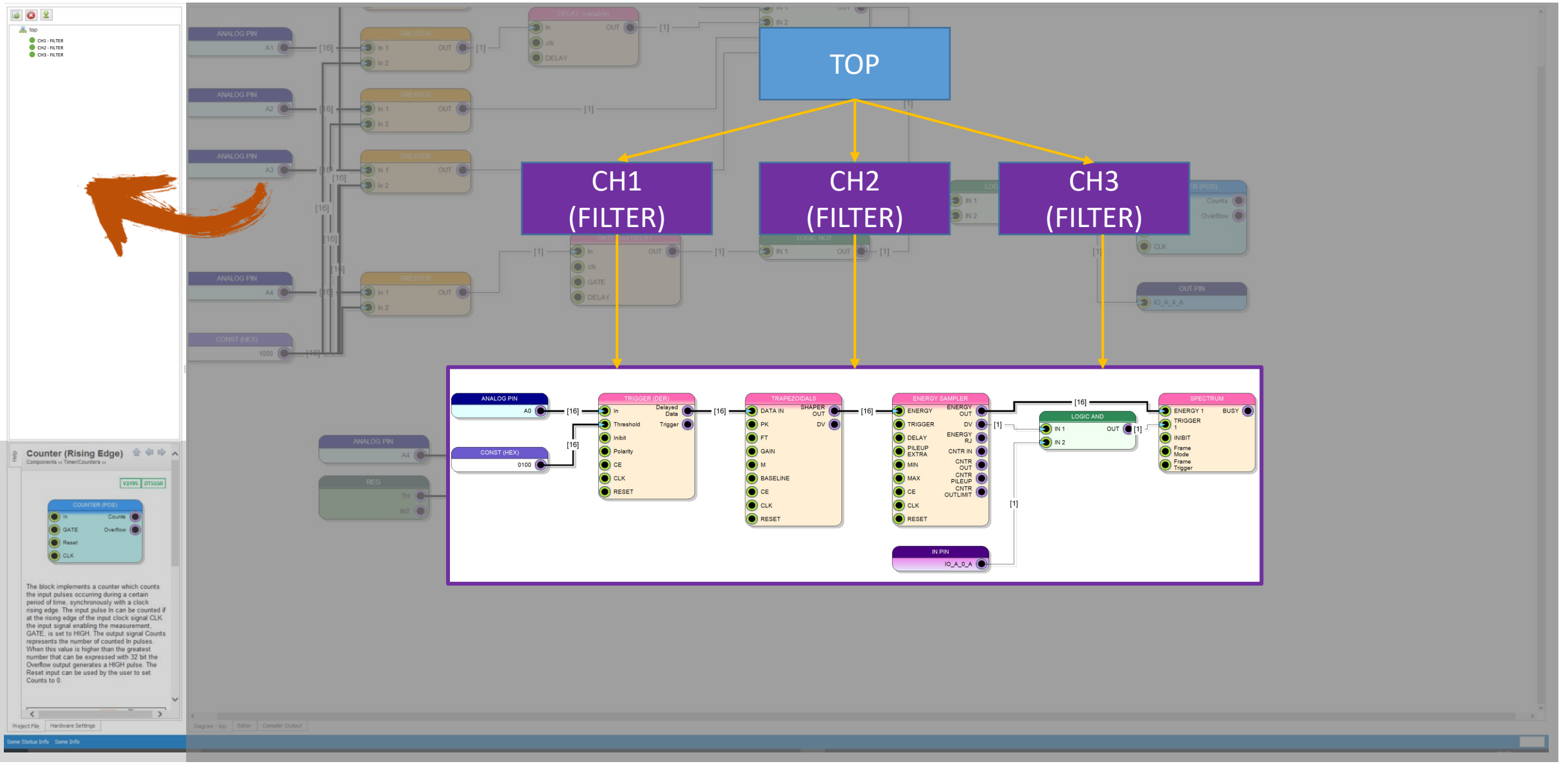
Heirarchical design



PEAK_FINDER



Multi-channel design



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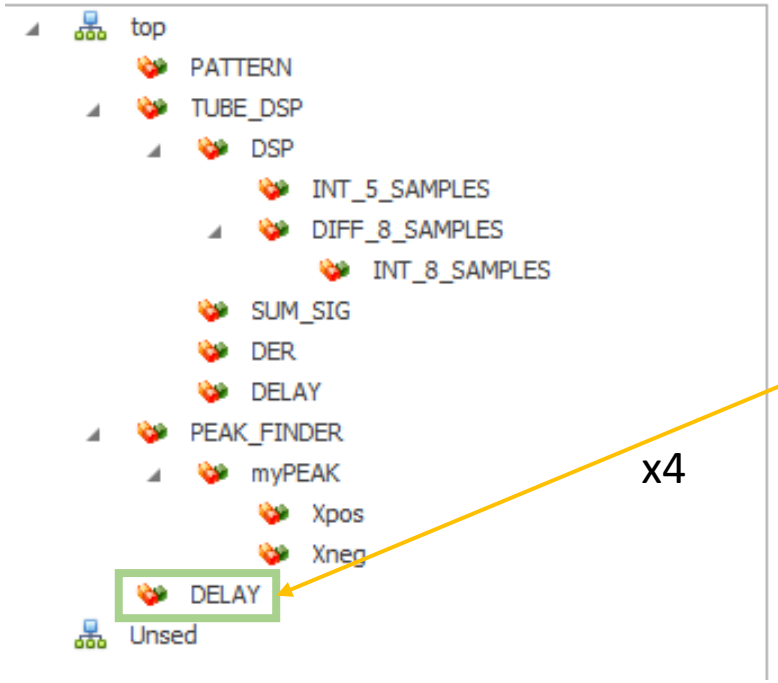
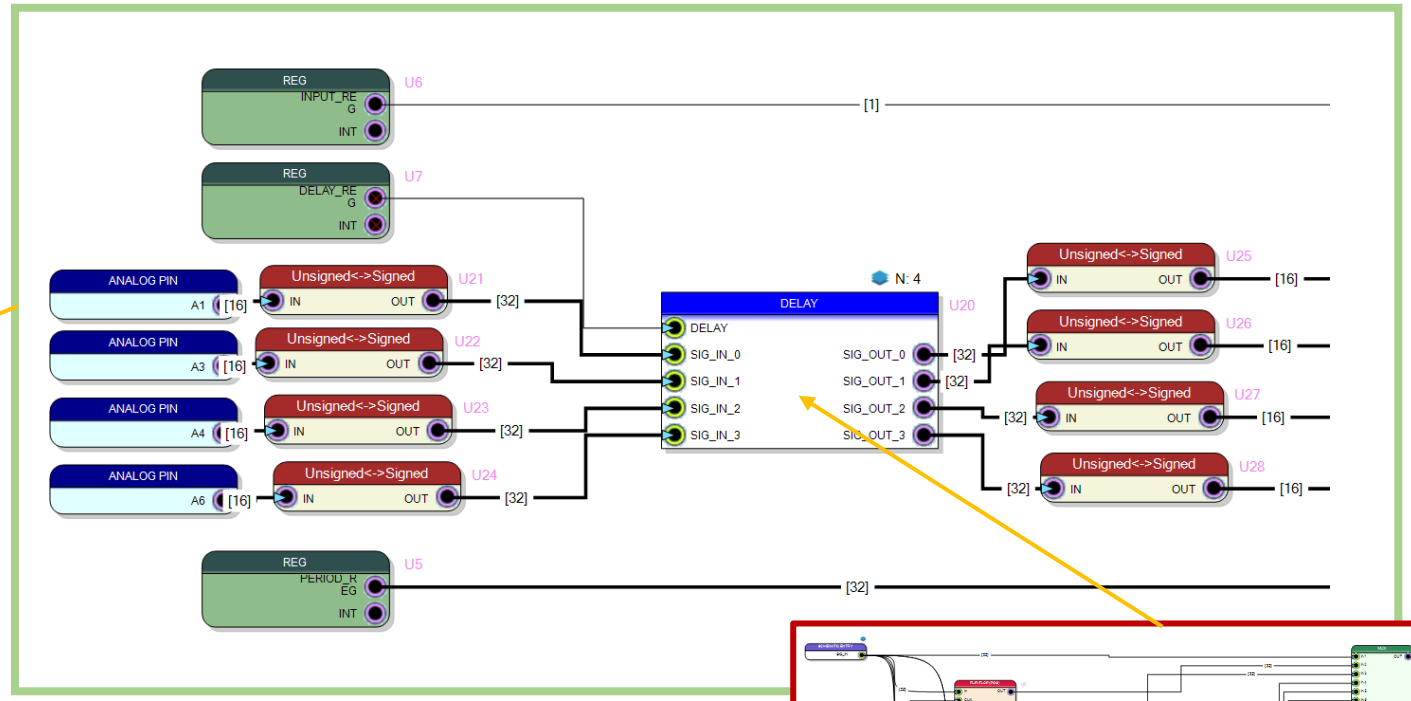
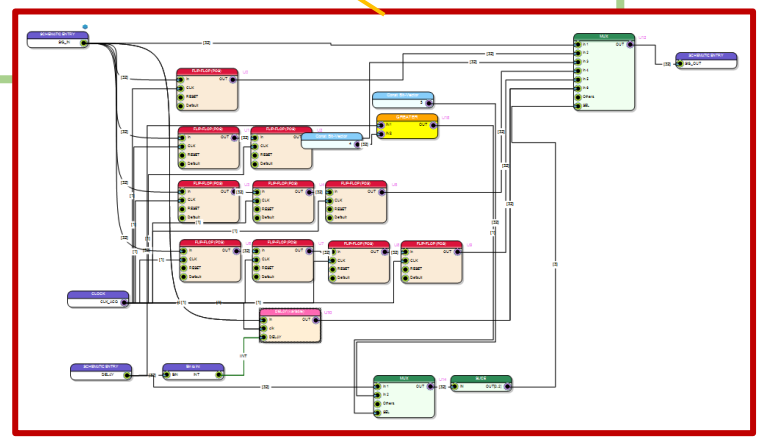


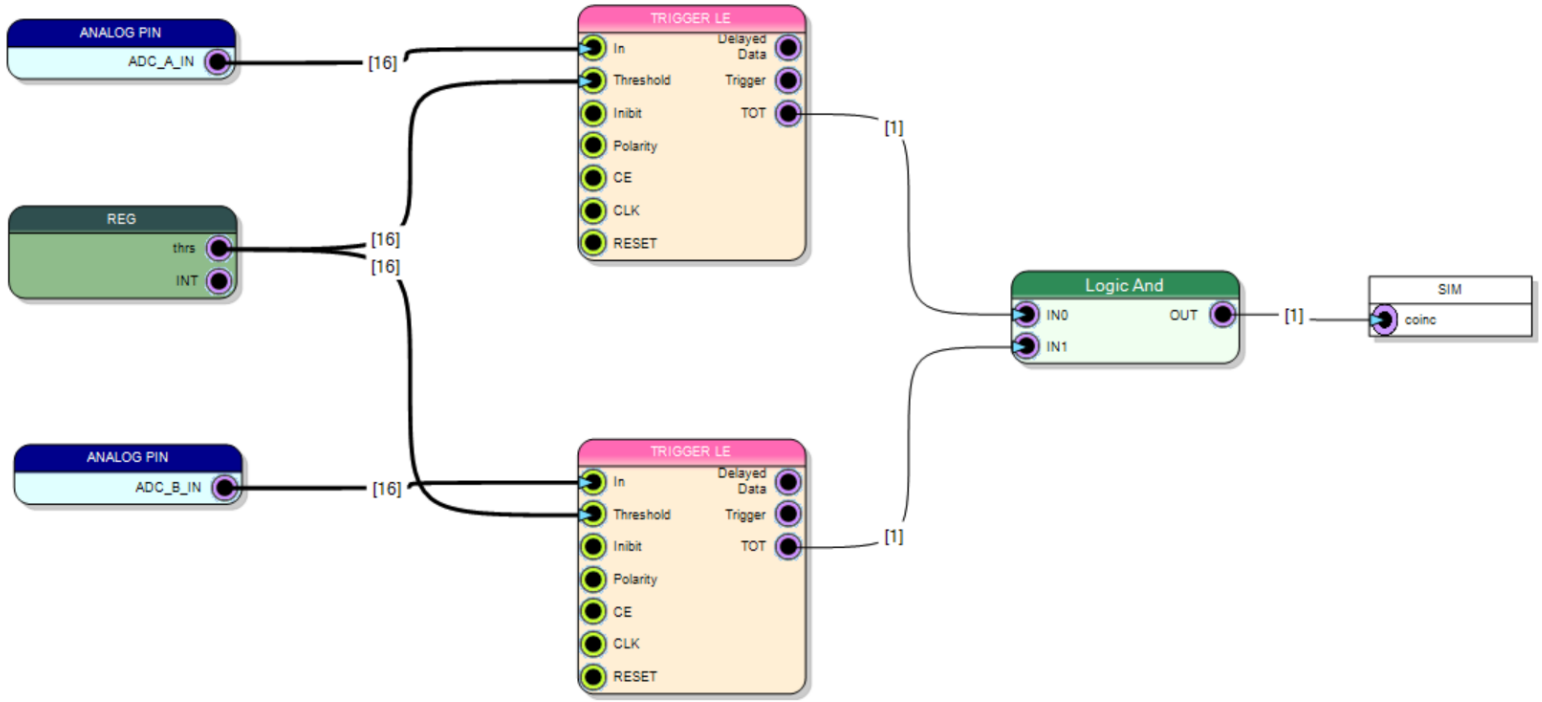
x4





Integrated simulation

- Save your time → Compile can require hours, simulation few seconds
- Simpler debug → You can inspect any net and signal
- Better test coverage → You can insert critical signal to check how firmware perform



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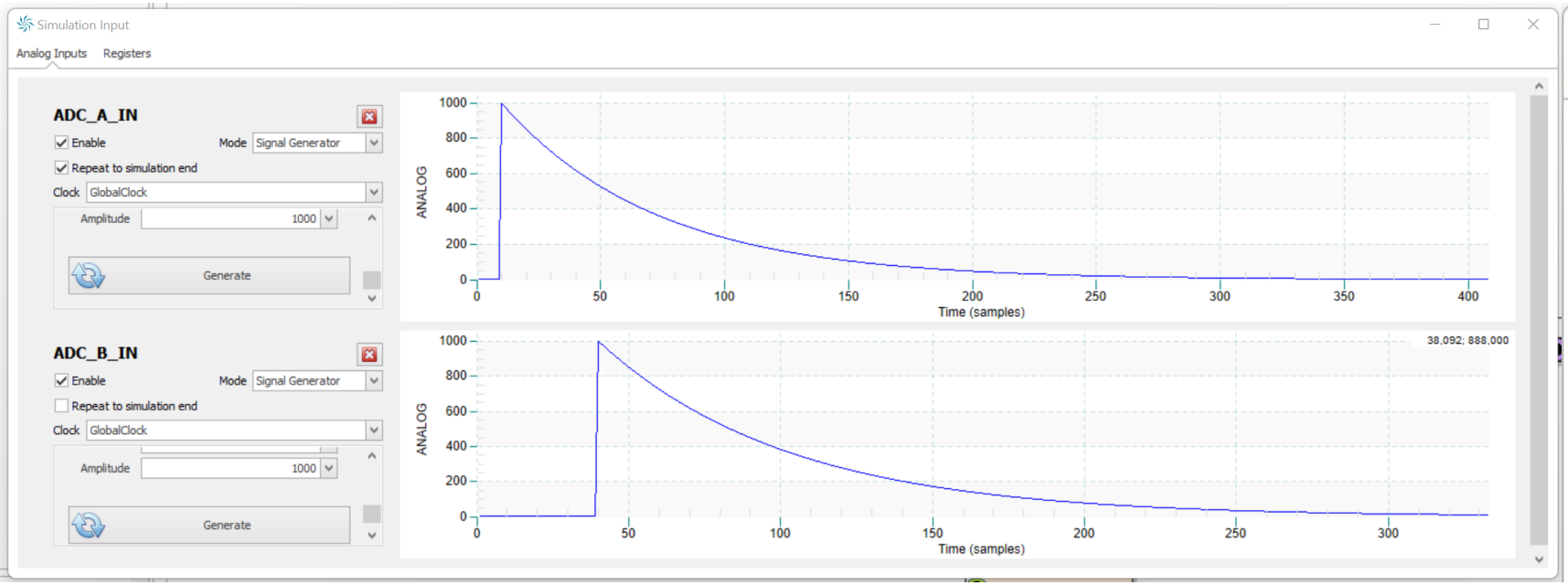
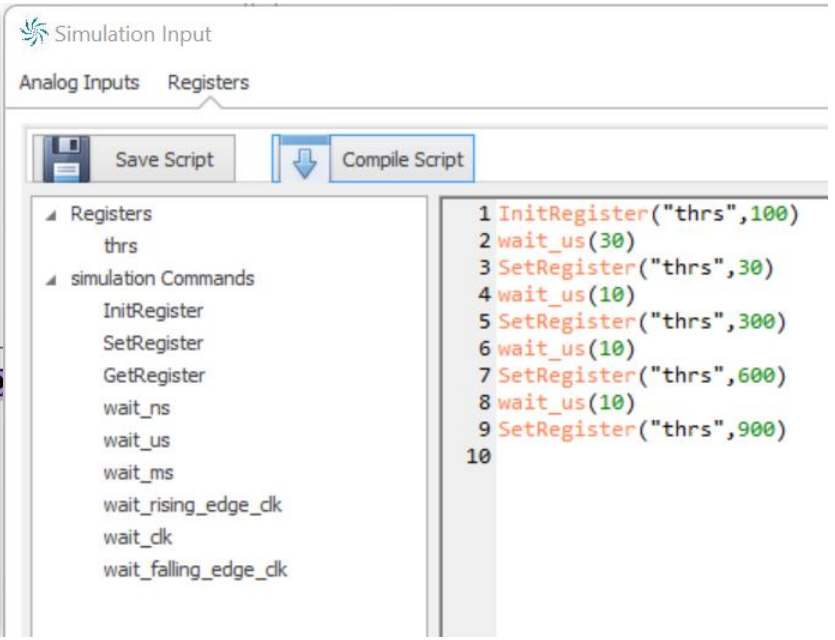
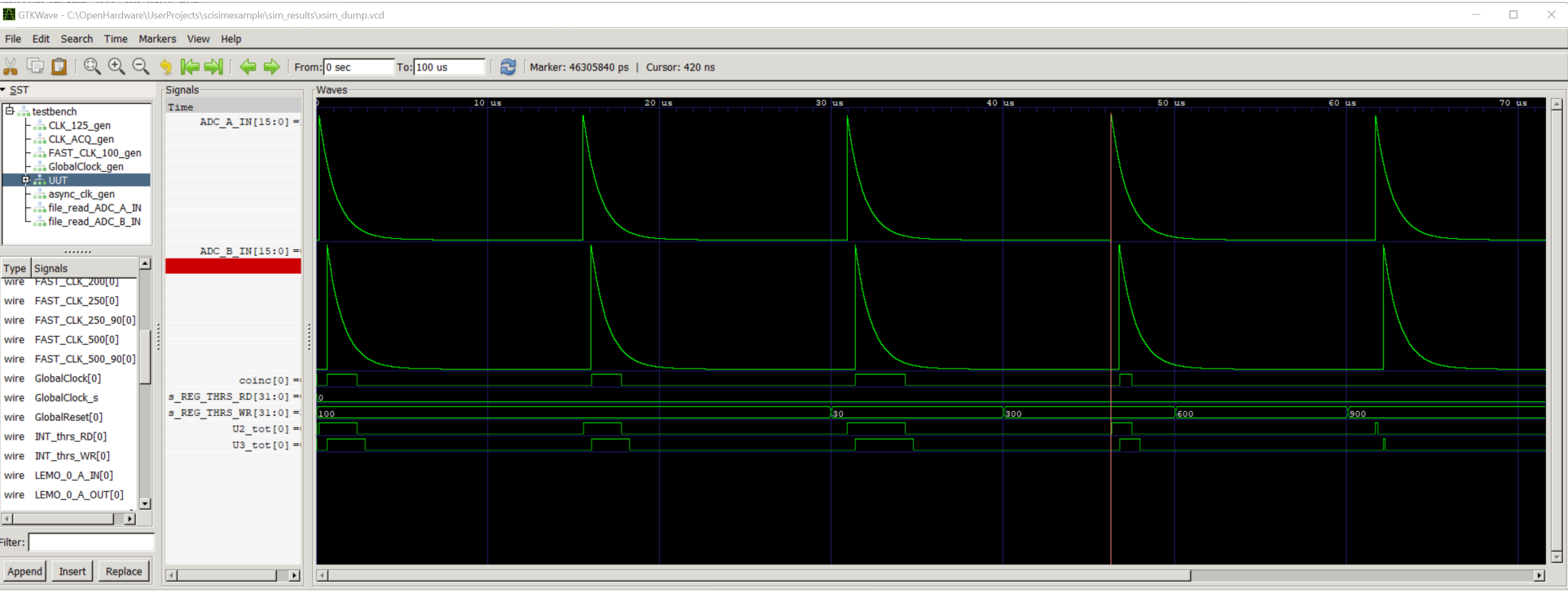


Generate analog signal to replace ADC data stream

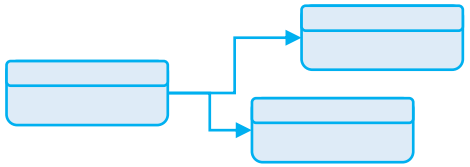


Write script to simulate Register RW

Integrated simulation



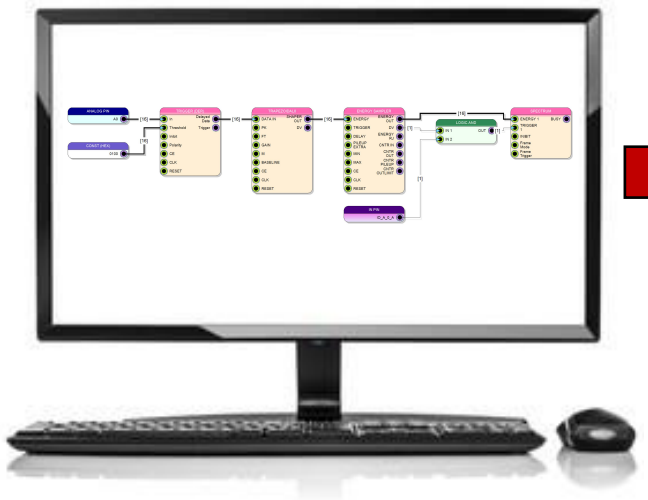
Remote Compile Service based on MyCAEN Cloud

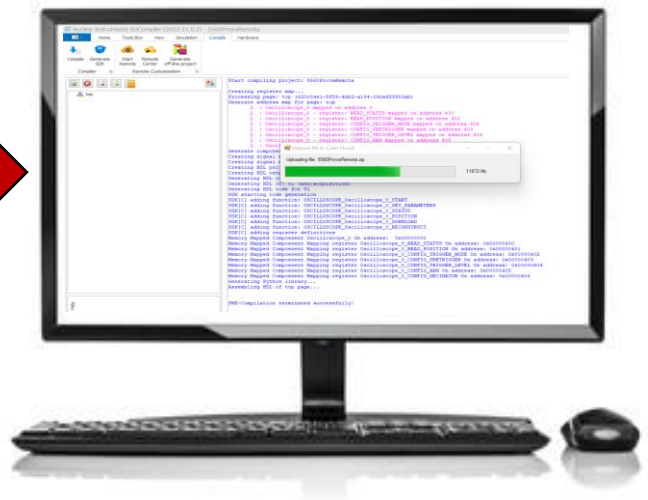


Design entry with SciCompiler

Upload project on the cloud

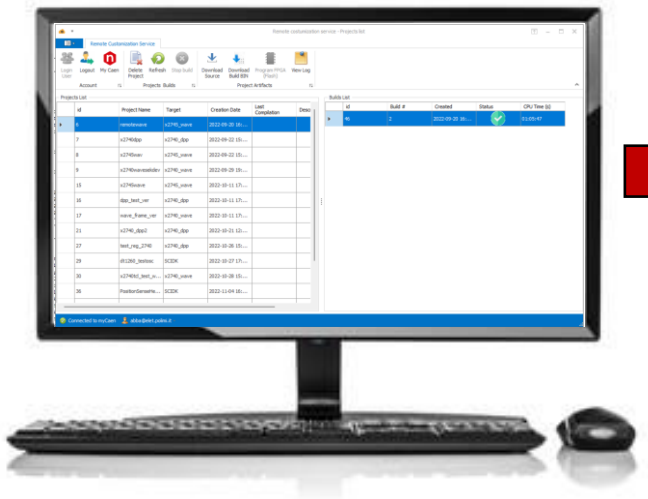
Remote Compile on MyCaen





Remote Compile Service based on MyCAEN Cloud

Download the firmware compiled

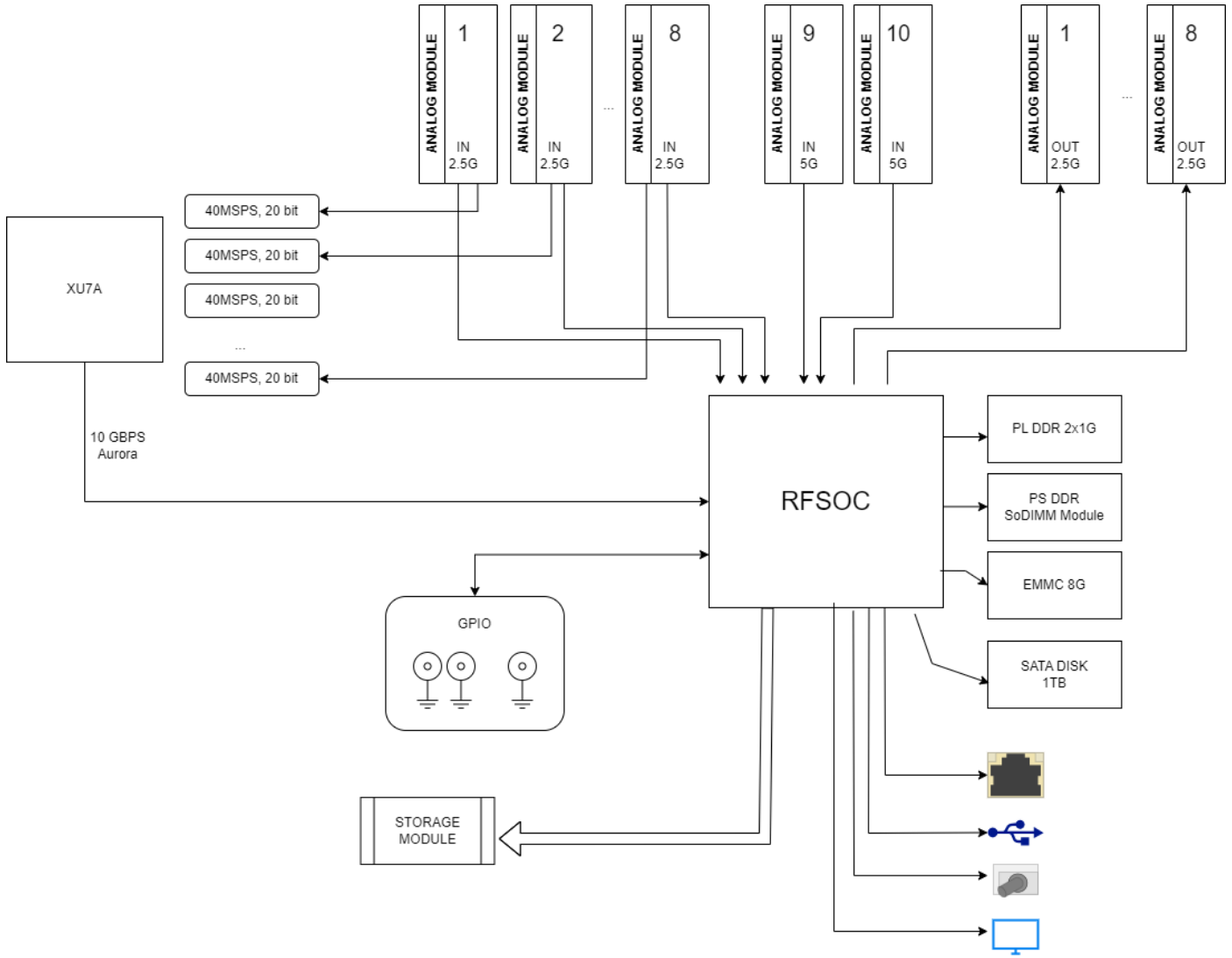


Install the firmware on the device


DT5550
DT5560
V2495
DT550W
R5560
R5560SE
V2730
V2740/5
DT1260
SCICOMPILER
OPENFPGA
HARDWARE PLATFORMS

UPCOMING SYSTEM: WaveJET 5GSPS, 8 channels digitizer

PRELIMINARY



Ultra FAST 5 GSPS Digitizer and Realtime Processor

"VERSION A"

Analog Input:

- 2 x 5 Gsps, 14 bit
- 8 x 2.5 Gsps, 14 bit

Analog Output:

- 8 x 10 Gsps, 14bit

"VERSION B"

Analog Input:

- 8 x 5 Gsps, 14 bit

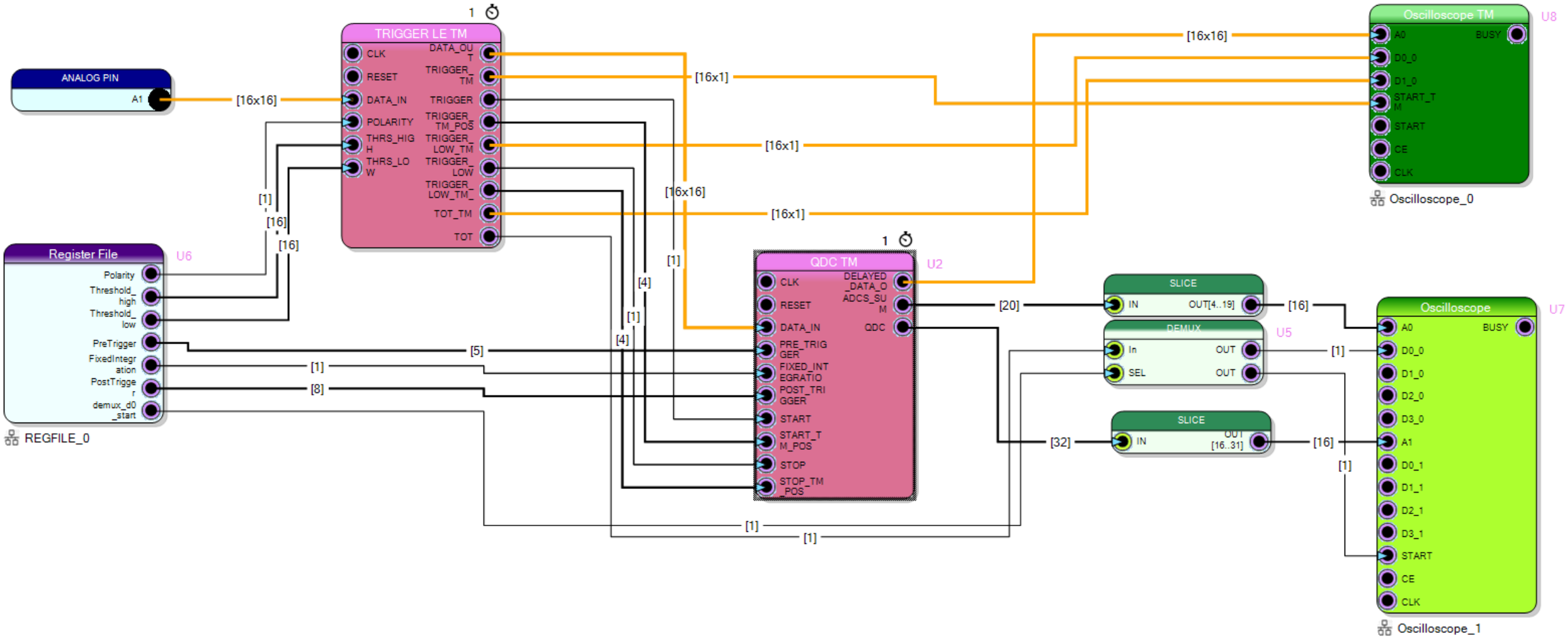
Analog Output:

- 8 x 10 Gsps, 14bit

- Programmable oscilloscope-like analog front-end
- Fully supported by Sci-Compiler
- Integrated solid-state disk for long time (up to hours) acquisition
- Ethernet and USB3 connectivity (optical optional)

UPCOMING SYSTEM: DIGITAL CHARGE INTEGRATION @ 5GHz

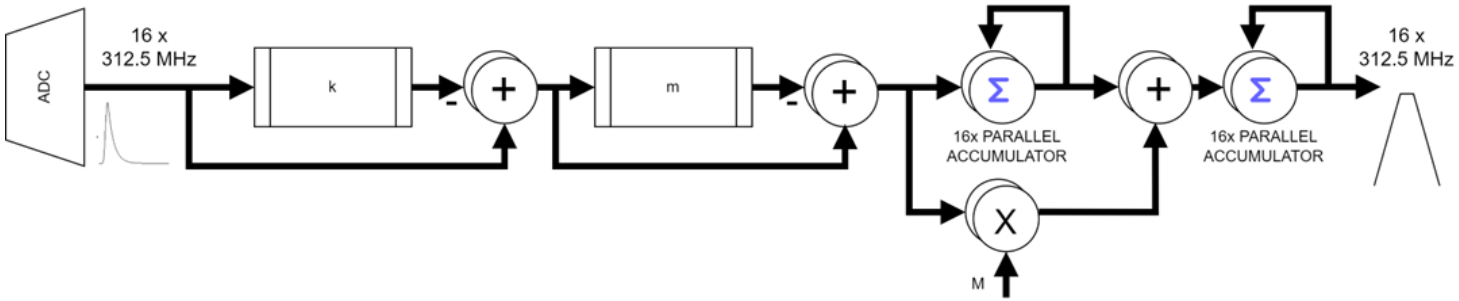
PRELIMINARY



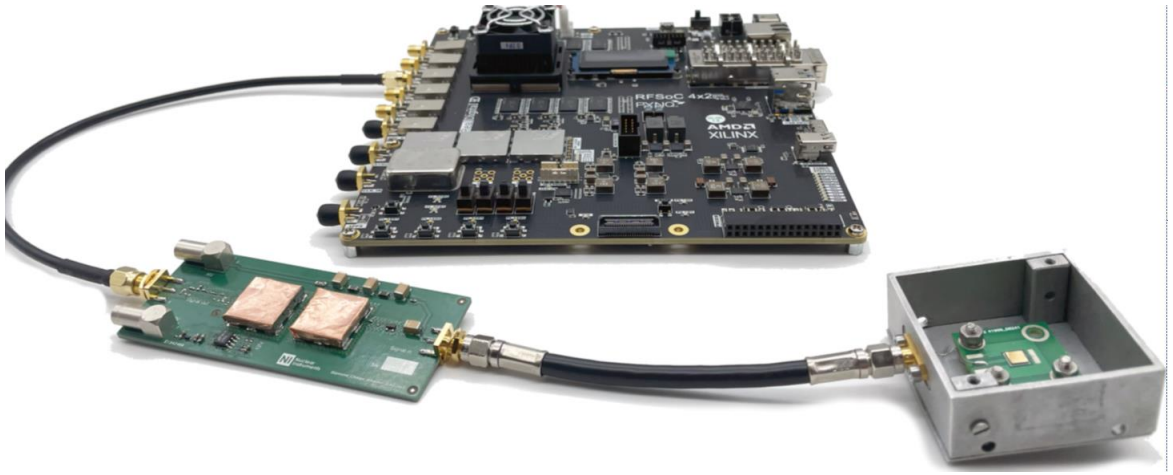
UPCOMING SYSTEM: TRAPEZOIDAL PHA @ 5GHz

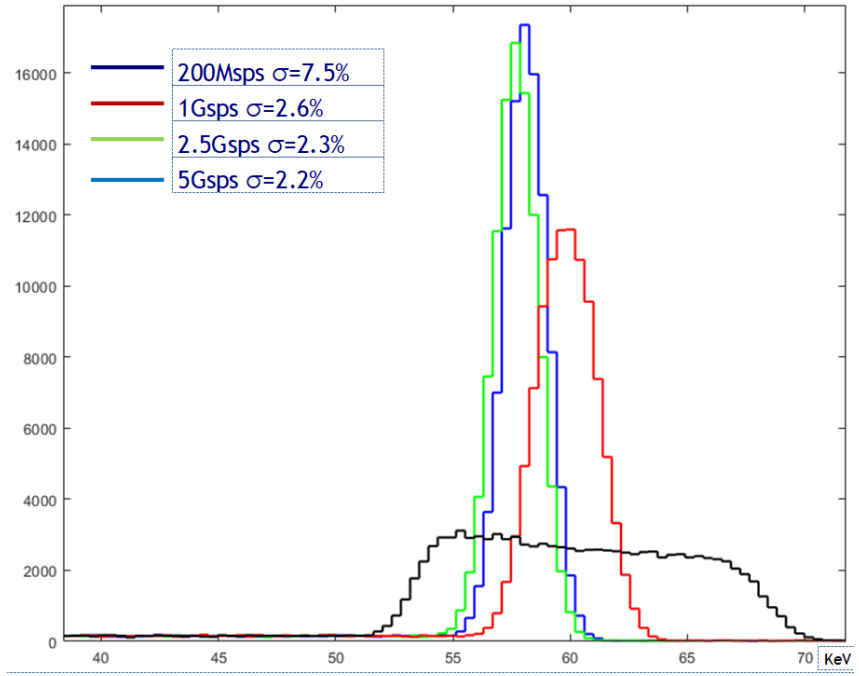
PRELIMINARY

Parallelized version of Trapezoidal Filter available in Sci-Compiler for new ultra-high-speed digitizer



Diamond detector + Custom InGAs Amplifier + Xilinx RFSoC





Implementation of multi-GHz digital shaper for high-rate nuclear spectroscopy – *A. Abba*