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The Level-1 Topological Processor for ATLAS Phase-I upgrade and its firmware evolution for use within the Phase-II Global Trigger

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The increased instantaneous luminosity of the LHC in Run 3 brings the need for the upgrade of the ATLAS trigger system. The newly commissioned Phase-I L1Topo system, which replaces its Phase-0 predecessor, processes data from the Feature Extractors (FEXes) and the upgraded Muon to Central Trigger Processor Interface (MUCTPI) to perform topological and multiplicity triggers. The L1Topo system consists of three ATCA modules, each hosting two processor FPGAs (Xilinx Ultrascale+ 9P). The L1Topo firmware is composed of a large number of sort/select, decision, and multiplicity algorithms, that are automatically assembled and configured based on the provided trigger menu. For the HL-LHC, the Phase-I L1Topo system will be replaced by a Global Trigger, a time-multiplexed system, which concentrates the data of a full event into a single FPGA. In order to match the new operational environment, the fully synchronous, very low latency (new data arriving every 25 ns), parallel implementation (˜2.5m LUTs) of the Phase-I Topological firmware is being adapted to a significantly higher latency budget (new data arriving every 1.2 us) and a substantially tighter resource budget (˜100k LUTs). The main challenge is to allow for multiple working points of the utilized resources and latency for each algorithm. A detailed overview of the Phase-I L1Topo hardware and firmware is provided. Preliminary performance results achieved by the Phase-I L1Topo together with a description of the challenges found during the commissioning process are included. Phase-II related firmware adaptations are also discussed.

Minioral

Yes

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No

Are you a student?

No

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