L1Topo: The Level-1 Topological Processor for ATLAS Phase-I upgrade and its firmware evolution for use within the Phase-II Global Trigger

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PRISMA Cluster of Excellence

BMBF-Forschungsschwerpunkt ATLAS-EXPERIMENT FSP 103 ATLAS Physik bei höchsten Energien mit dem ATLAS-Experiment am LHC

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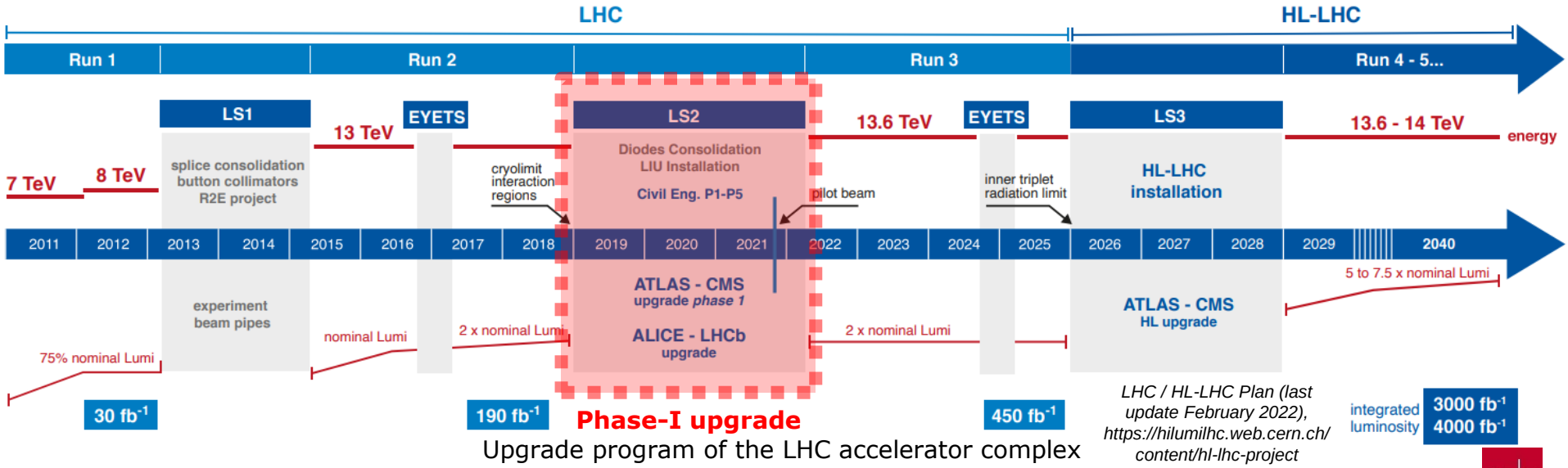
Phase-I Upgrade of the ATLAS detector

- The Phase I upgrade took place during the Long Shutdown 2: 2019-2022
- The following Run 3 is in operation: 2022 to 2025
- Peak luminosity of $2x10^{34}$ $cm^{-2}s^{-1}$

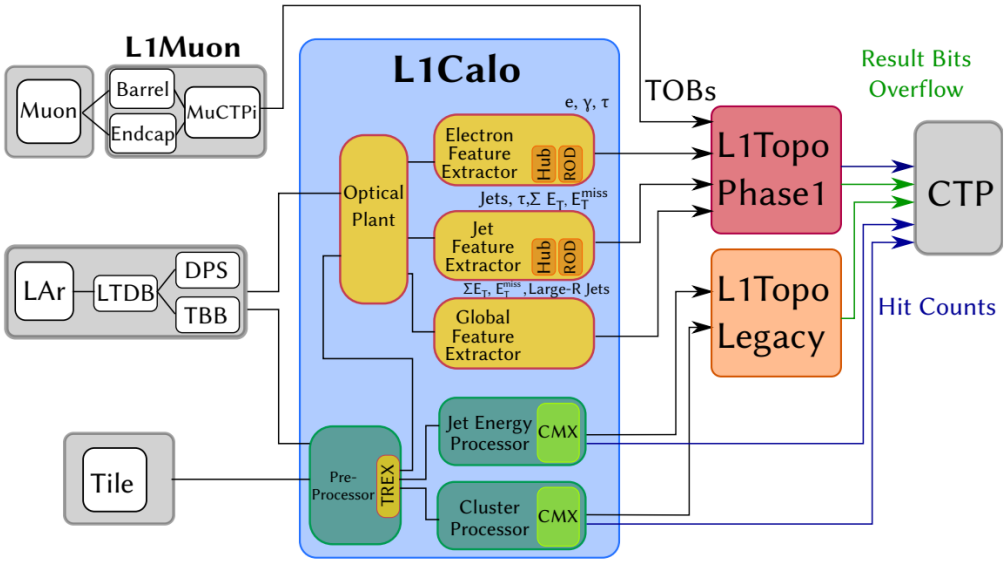


Upgrade program of the LHC accelerator complex

LHC / HL-LHC Plan (last update February 2022), https://hilumilhc.web.cern.ch/content/hl-lhc-project

Phase-I Level-1 Trigger System

- The increased instantaneous luminosity of the LHC in Run 3 → upgrade of the ATLAS trigger system is necessary
- Phase-I Level-1 Trigger System
  - Performs real time event selection
  - Reduces the event rate: 40 MHz → 100kHz
  - Staying below the maximum readout rate of the ATLAS detector
  - Overall system latency budget 2.5 μs

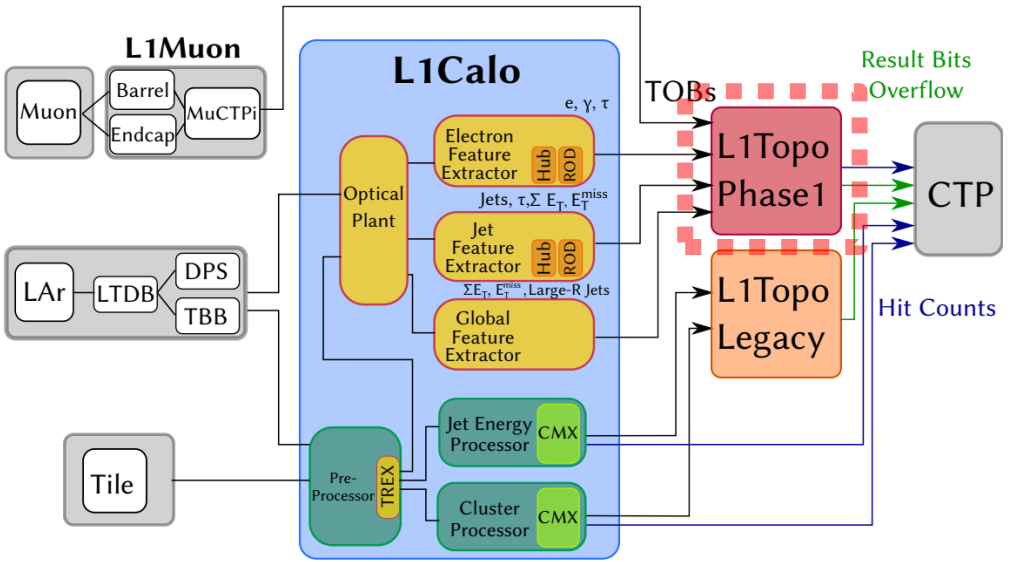


A block diagram of the Level-1 trigger system after the Phase-I upgrade

ATLAS Collaboration, "Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System", CERN-LHCC-2013-018

Phase-I L1Topo system: Functionality

- As part of the Level-1 trigger system, the Level-1 topological trigger (L1Topo) processes data on the **real-time** data path from the individual Feature Extractors (FEXes) and the upgraded Muon to Central Trigger Interface (MUCTPI) to perform topological triggers as well as triggers, counting number of objects
- Provides high processing capabilities in order to make use of the input objects with increased granularity from the new FEXes and the MUCTPI



A block diagram of the Level-1 trigger system after the Phase-I upgrade

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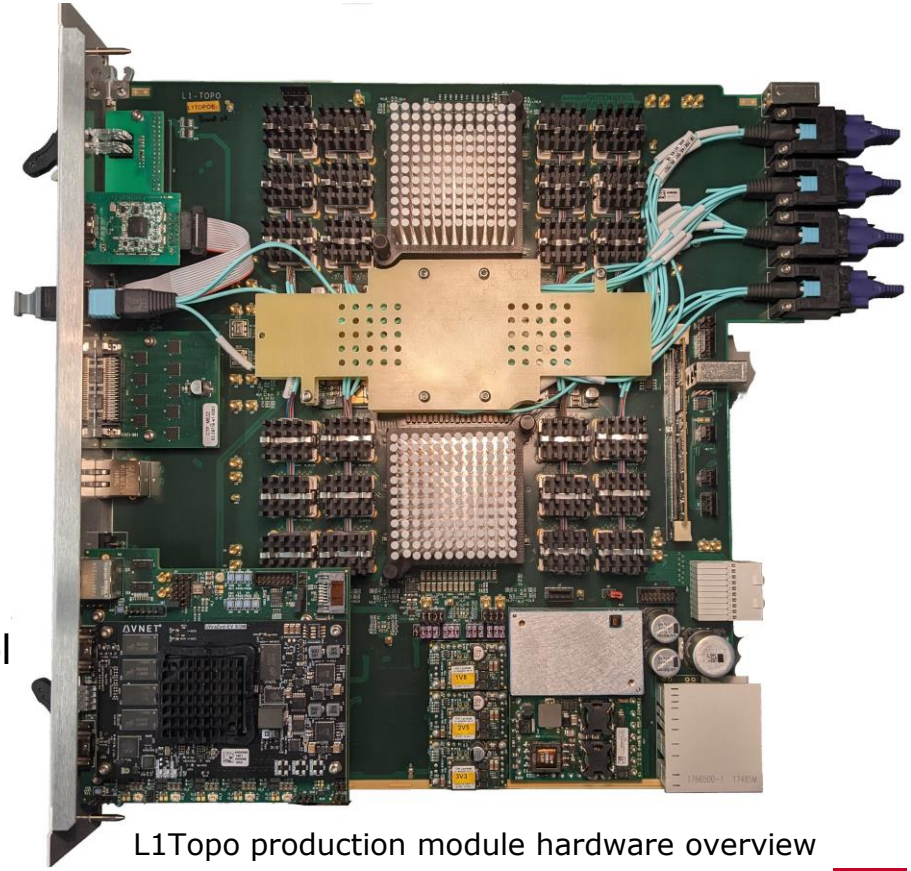
Phase-I L1Topo system: Hardware

- The L1Topo system consists of three ATCA modules
  - Each hosting two processor FPGAs: Xilinx Ultrascale+ 9P
- High-speed optical transceivers: Avago MiniPODs
  - Support data transmission at speeds up to 11.2 Gb/s per link
- Zynq based control mezzanine
  - Configuration, monitoring, slow control
- Similar hardware building blocks as on the jFEX module

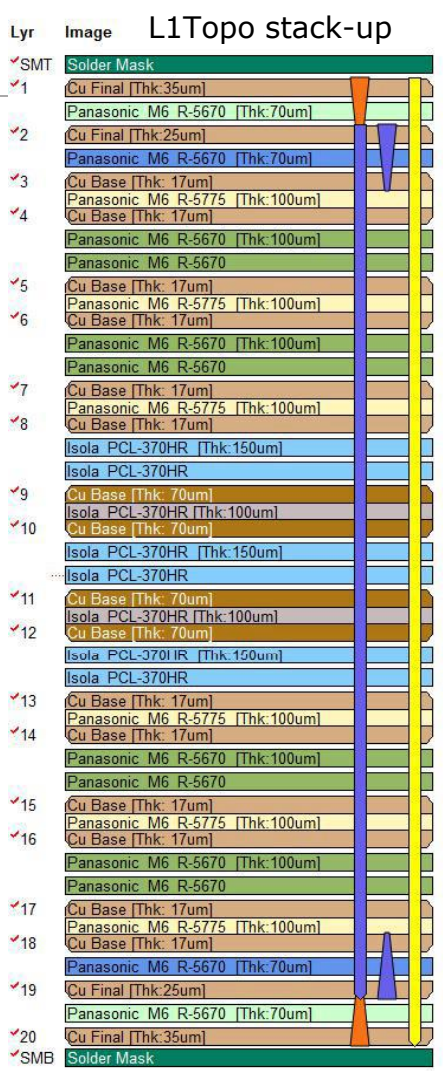


L1Topo production module hardware overview

Phase-I L1Topo system: Signal Integrity

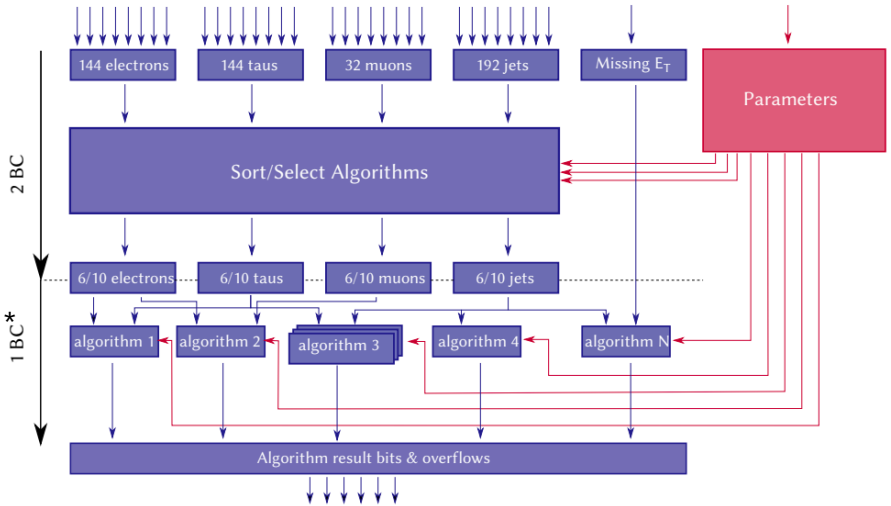
- High-speed PCB design routing techniques
  - High-speed differential pairs adhere to strict physical and spacing constraints
  - Staying within the phase tolerance limit: phase tuning performed
  - Achieving a required differential impedance: in-pair spacing and trace width controlled
  - Minimizing the crosstalk: spacing sufficiently larger than the in-pair spacing used across all pairs

- The high speed stack-up design
  - Minimizing the crosstalk: signal planes shielded by the ground planes
  - Avoiding stubs on the signal lines: high-speed signals occupy the top and bottom inner layers and use microvias
  - Good dielectric constant and dissipation factor for high frequencies: ultra-low transmission loss and highly “heat resistant” PCB material (MEGTRON6) used



Phase-I L1Topo system: Firmware

- LHC Bunch Crossing synchronous firmware – new event data every 25 ns
- “Select” algorithms select all Trigger Objects (TOBs) passing configurable parameter-based threshold
- “Sort” algorithms output a list of the leading TOBs with the highest Transverse Energy (ET), that pass the thresholds, and sort them by ET
- “Decision” algorithms perform calculations for one or more lists of TOBs, including angular differences, invariant masses, large jet reclustering, and missing transverse energy



L1Topo “Sort/Select” and “Decision” algorithms structure

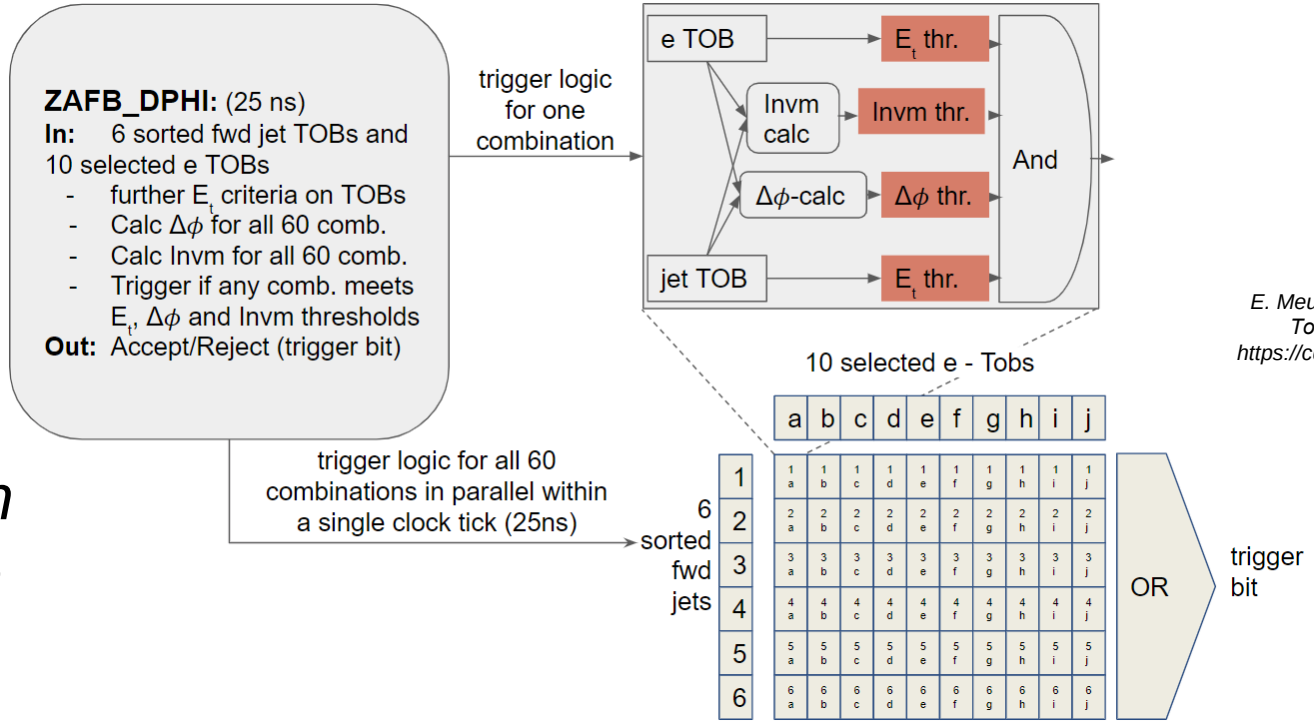
* 1 BC ~ 25 ns
BC (Bunch Crossing) – collision between the particle beams

J. Damp, “Search for Dijet Resonances with the Level-1 Topological Processor at ATLAS”, PhD thesis: Johannes Gutenberg-Universität Mainz, 2020

Phase-I L1Topo system: Firmware

- **1 BC (25 ns) – very tight latency budget** for Decision algorithms → full parallelization required
- High resource usage as a consequence: **2.5M LUTs** across 6 FPGAs

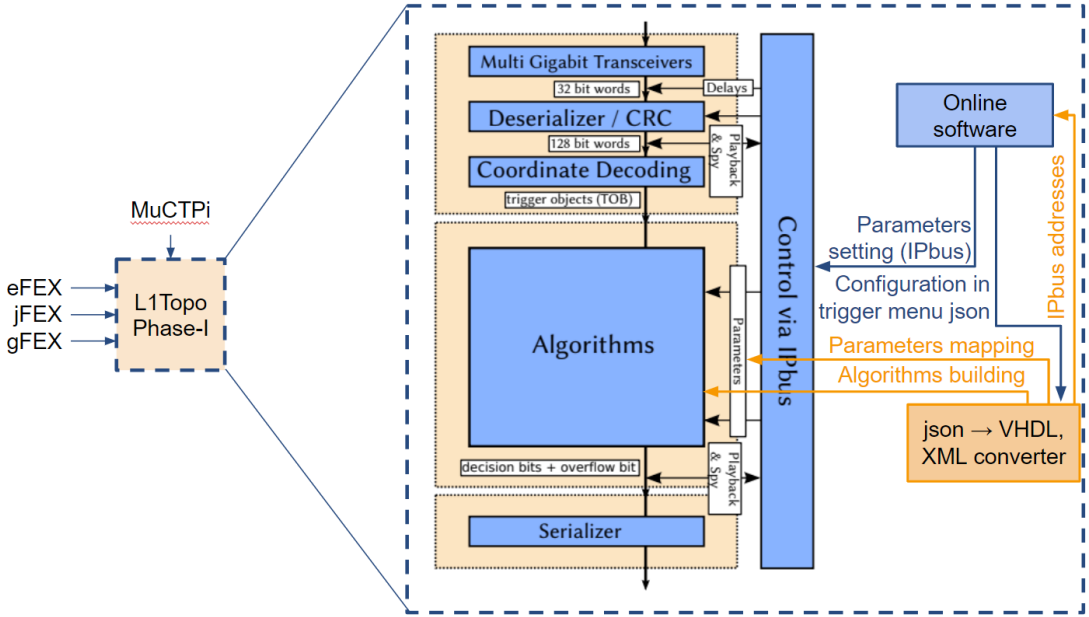
Algorithm Example



E. Meuser, "The ATLAS Level-1 Topological Processor", https://cds.cern.ch/record/2869237

Phase-I L1Topo system: Firmware

- The algorithms are automatically assembled and configured based on the provided trigger menu
- The algorithm parameters can be set and changed via the IPBus by the Online Software during a Run
- The topological trigger configuration is fully described in



in a single menu-driven json file, from which algorithm VHDL code, as well as IPbus address mapping, are automatically generated

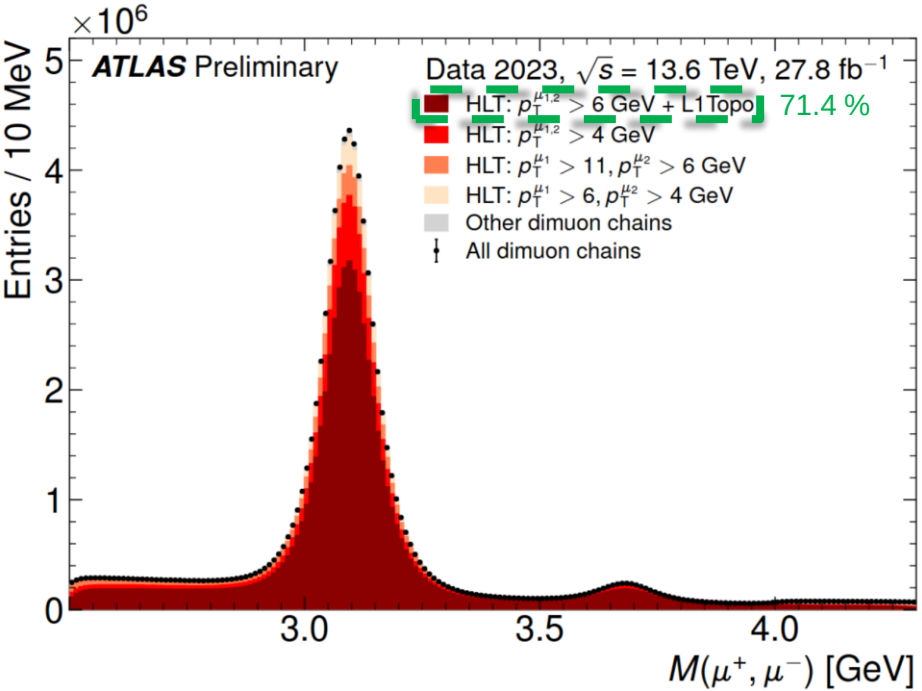
- Consistency between the firmware and the software is ensured
- Menu change may require a firmware rebuild, leaving little time for testing

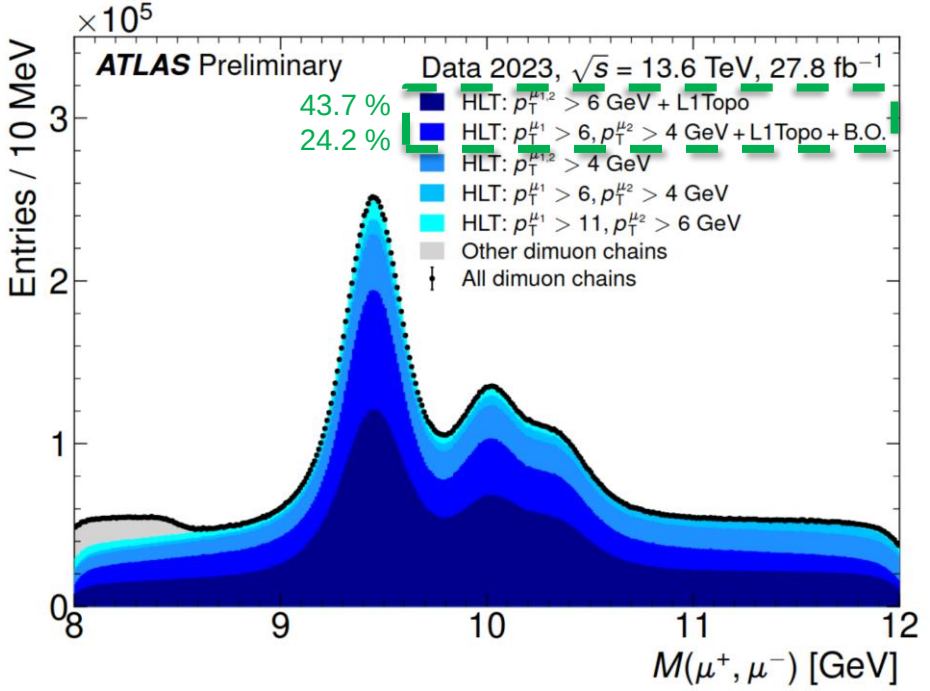
Phase-I L1Topo system: Commissioning

- The Phase-I L1Topo system has been fully commissioned with the rest of the new L1 trigger systems in ATLAS
- Main commissioning challenges due to 4 different input sources
  - Different input format of TOBs
  - Different granularity of TOB coordinates
  - Complicated detectors' geometry
  - Different time of TOBs' readiness
- Comparison against software implementation
  - Debugging with playback / spy
  - High statistics continuous online monitoring
- The Phase-I L1Topo system has come into routine operation taking data in 2024

Phase-I L1Topo system: First performance results

- L1Topo chains provide about 70 % of unique rate for J/Ψ and ϒ candidates

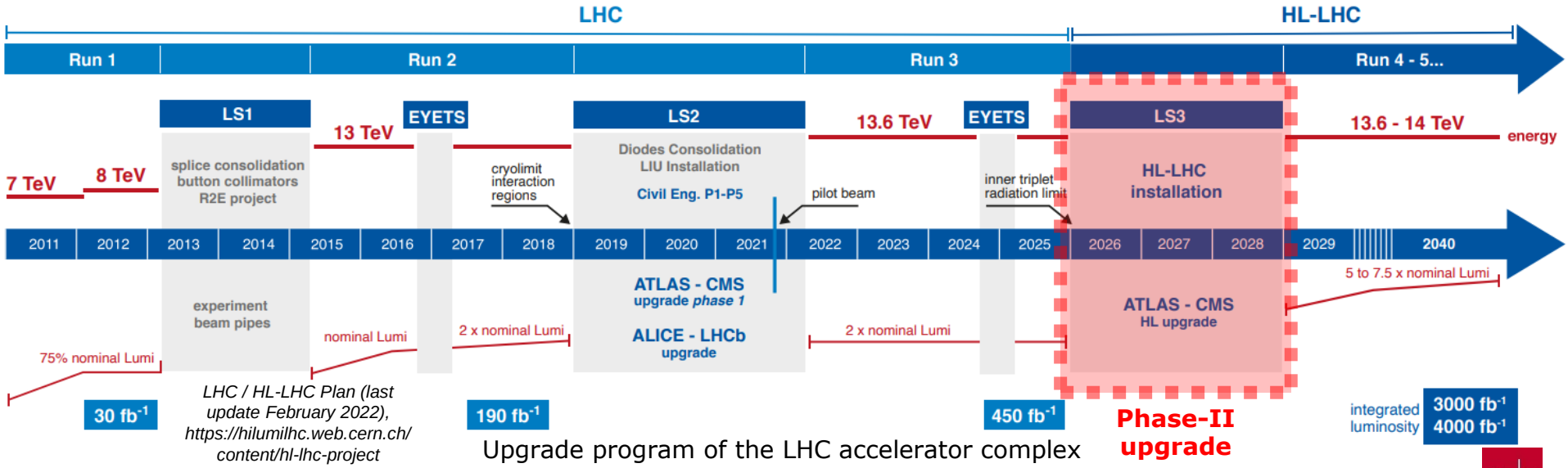




https://twiki.cern.ch/twiki/bin/view/AtlasPublic/BPhysicsTriggerPublicResults

Phase-II Upgrade of the ATLAS detector

- The Phase II upgrade is planned during the Long Shutdown 3: 2026-2029
- The following Runs 4 and 5 will be in operation: 2029 to 2040
- Peak luminosity of 7.5×10^{34} $cm^{-2}s^{-1}$



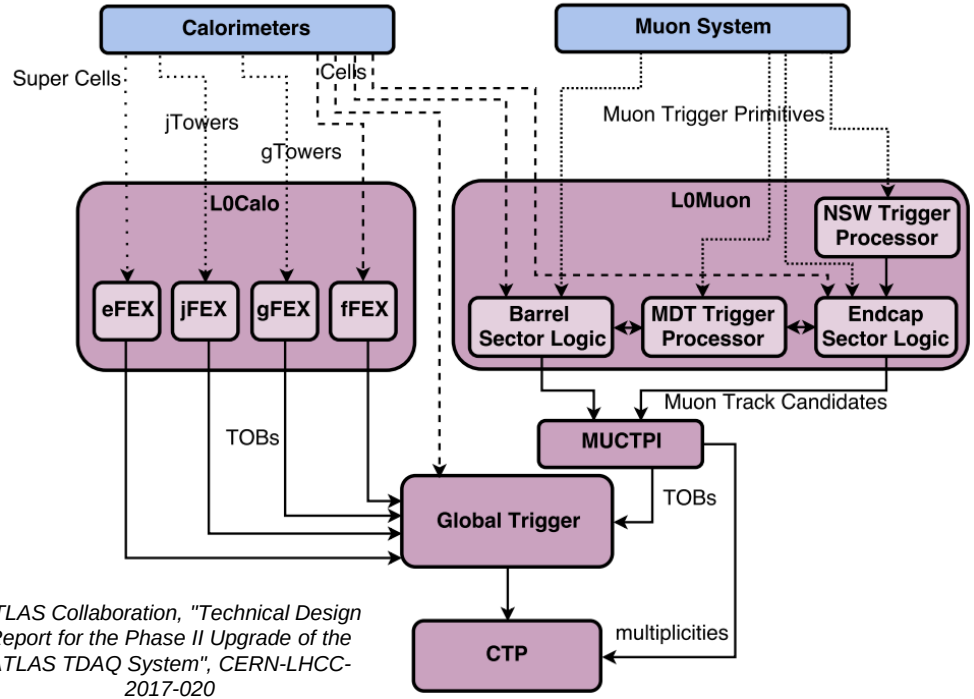
LHC / HL-LHC Plan (last update February 2022), https://hilumilhc.web.cern.ch/content/hl-lhc-project

Upgrade program of the LHC accelerator complex

Phase-II Global Trigger system: Functionality

- The instantaneous luminosity of the LHC in Run 4 is significantly increased → further upgrade of the ATLAS trigger system is necessary

- Phase-II Level-0 Trigger System
  - Overall system latency budget increased from 2.5 to 10 μs
  - Level-0 accept rate increased from 100 kHz to 1 MHz

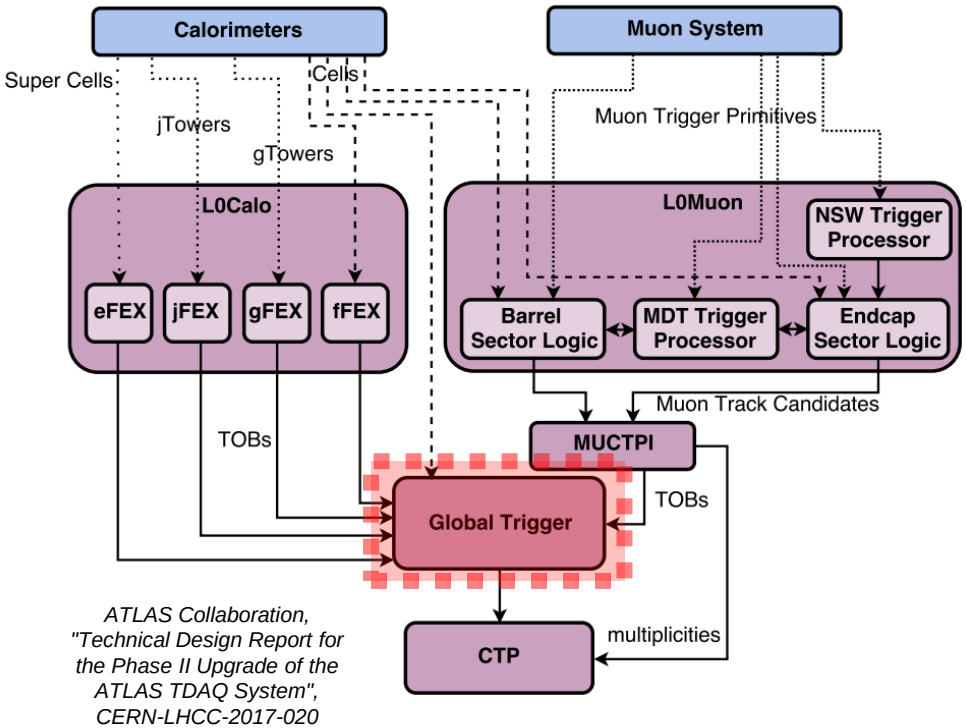


ATLAS Collaboration, "Technical Design Report for the Phase II Upgrade of the ATLAS TDAQ System", CERN-LHCC-2017-020

A block diagram of the Level-0 trigger system after the Phase-II upgrade

Phase-II Global Trigger system: Functionality

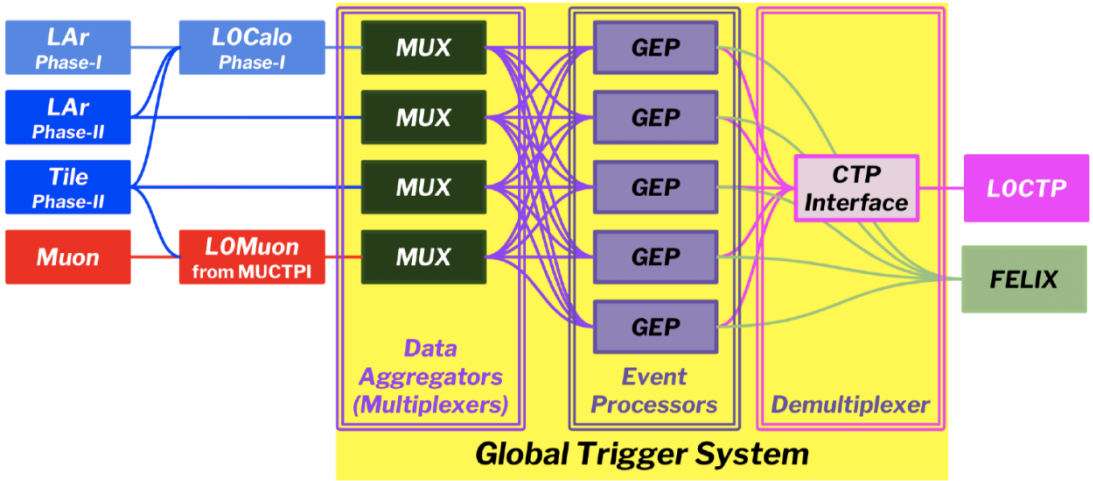
- As part of the Phase-II Level-0 Trigger System, the Global Trigger **replaces** the Phase-I Topological Processor
- The Global Trigger will absorb the functions of the Phase-I Topological Processor and **significantly extend** them
  - Uses full-granularity calorimeter cells to perform offline-like algorithms
  - Identifies topological signatures
  - Processes the trigger information from the Run 3 hardware systems
  - Transmits the processed trigger information to CTP for final decision



A block diagram of the Level-0 trigger system after the Phase-II upgrade

Phase-II Global Trigger system: Implementation

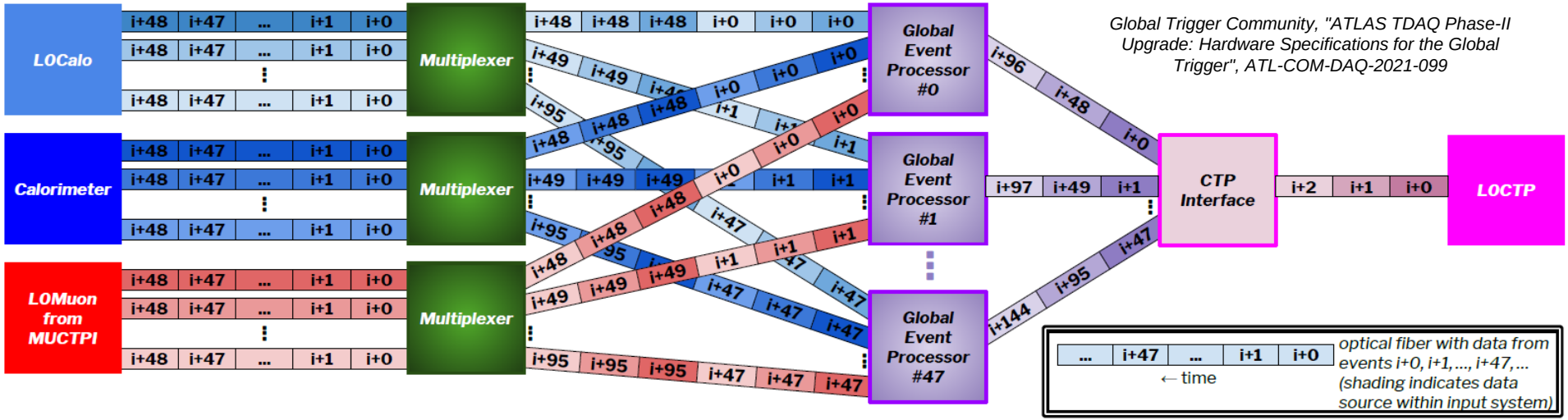
- Time-multiplexed system concentrates data of full event into a single processor
- Composed of 3 main layers
  - Multiplexing (MUX) layer
  - Global Event Processor (GEP) layer
  - Demultiplexing Global-to-Central Trigger Processor (CTP) Interface
- Will provide a synchronous interface to the rest of ATLAS detector



ATLAS Collaboration, "Technical Design Report for the Phase II Upgrade of the ATLAS TDAQ System", CERN-LHCC-2017-020

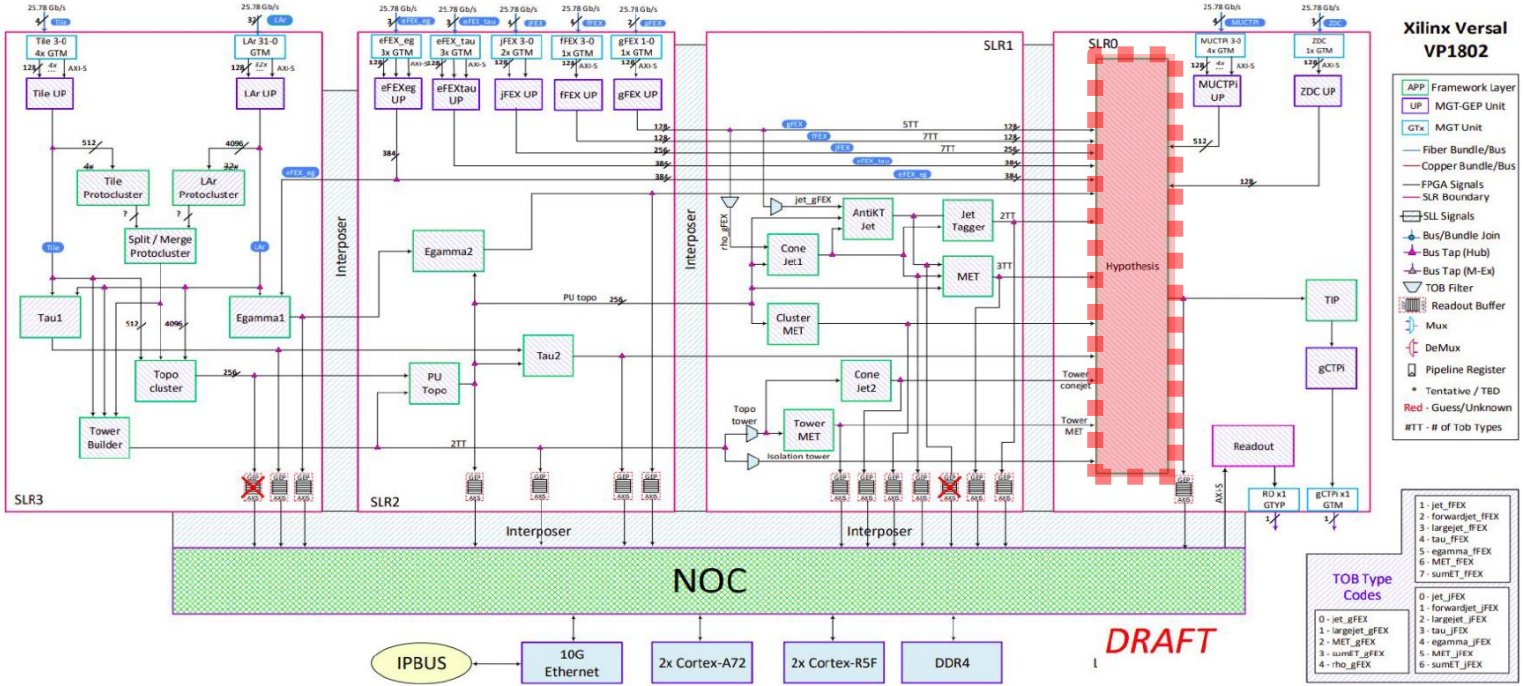
Phase-II Global Trigger system: Implementation

- 48 MUX nodes receive **real time** data from L0Calo, Calorimeter and MuCTPi every BC and transmit a full event to a single GEP node every BC
- As a result, the latency budget for each event processor is 1.2 μs



Phase-II Global Trigger system: Topo algorithms

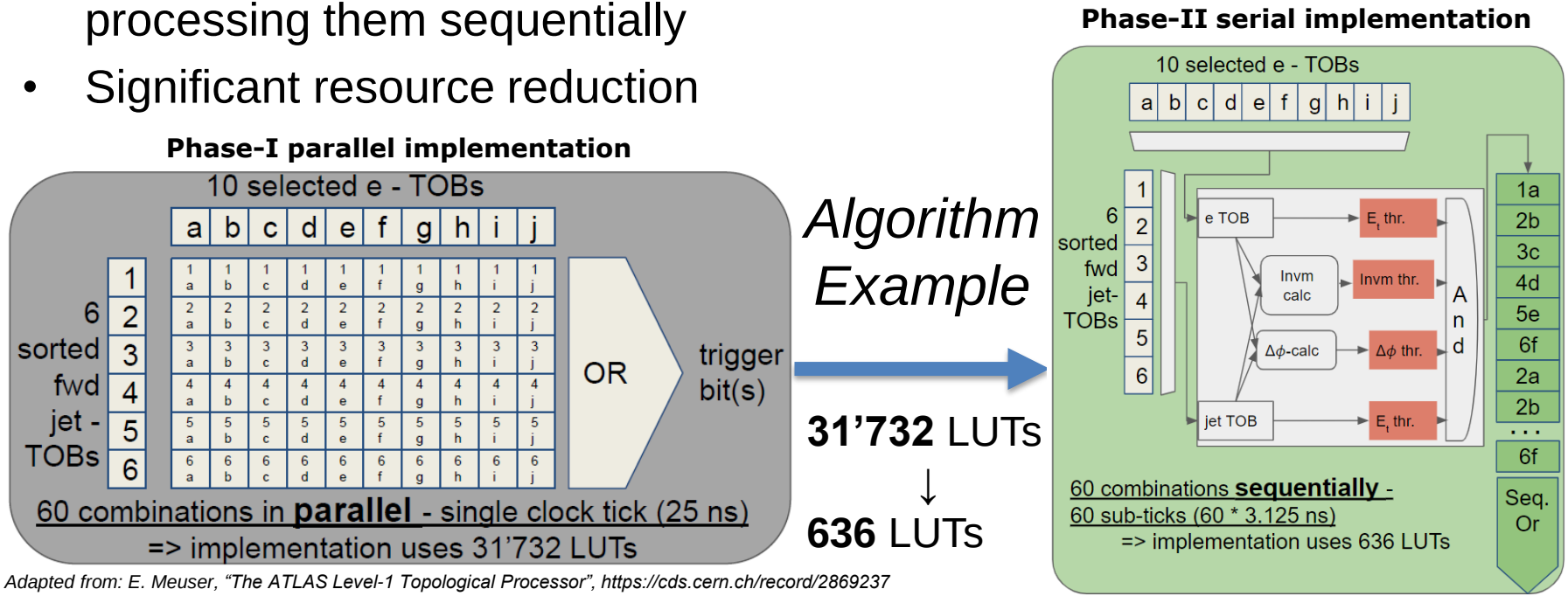
- Abundance of algorithms within the GEP node in order to process the full event data
- Even though Topo algorithms' block in Phase-II has significantly higher latency budget, it is only allowed to occupy a maximum of **100k LUTs**



Jeff Eastlack

Phase-II Global Trigger system: Topo algorithms

- Main strategy – fitting within the tight resource budget at a cost of higher latency
- Instead of processing all combinations in parallel in a single clock tick, processing them sequentially
- Significant resource reduction



Adapted from: E. Meuser, "The ATLAS Level-1 Topological Processor", https://cds.cern.ch/record/2869237

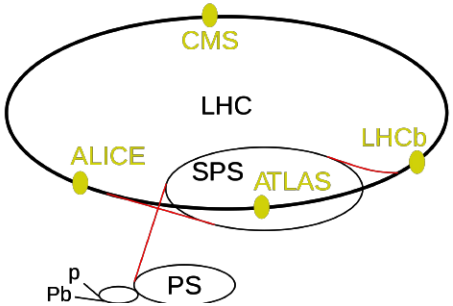
Conclusion

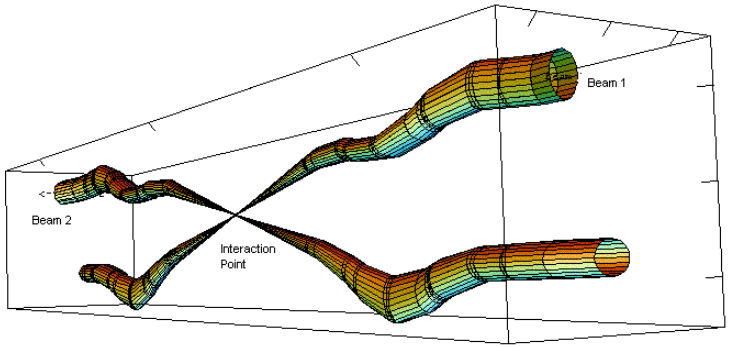
- Performing topological and multiplicity triggers, the L1Topo system is an essential component within the ATLAS Level-1 trigger system
- The Phase-I L1Topo system hardware and firmware has been developed in order to process the data from the FEXes and the MUCTPI
- The Phase-I L1Topo system has been fully commissioned and come into routine operation taking data in 2024
- The Phase-I Topological firmware is being adapted for use within the Global Trigger System, taking into account the new resources and latency envelope of the Phase-II upgrade

Backup

ATLAS detector

- Particle beams collide every 25 ns (frequency of 40 MHz)
  - Bunch Crossing – time between the collisions (25 ns)





Relative beam sizes around IP1 (Atlas) in collision