Contribution ID: **54** Type: **Oral presentation**

Integration of Hardware Acceleration Techniques in Real-Time Framework using FPGAs devices

Monday 22 April 2024 15:25 (20 minutes)

This contribution explores the feasibility of using high-level C/C++ like languages to achieve the integration of specified FPGAs-based applications with the function blocks of the ITER Real-Time Framework (RTF). RTF enables the development, deployment and execution of instrumentation and control (I&C) applications optimized for real-time performance on ITER CODAC Core System. High Level Synthesis (HLS) and OpenCL are high-level synthesis languages that allow users to implement complex algorithms on FPGA deevices using C/C++ programs. From this perspective, using FPGAs allows to increase the computational power limiting the latencies of a specified functional block that is run in RTF. The proposal presented notably reduces development time and maintenability compared to the solutions based on Hadware Description Languages, such as VHDL or Verilog.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

Author: GONZALEZ BRITO, Cesar (Universidad Politécnica de Madrid)

Co-authors: Prof. RUIZ, Mariano (Universidad Politécnica de Madrid); Dr CARPEÑO, Antonio (Universidad Politécnica de Madrid); Mr PIÑAS HIGUERUELA, Alejandro (Universidad Politécnica de Madrid); Mr COSTA, Víctor (Universidad Politécnica de Madrid); Dr NIETO VALHONDO, Julián (Universidad Politécnica de Madrid); Prof. BARRERA, Eduardo (Universidad Politécnica de Madrid)

Presenter: GONZALEZ BRITO, Cesar (Universidad Politécnica de Madrid)

Session Classification: Mini-Orals, Orals Presentations

Track Classification: Real Time Diagnostics, Digital Twin, Control, Monitoring, Safety and Security