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Type: Oral presentation

Development and test of a 48-optical ports high precision clock distributor board

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High precision clock distribution is of primary importance for the accurate synchronization of distributed detectors in medium to large-scale physics experiments and in some other scientific instruments as well. Common techniques for distributing a reference clock to a large number of end-points often rely on high-speed serial transceivers embedded in Field Programmable Gate Arrays and use precision phase measurements methods to track, and eventually compensate, distribution delay variations. White Rabbit is a well-known solution that combines these techniques with Ethernet technology. This work explores an alternative approach to clock distribution, specifically in view of the Hyper Kamiokande experiment. We report the design and test of a cascable 48-optical port clock distributor in 1U x 19" standard form-factor. The central element is a commercial System on Module equipped with a Xilinx Zynq UltraScale+ device. Superior port density compared to other designs is reached by using the large available number of ordinary differential I/O pairs instead of the limited count of high speed SerDes. This approach comes at the expense of lower link bandwidth. We detail the concepts and the difficulties of designing fixed-latency high-speed serial communication using ordinary FPGA I/O's and we investigate interoperability with dedicated multi-gigabit FPGA SerDes. We explain how to implement precise clock round-trip latency measurements with the proposed links. We present characterization measurements obtained with this demonstrator and show its main figures of performance. Finally, we outline how these studies will serve to construct Hyper Kamiokande's final clock distribution system.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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