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Software-Assisted Event Builder for Belle II Experiment

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In this paper, we present the design of the hybrid event builder algorithm for the Belle II DAQ. The event builder is implemented in PCIe40 FPGA boards and reads up to 48 127 MB/s channels per board. The first version of the event builder impemented the algorithm entirely in the firmware of the FPGA. But due to limited onboard memories, there are hard limitations on the operation conditions. The new algorithm employs independent event processing for each channel in FPGA, and a highly-optimized read-out software for final event building. This allowed us to increase the throughput of the system from 600 MB/s to 3 GB/s on a read-out computer with 20 CPU cores. The system is currently being commissioned and will be used in the upcoming data taking period starting in December 2023.

Minioral

No

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No

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