A Design of Clock and Timing System Prototype for Hard X-ray FEL Facility

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Introduction

Shanghai Hard X-ray Free Electron Laser Facility (SHINE) is the first high repetition-rate X-ray free electron lasers facility in China. Based on an eight GeV CW SCRF LINAC, the facility is built in a 3.1 km long tunnel underground at Zhang-Jiang High Tech Park, which can generate X-ray pulses in the photon energy range from 3 keV to 25 keV. In SHINE, the clock and timing system plays a crucial role. The distributed clock of multiple diagnostic and control device need not only a high quality and stability but also an ability of high precision automatic phase synchronization. In the existing accelerator devices, the clock and timing systems use electrical signal for clock distribution, which cannot achieve the mixed transmission of data and commands and the automatic phase compensation. The White Rabbit (WR) precise time protocol (PTP) is an implementation of PTP in synchronous Ethernet optical fiber networks, which can achieve multi-node precision clock synchronization for sub-nanosecond levels within a range of 10 km. However, the WR PTP is based on the standard network protocol with a 125 MHz time base, which does not match the special mechanical frequency of SHINE. Based on the standard WR PTP, this design presents a customized time synchronization protocol running at the frequency of about 135.417MHz (135 times of the machine clock in SHINE). Meanwhile, in order to meet the complex requirements of different devices in SHINE, we also proposed a high precision clock shaping method to achieve flexible clock delay and duty cycle adjustment in this system.

Design of the clock and timing system

1) Structure of the clock and timing system. As shown in Fig.1, the clock and timing system mainly consist of three parts: the master node, WR switch and the slave node. Similar to the normal WR clock systems, the master node or grandmaster WR switch will receive reference clock signal including reference clock and related pulse per second (PPS) signal. According to the top-down network synchronization structure of WR PTP, the slave node will automatically compensate the phase difference with the upper WR switch. Meanwhile, each slave node electronics connect to other SHINE's devices through the FMC interface, sending the synchronous clock, data and commands.

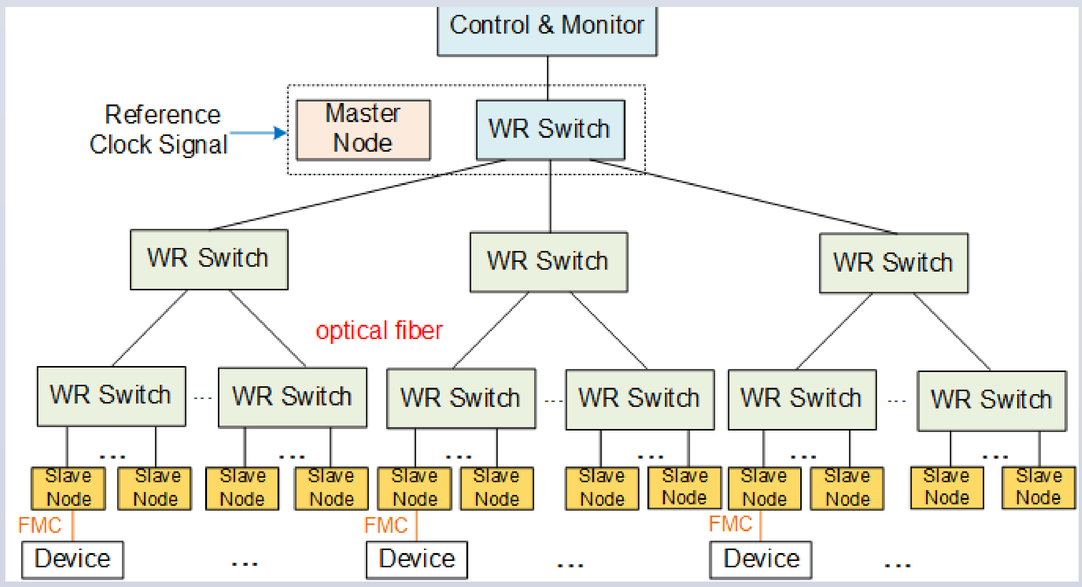

Fig.1. Structure of the clock and timing systems

2) Slave node electronics. As the crucial part in the clock and timing system, the slave node will complete the automatic phase compensation and flexible clock processing. The details is shown in Fig.2. As mentioned above, the slave node mainly has two part peripheral circuits besides the FPGA: the WR clock recovery system (CRS) and the clock processing circuits (CPC).

The customized WR CRS is similar to that of standard WR and the phase adjust PLL provides WR reference clock signal with special frequency. The other circuits, including two fan-out PLL, 12-channels D Flip Flop (DFF), combining with the related logic in FPGA, complete the flexible clock processing functionality. Using the peripheral circuits of the PLLs and DFFs aims to ensure the high quality of the distributed machine clocks that are finally sent to devices through FMC interface. In addition, the fan-out PLL can also accomplish multi-channel fine delay adjustments with a step of about 400 ps.

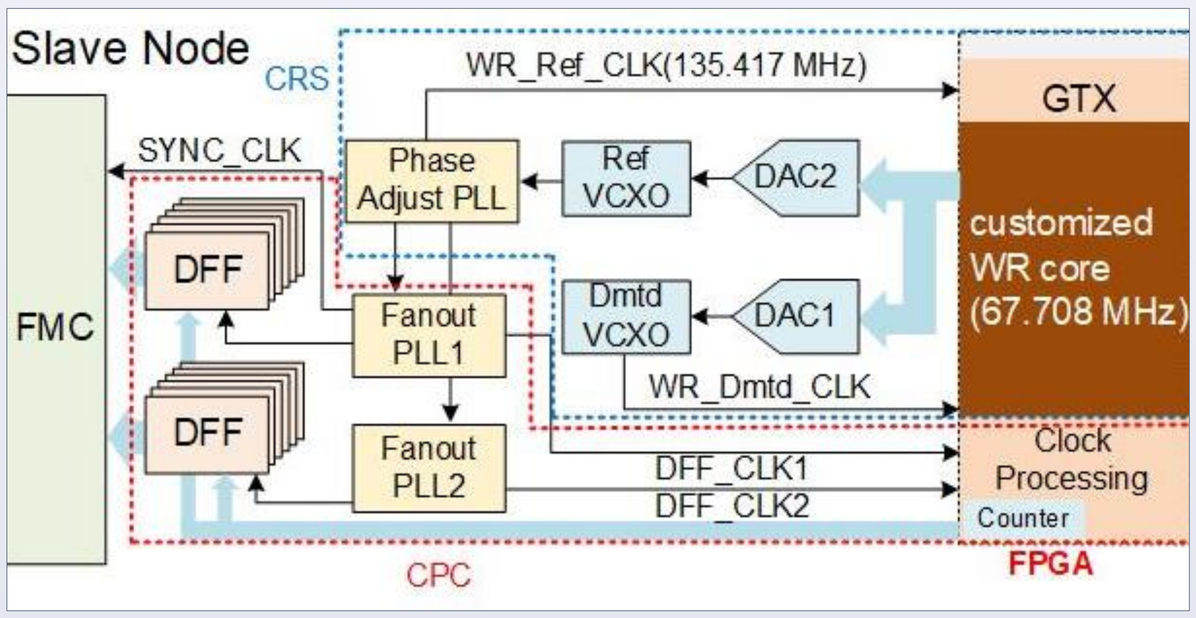

Fig.2. Block of the slave node

3) Master node electronics. The master node electronics can be configured as the WR grandmaster model or the slave model. Its main task is to send the control commands or information through the WR network. The circuit structure of master node is similar to the slave node. We do not repeat the details no more here.

Testing Results

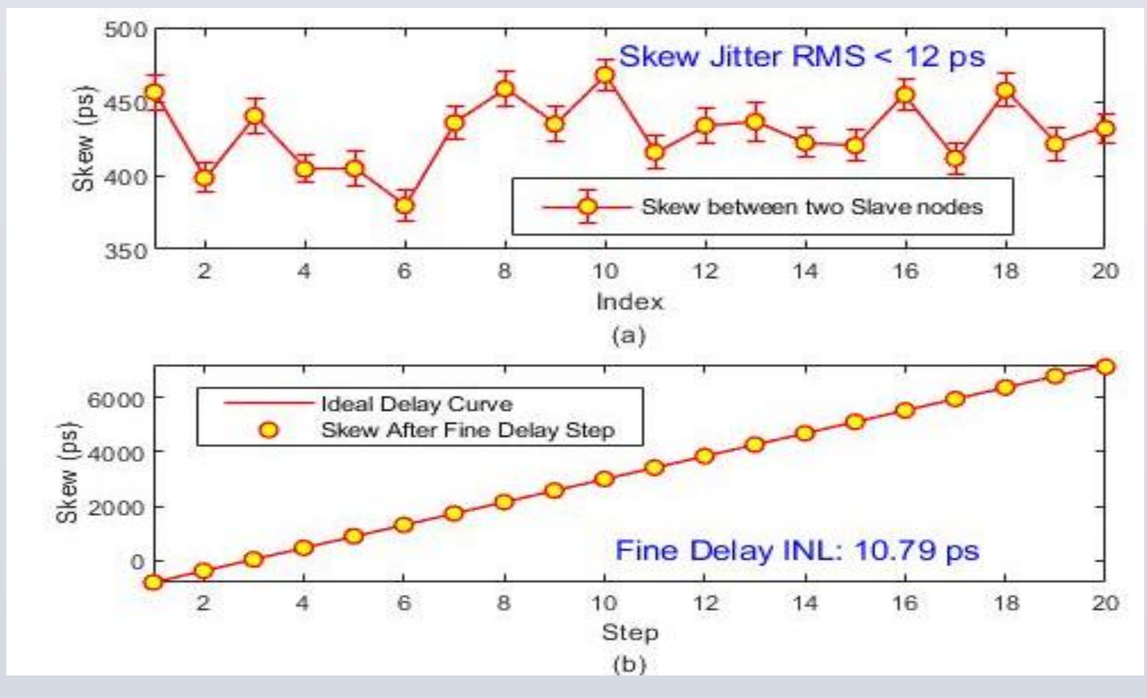

Fig.3. (a) Skews between two slaves after powering up and down multiple times (b) Phase adjustment test of fine delay

In order to evaluate the performance of automatic phase compensation, we powered up and down the whole prototype circuits 20 times. Shown in Fig. 3(a). is the skews of the synchronous machine clock in two slave nodes. The results indicate that the skew jitter RMS of distributed clock is less than 12 picoseconds and the peak-to peak skew varies within the range of 120 picoseconds after powering up and down multiple times.

Meanwhile, we also tests the clock phase delay of the prototypes. Fig. 3(b). presents the test results of the fine delay. With the fine delay circuits, we can achieve about fine delay with the step of about 400 picoseconds in a coarse clock cycle and the INL of the fine delay is less than 15 ps.

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