A Low-power VCSEL Driving Structure Implemented in a 4 x 14-Gbps VCSEL Array Driver

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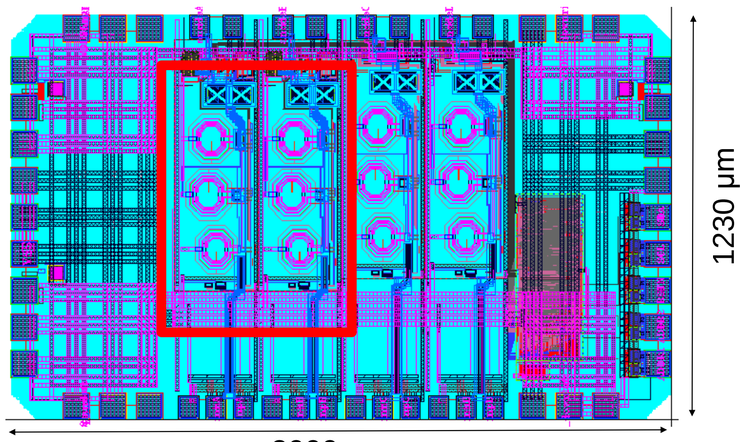
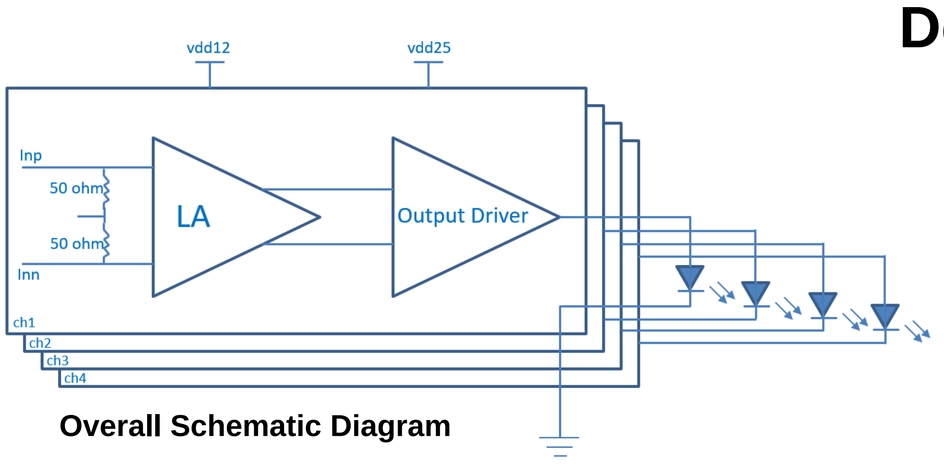


4 x 14- Gbps/ch VCSEL Array Driver

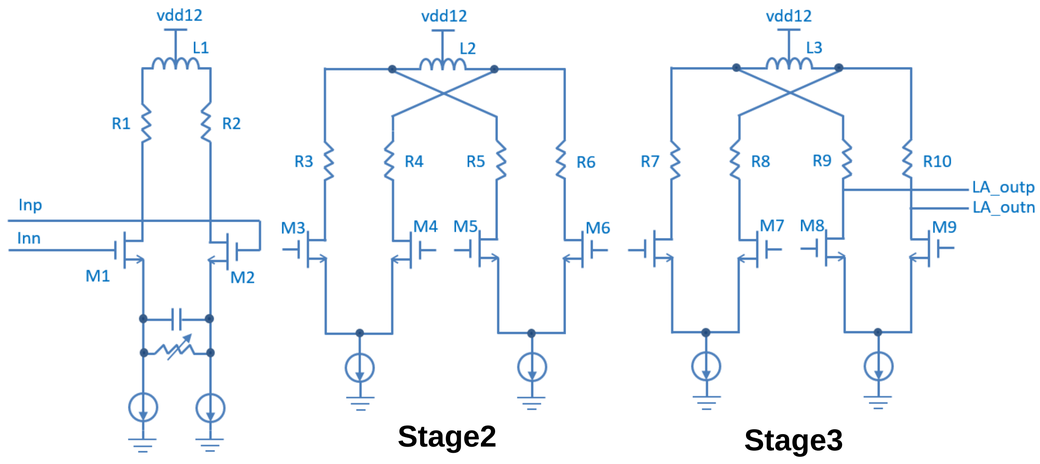
Introduction

- A 4-channel, 4 x 14-Gbps VCSEL array driver ASIC, has been designed and fabricated in a commercial 65nm CMOS technology for the potential applications such as detector front-end readout in particle physics and related fields.
- Two different designs are integrated in the chip, and the proposed design is located in the first two channels. It features a novel low-power output structure, and achieves a 44 mW/ch power consumption when delivering a 2 mA ~7 mA output current to the VCSEL at a data rate of 14 Gbps.
- The die measures 2000 µm x 1230 µm. The die was wire bonded to the VCSEL array, and integrated within the array optical module. The proposed design has been fully tested.

Designs

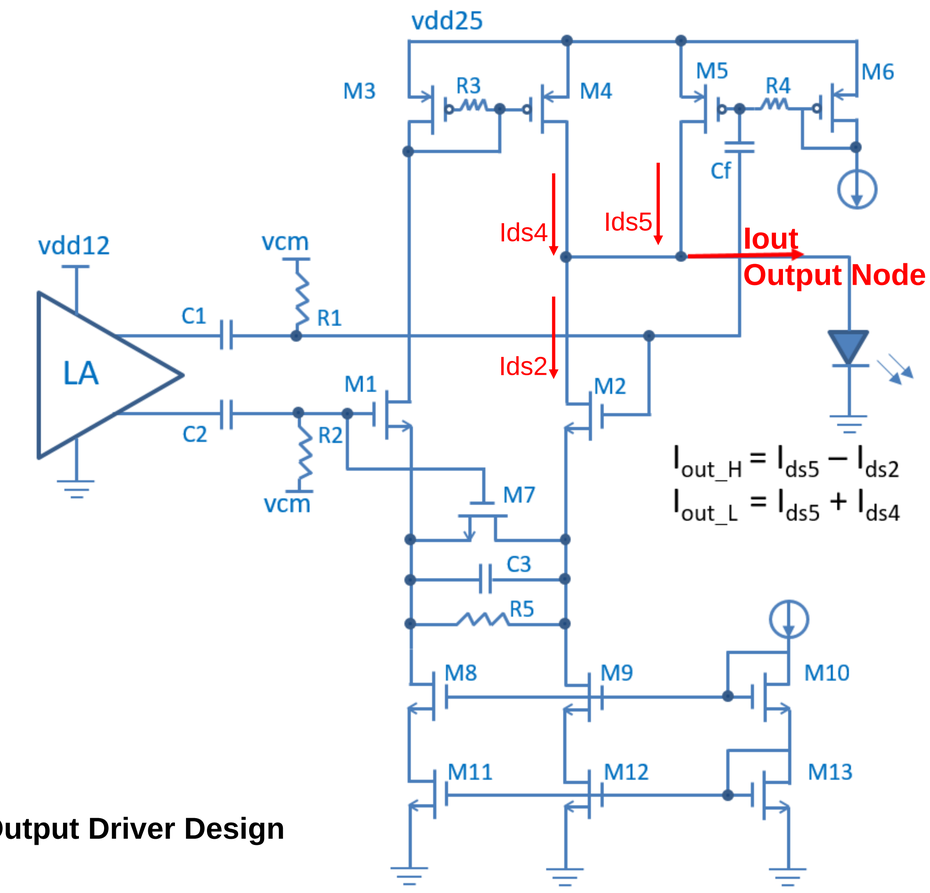


Overall Schematic Diagram



Limiting Amplifier (LA)

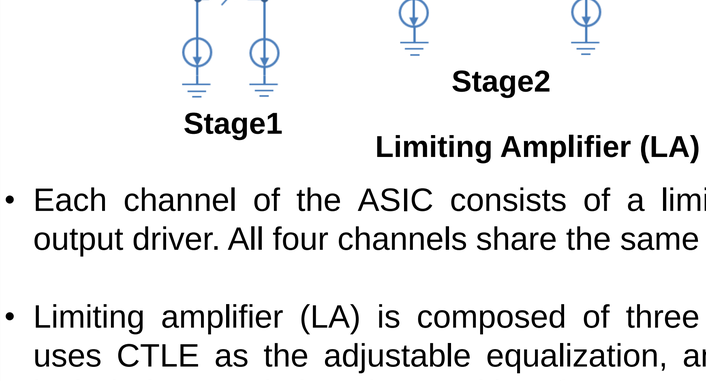
- Each channel of the ASIC consists of a limiting Amplifier (LA) and an output driver. All four channels share the same LA design as shown above.
- Limiting amplifier (LA) is composed of three differential stages. Stage1 uses CTLE as the adjustable equalization, and a passive inductance is included to optimize the peaking frequency. Stage2 and Stage3 both employ shared inductance structure.



Output Driver Design

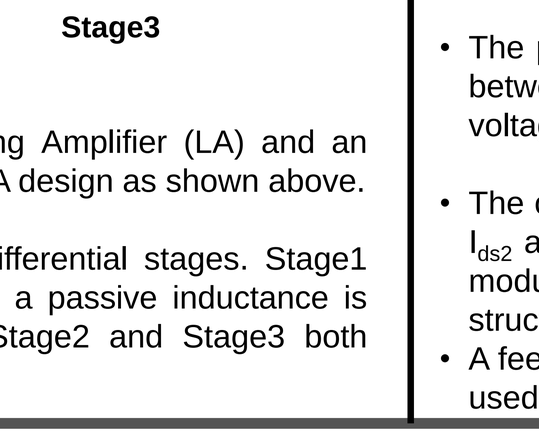
- The proposed output driver schematic is shown above. On-chip AC coupling is used between LA and output driver to lift the common voltage close to the VCSEL threshold voltage.
- The output current $\mathbf{I_{out} = I_{ds5} + I_{ds4} - I_{ds2}}$. Ids4 is mirrored from Ids1 by M3, so I_{ds4} and I_{ds2} are complementarily provided. Thus, the output amplitude consists both from the modulated right brunch(I_{ds2}) and the left brunch(I_{ds1}), making it a more efficient structure from the structure level compared to the conventional design.
- A feed-forward capacitor (Cf) together with R4, a CTLE(C3 and R5) structure are both used to improve the bandwidth.

Test results



Optical eye diagram testing set up

10Gbps optical eye



14Gbps optical eye

- The VCSEL driving ASIC is integrated in an array optical module and tested optically.
- VCSEL Array used in the test:
  II-VI 14G series
  APA4401040201 II-VI
- Wide-open 10-Gbps/ch and 14-Gbps/ch optical eye diagrams of the proposed VCSEL driver design were captured and shown in the left.
- The tested power consumption is 44mW/ch for the proposed driving structure at a data rate of 14 Gbps.

Conclusion

- A novel output stage structure of a VCSEL driver is proposed, designed and implemented in a 4 x 14Gbps/ch VCSEL array driver.
- The test results show wide-open 10Gbps and 14 Gbps optical eyes, and the design achieves a power consumption of 44 mW/ch at 14 Gbps data rate.

Acknowledgments

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