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Design of a configurable column-parallel ADC in the MAPS for real-time beam monitoring

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As the leading research platform of heavy-ion science in China, the Heavy Ion Research Facility in Lanzhou (HIRFL) provides heavy-ion beams for research on nuclear physics and related applications. The beam monitoring system in HIRFL ensures the beam can be delivered in an accurate manner. The full image of the beam energy deposition is needed for accurate beam calibration, thus a Monolithic Active Pixel Sensor (MAPS), which can provide the energy deposition in each pixel, is being designed in a 130nm CMOS process. The MAPS will be equipped in different terminals where the sampling frequencies and required resolution varies. As the key part in realizing this MAPS with full-image output, a novel column-parallel ADC with configurable resolution from 5bit to 9bit has been designed for the MAPS. To respond to the restrict constraints of power dissipation, size, working speed and accuracy for the MAPS, the column-parallel ADC combines the dedicated sample phase and the signal conversion phase into a single phase. Moreover, the ADC has a high tolerance to the offset of the comparators by generating 1.5-bit in every stage. Each column-parallel ADC covers a small area of 100um x 300um, consumes low power of 5.4mW at 3.3V supply and provides the sampling rate from 5MS/s to 10MS/s with the dynamic input range of 1000 mV. In 9-bit mode, it can achieve the ENOB of 8.07 bit with the SNDR of 50.34dB. This paper discusses the design and performance of the column-parallel ADC.

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