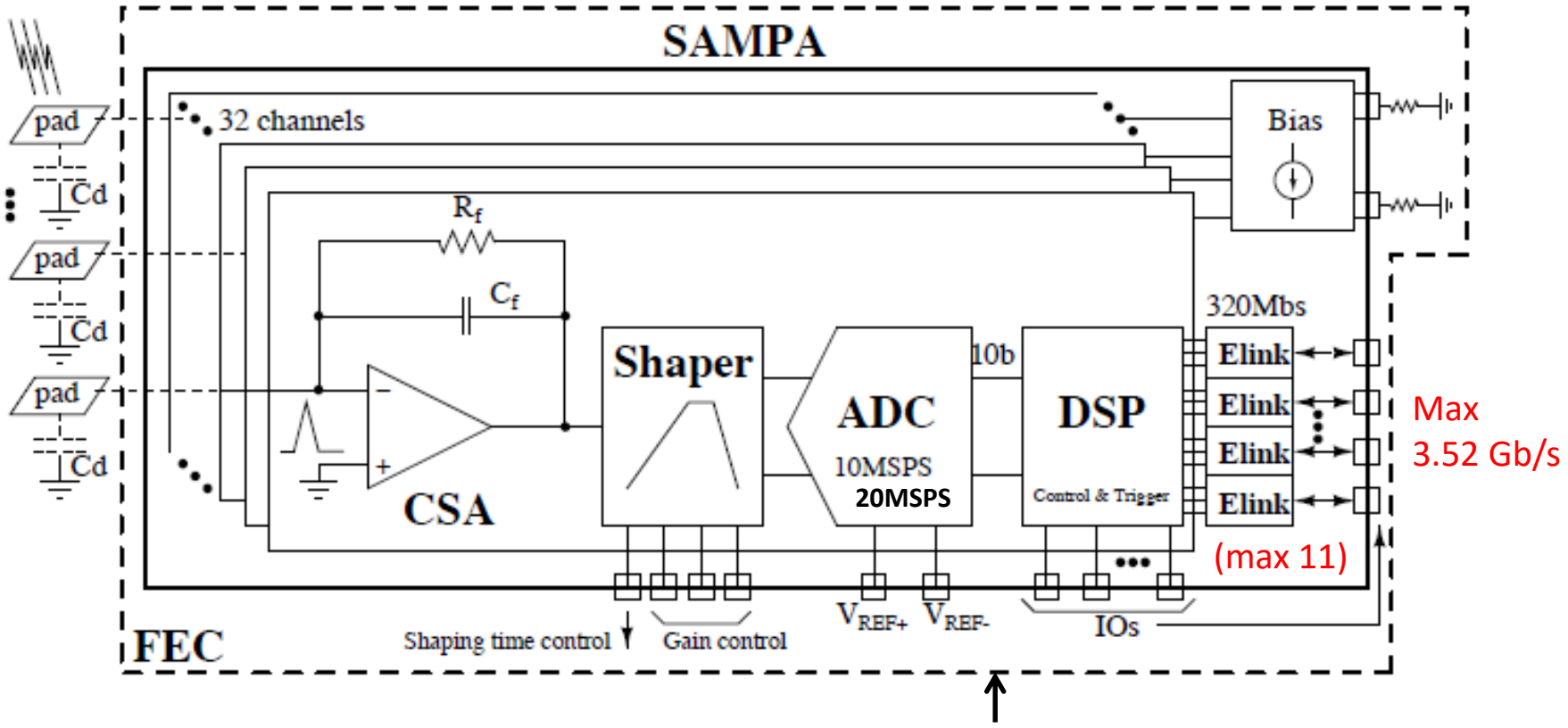
Project Motivation

- For CERN LHC Run 3 (2021) the ALICE collaboration is upgrading their TPC with a GEM based detection system that is read out continuously.
- A new front end ASIC (**SAMPA**) was developed for this purpose.
- We are interested in seeing how experiments at Jefferson Lab can take advantage of this technology and of the continuous readout concept.

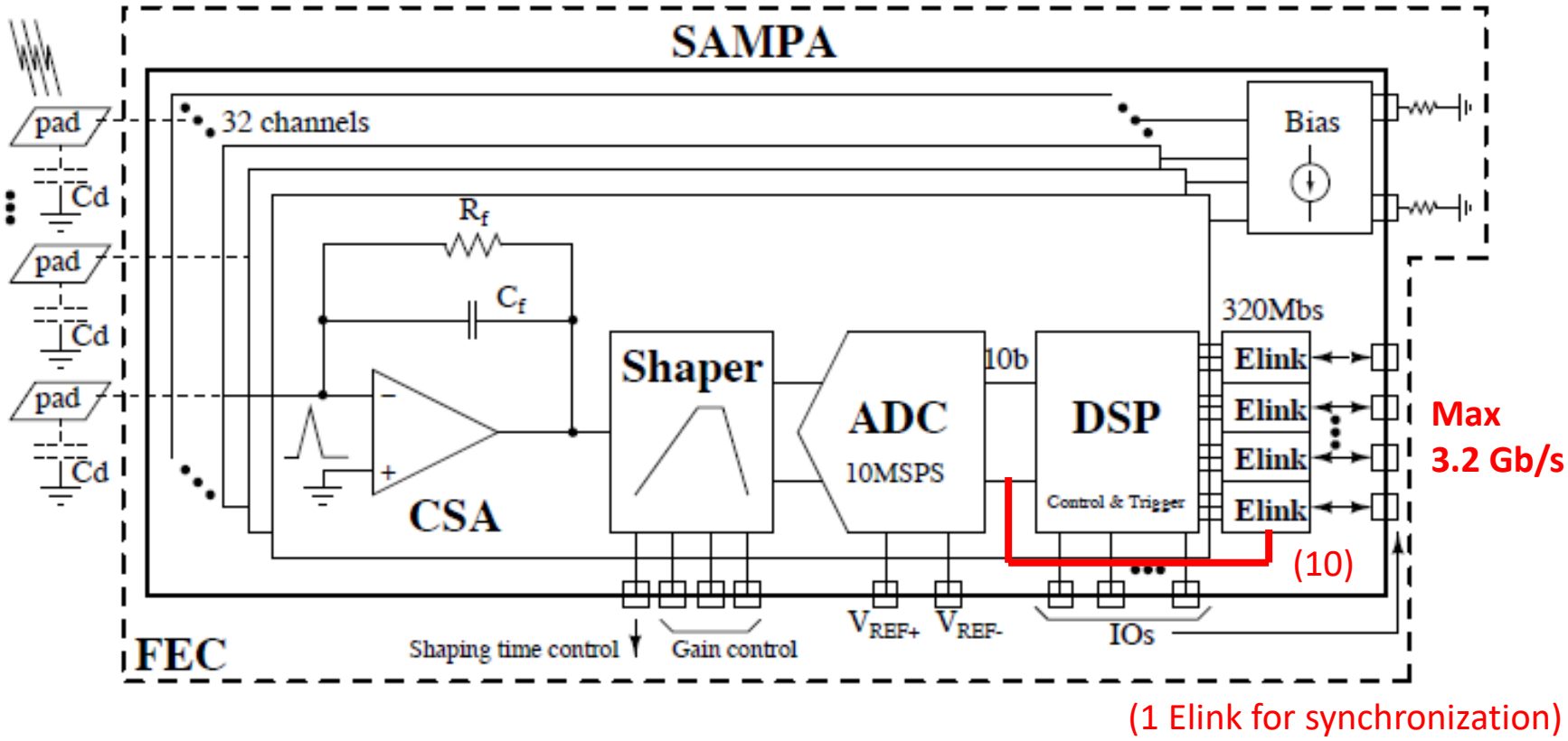
SAMPA Block Diagram



Raw data rate (10MHz) = 32ch x 10b x 10M/s = 3.2Gb/s

(20MHz) = 6.4Gb/s

SAMPA Block Diagram



Raw ADC Mode – bypass DSP

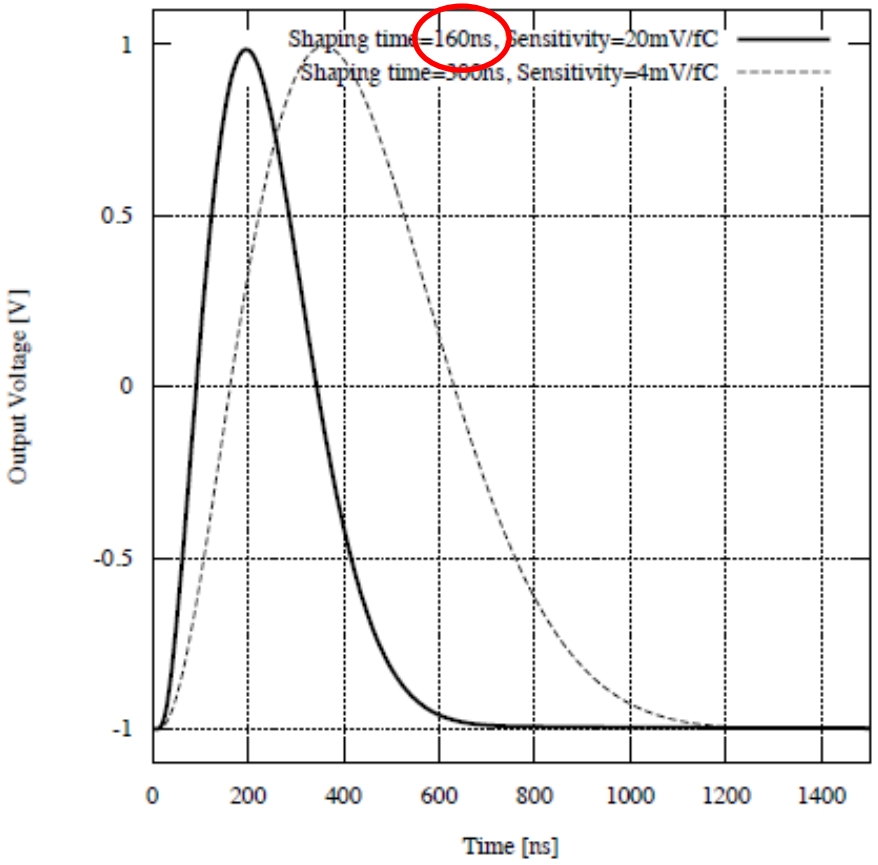
(Raw data rate (10MHz) = 3.2Gb/s = MAX output of chip)

Functional Blocks

- Charge Sensitive Amplifier (CSA)
  - Integrates and amplifies short current pulse
  - Output is a Voltage signal with amplitude proportional to the total charge Q
  - Tail of Voltage pulse is long (T = Rf*Cf)
  - Vulnerable to pile-up unless followed by a shaping filter

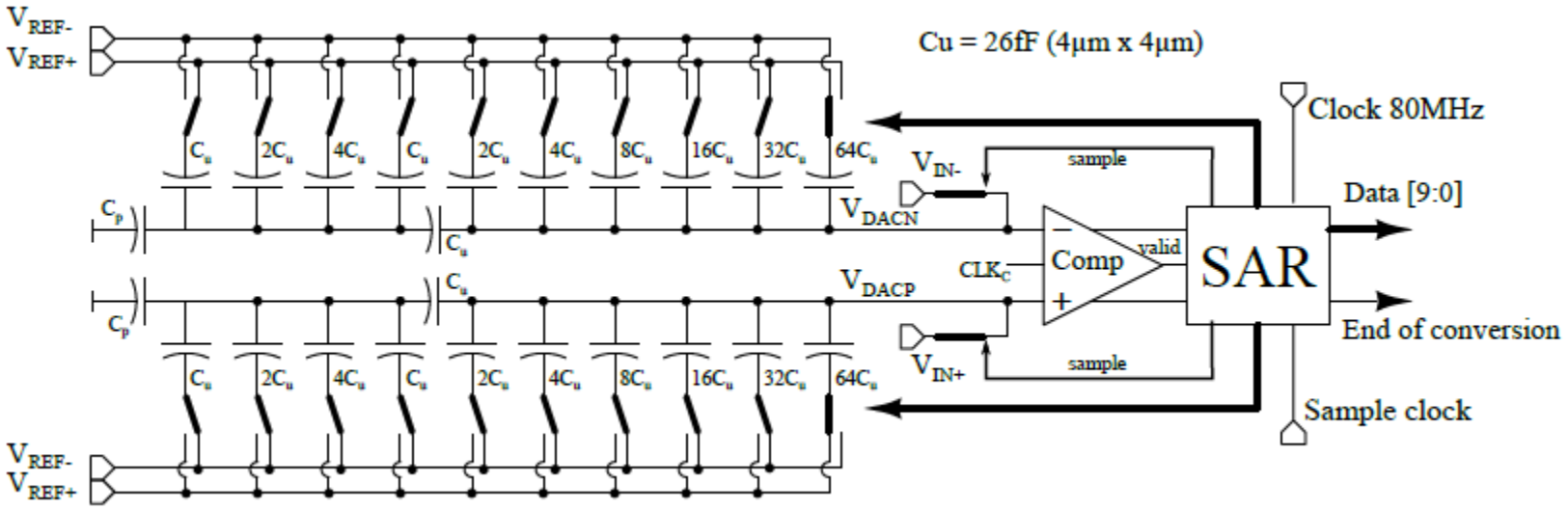
- Shaper
  - Creates a 4^{th} order semi-Gaussian pulse shape
  - Available shaping times (TS): ~~80~~, 160, 300 ns (SAMPA V3, V4)
  - Permits sampling by ADC at reasonable rates (10, 20 MHz)
  - 80 ns option eliminated in order to reduce noise in CSA
  - SAMPA V5 is now in production with 80, 160 ns shaping times (sPHENIX)

Pulse from Shaper



Functional Blocks

- ADC
  - 10 bit precision
  - 10 MSPS or 20 MSPS (5 MHz for ALICE TPC)
  - Split capacitor fully differential SAR architecture (low power)
  - ADC data rate = 10 MSPS * 10 bits * 32 channels = 3.2Gb/s (6.4 Gb/s)



Successive Approximation Register

Functional Blocks

- DSP
  - Baseline Correction 1 (BC1) – removes low frequency perturbations and systematic effects
  - Digital Shaper (DS) – tail cancellation or peaking time correction (IIR filter)
  - Baseline Correction 2 (BC2) – moving average filter
  - Baseline Correction 3 (BC3) – slope based filter (alternative to BC2)

  - **Zero suppression – fixed threshold**
  - Formatting; encoding for compression – Huffman
  - Buffering (16K x 10 bit)

Functional Blocks

- e-link
  - Electrical interface for transmission of serial data over PCB traces or electrical cables, for distances of several meters
  - Up to 320 Mb/s
  - Developed by CERN for the connection between Front-end ASICs and their GigaBit Transceiver (**GBTx**) chip

  - SAMPA: 11 e-links → 3.52 Gb/s max data output
  - Number and speed of SAMPA e-links used is programmable

SAMPA Specifications (ALICE)

Specification	TPC	MCH
Voltage supply	1.25 V	1.25 V
Polarity	Negative	Positive
Detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
Peaking time (ts)	160 ns	300 ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 600e@ts=160 ns*	< 950e @ Cd=40 pF* < 1600e @ Cd=80 pF*
Linear Range	100 fC or 67 fC	500 fC
Sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=160 ns	< 0.2%@ts=300 ns
ADC effective input range	2 Vpp	2 Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10 (20) Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
ENOB (ADC)**	> 9.2-bit	> 9.2-bit
Power consumption (per channel) CSA + Shaper + ADC	< 15 mW	< 15 mW
Channels per chip	32	32

*R_{esd} = 70Ω

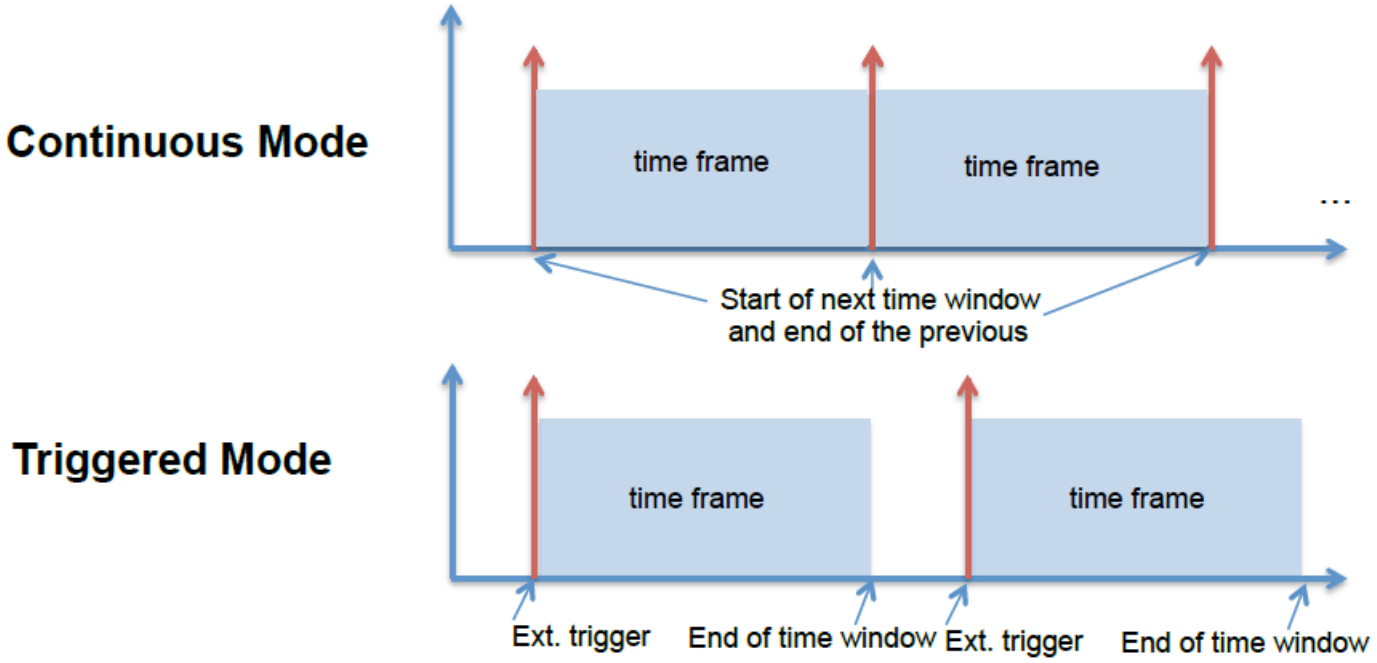
** @ 0.5MHz, 10Msamples/s

SAMPA Readout - Zero Suppression

- Cluster – consecutive ADC samples above threshold (**> 1**)
- pre/post samples can be included in the cluster (program up to 3 pre, 7 post)
- Clusters are merged if there are up to 2 samples below threshold separating them

- For each time frame all channels produce their own data packet from the cluster data
- Header for data packet has time stamp (bunch crossing counter)
- Cluster data has time offset (sample number) appended

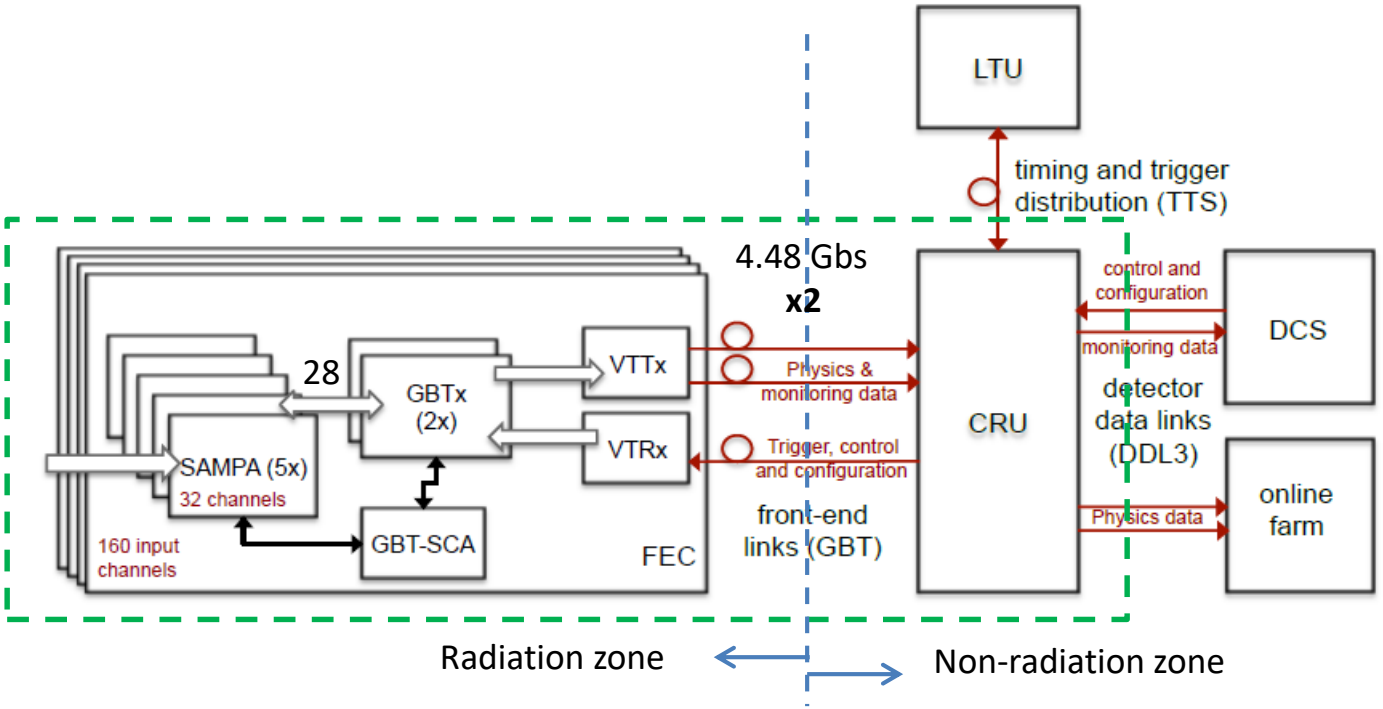
SAMPA Readout



Data from ADC can be delayed by up to 192 samples to account for trigger latency

Time frame is programmable (max = 1024 ADC samples)
102.4 us @ 10 MSPS
(51.2 us @ 20 MSPS)

ALICE SYSTEM



FEC – Front End Card (160 ch / FEC)

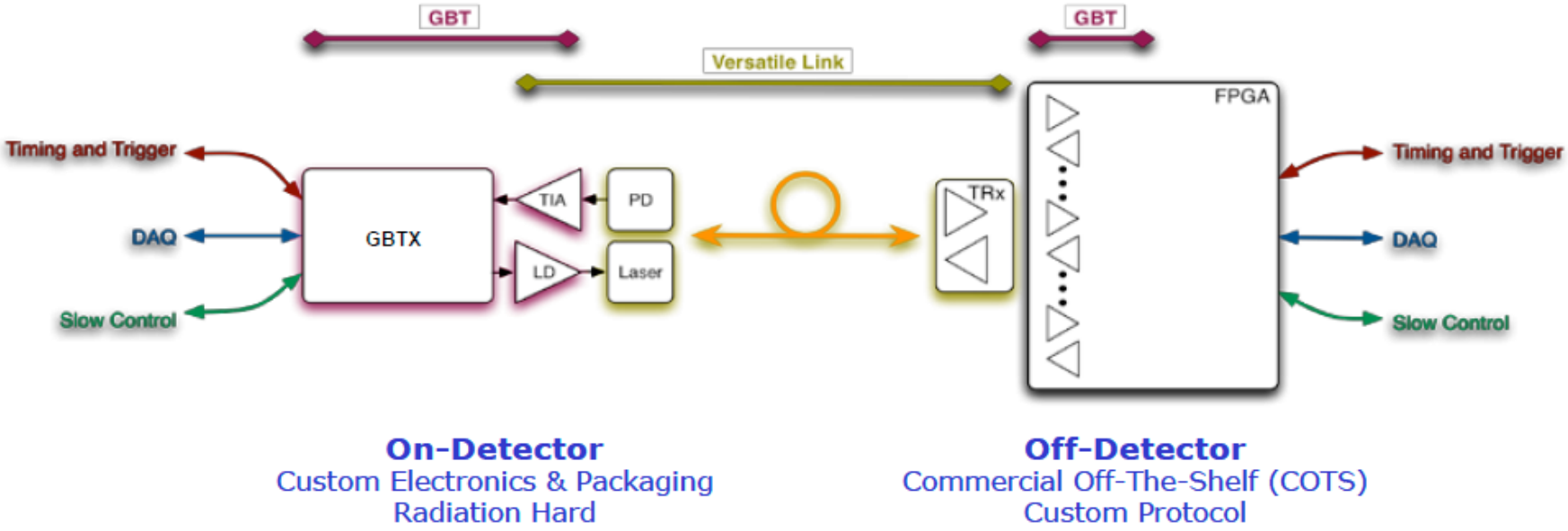
CRU – Common Readout Unit (~12 FECs / CRU = ~1920 ch / CRU)

GBTx – Giga Bit Transceivers

GBT-SCA – GBT Slow Controls Adapter

VTTX, VTRx – Fiber optic tranceivers

GBT link



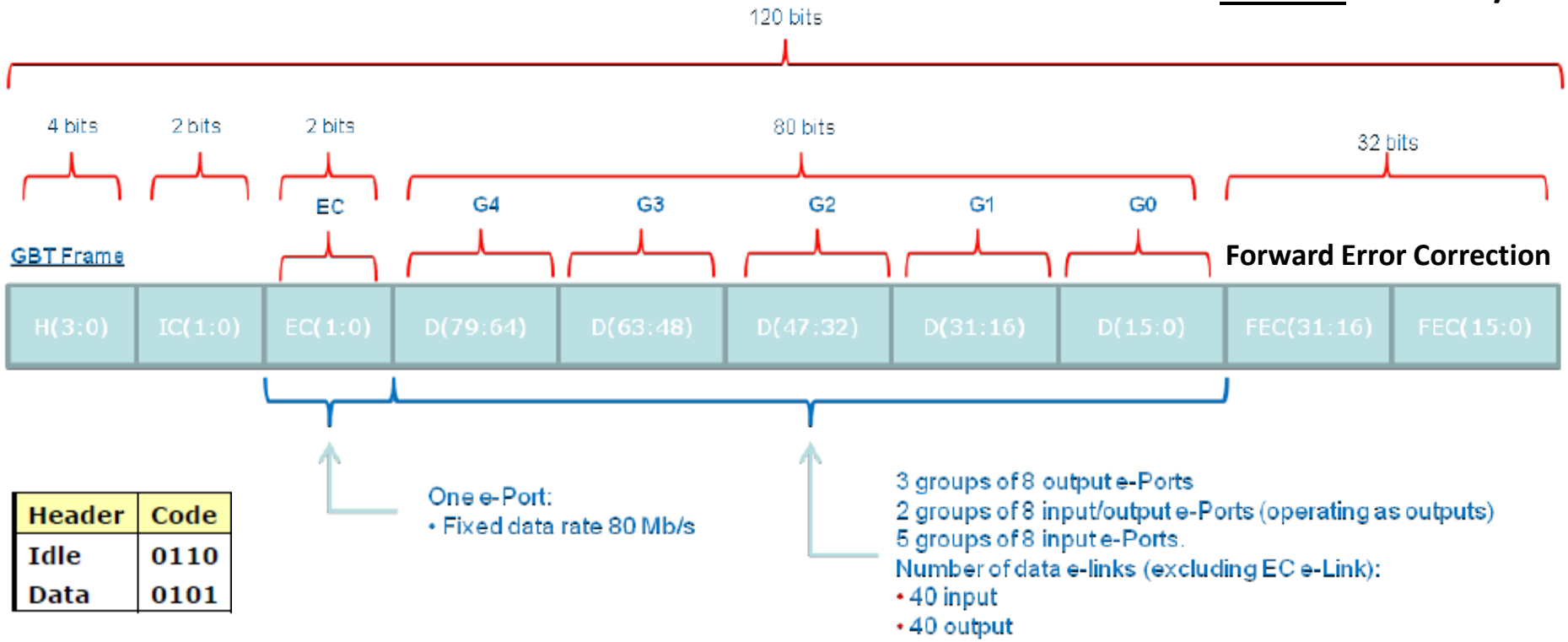
Single bidirectional optical link simultaneously provides data paths for:

- Timing and Trigger Control (TTC)
- Data Acquisition (DAQ)
- Slow Controls (SC) – configuration and monitoring

<u>Fixed Latency</u>

GBT frame format

80 bit payload
80 bits x 40 MHz = **3.2 Gb/s**



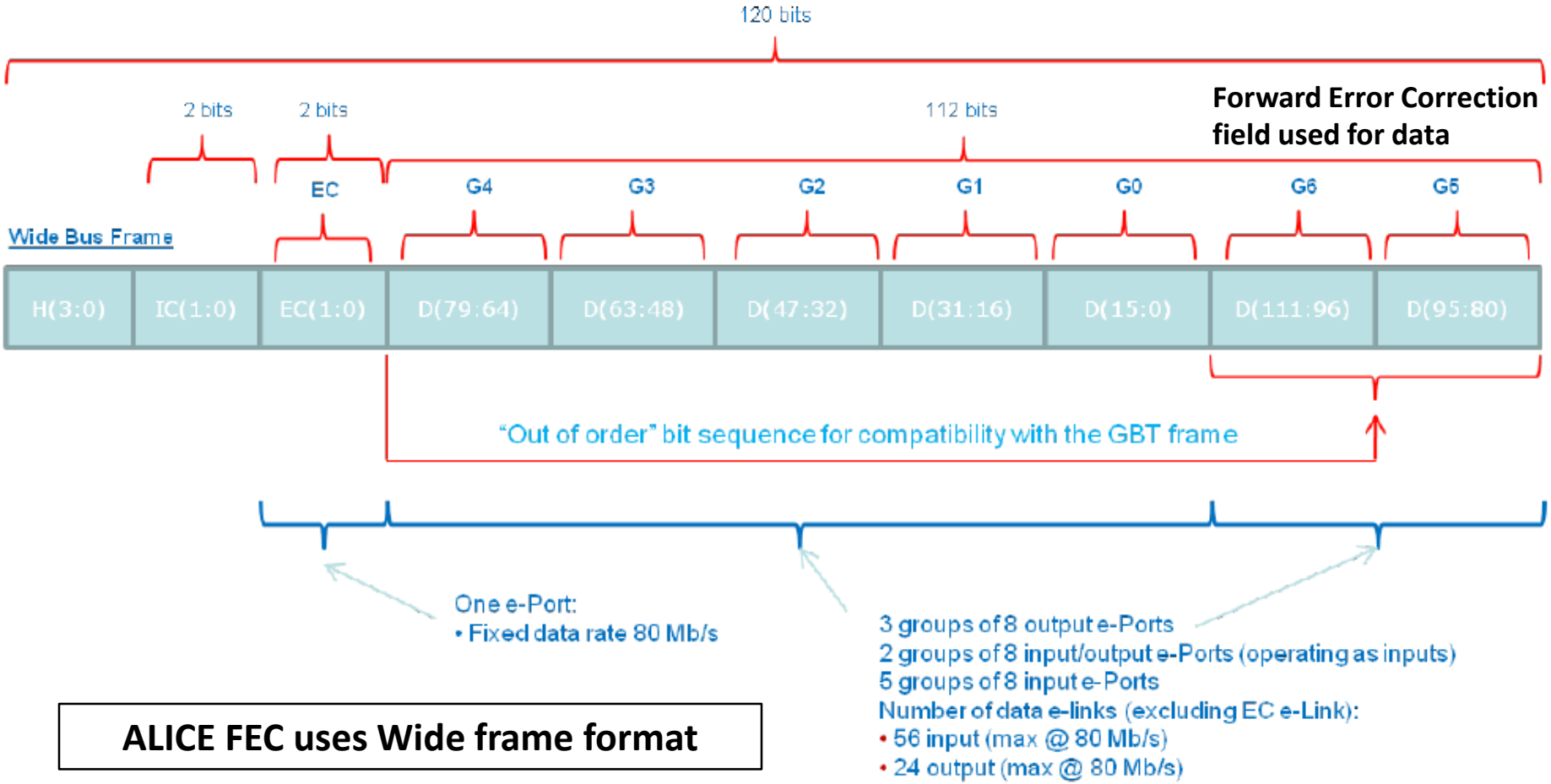
Header	Code
Idle	0110
Data	0101

32-bit Forward Error Correction field
Corrects up to 16 bit burst error

GBT Wide frame format

112 bit payload

112 bits x 40 MHz = **4.48 Gb/s**

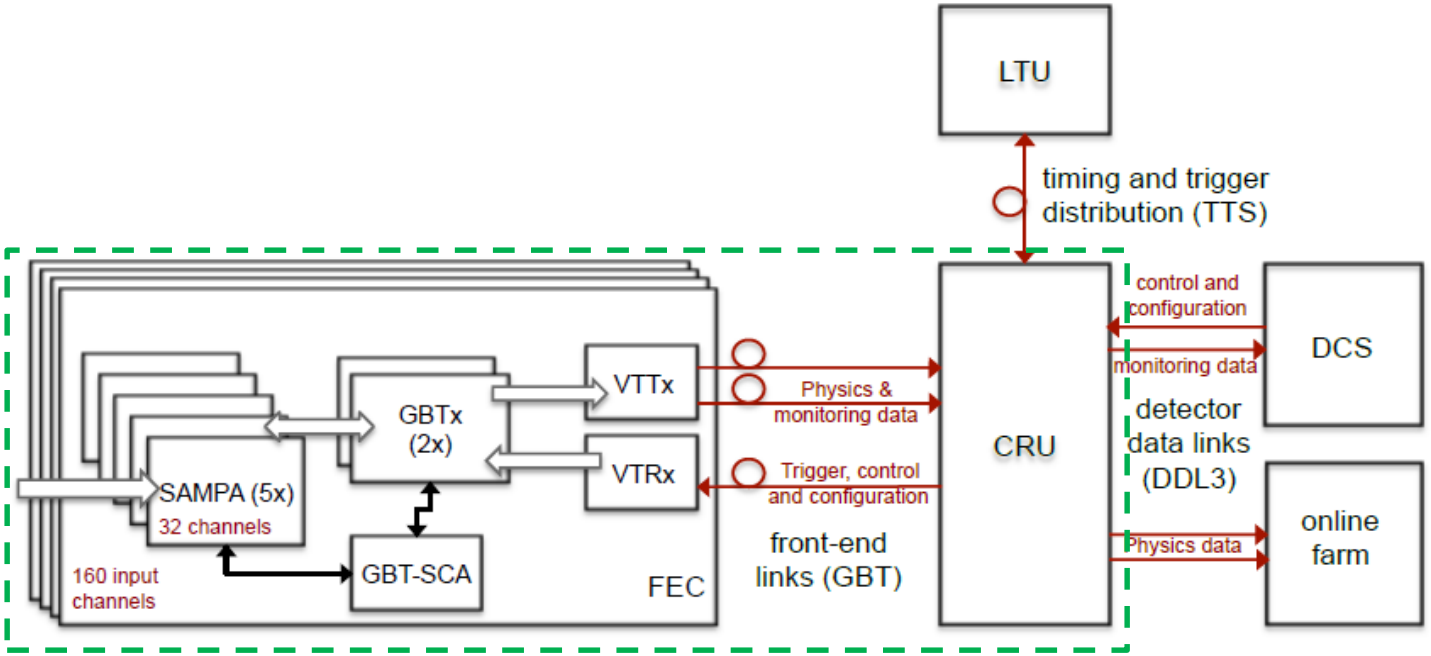


ALICE FEC uses Wide frame format

Common Readout Unit (CRU)

- Interface between the on-detector systems, the online computing system, and the Central Trigger Processor
- Multiplexes data from several front-end links into higher speed data links
- Can do processing on data (big FPGA)
- Sends trigger, control, and configuration data to front-ends
- Based on commercial high-performance FPGA
- Located outside of radiation area, so no worry of SEUs
- **PCIe** platform

- **Chosen Path** – use as many components of the ALICE TPC readout/control chain as possible



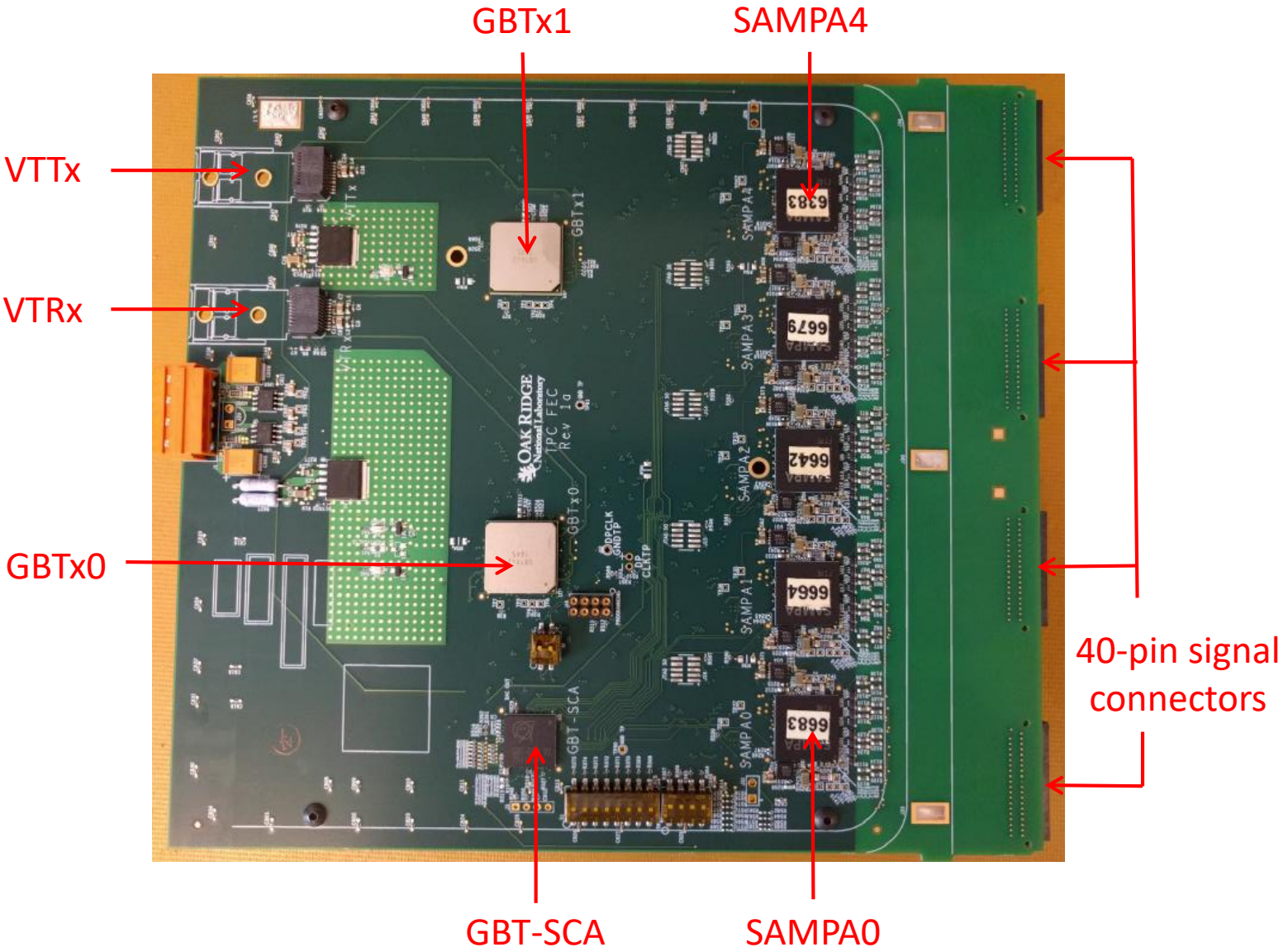
FEC – Front End Card (160 ch / FEC)
CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU)

System Components

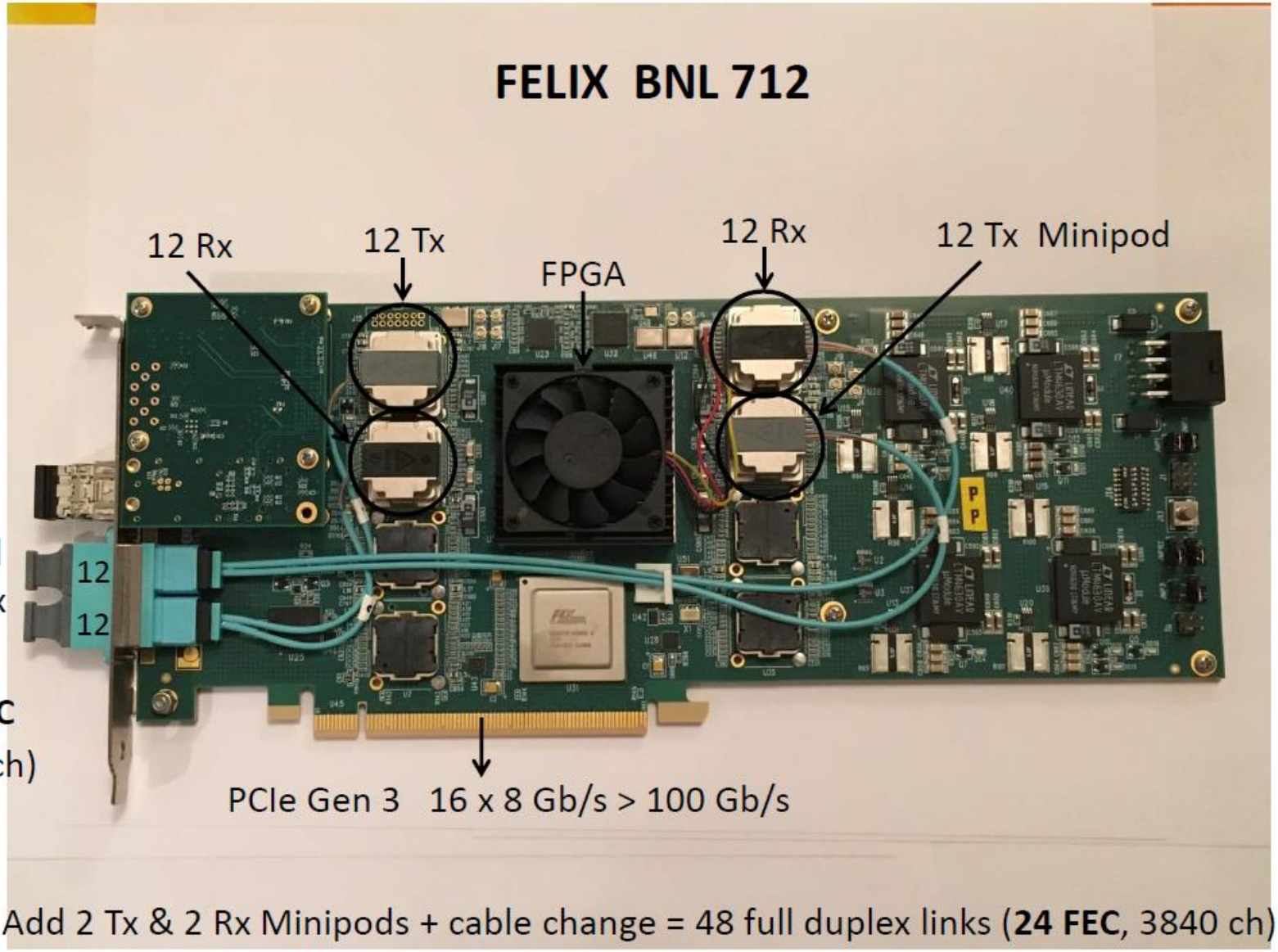
- Built 5 ALICE TPC FECs from manufacturing files (Oak Ridge)
- Purchased FELIX CRU (ATLAS BNL-712) from BNL (ALICE CRU not available)

- Course change:
  - ALICE FECs use GBTx Wide frame format
  - FELIX CRU firmware did not support it (have to get and modify their firmware)
  - Obtain C-RORC readout card (ALICE/ATLAS). For their tests of SAMPA FECs they modified firmware to support GBTx Wide frame format
  - Start with their existing test software for C-RORC

FEC – JLab version



FELIX BNL 712



Add 2 Tx & 2 Rx Minipods + cable change = 48 full duplex links (**24 FEC**, 3840 ch)

C-RORC/T-RORC

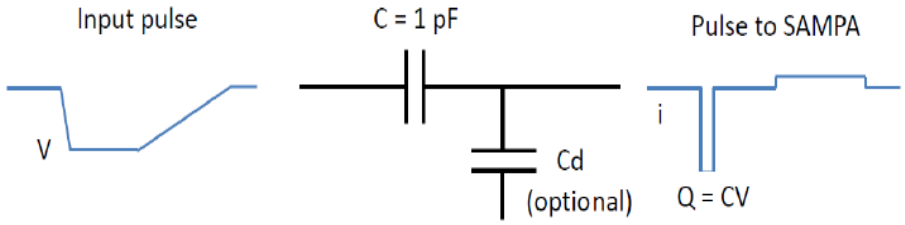
(~ 30 Gb/s)

SAMPA Studies

- Linearity - 10 MHz sampling, 20 MHz sampling, 20 mV/fC gain, 30 mV/fC
- Effect of input capacitance on noise
- Effect of charge deposition time on SAMPA pulse shape
- Time resolution – 20 MHz sampling
- Cross-talk
- Effect of pulse time shift relative to sampling clock on extracted pulse parameters – 10 MHz sampling, 20 MHz sampling

Injecting Charge in the SAMPA Inputs

A voltage step is applied to a 1 pF capacitor (2% tolerance) that is connected to the SAMPA input. The leading edge is fast (3 ns) so that we can observe the system's response to an impulse stimulus. The trailing edge is very slow (25 μs) so that the reverse current pulse is virtually undetectable. The charge injected is Q = CV.



20 MHz sampling: pulse period = **50.004 us** (SAMPA time frame = 50.000 us)
10 MHz sampling: pulse period = **100.008 us** (SAMPA time frame = 100.000 us)

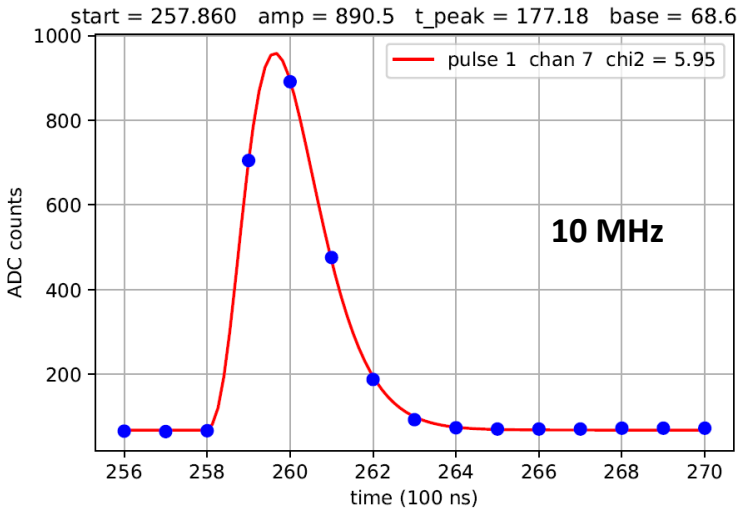
(Can adjust leading edge of input pulse to inject same charge over longer time period.)

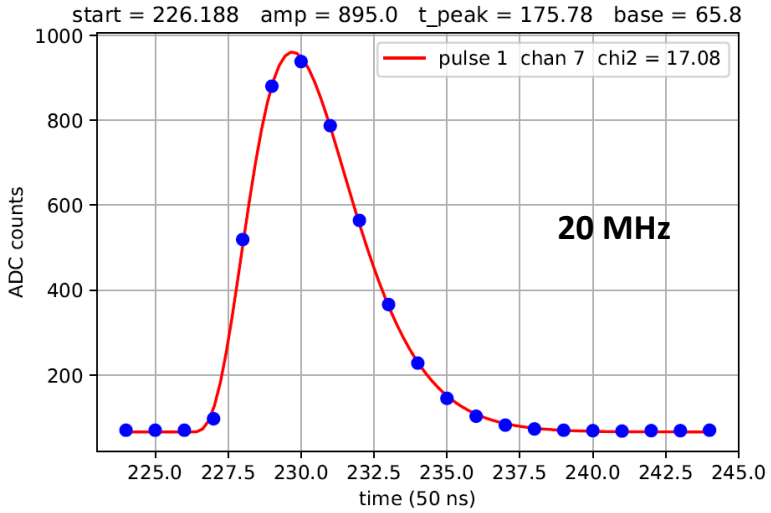
SAMPA Pulse Shape

$$f(x) = A\left(\frac{x-t}{\tau}\right)^{N} e^{-N\left(\frac{x-t}{\tau}\right)} + Bl.$$

A is the peak, ***N=4*** is the shaping order of the amplifier, τ is the peaking or decay time, *Bl* is the baseline, and *t* is the start time of the pulse. The waveform *amplitude* is Ae^{-4}. The maximum value of *f* = *amplitude* + *Bl*, and occurs at time $t + \tau$. We refer to this equation as the SAMPA impulse shape.

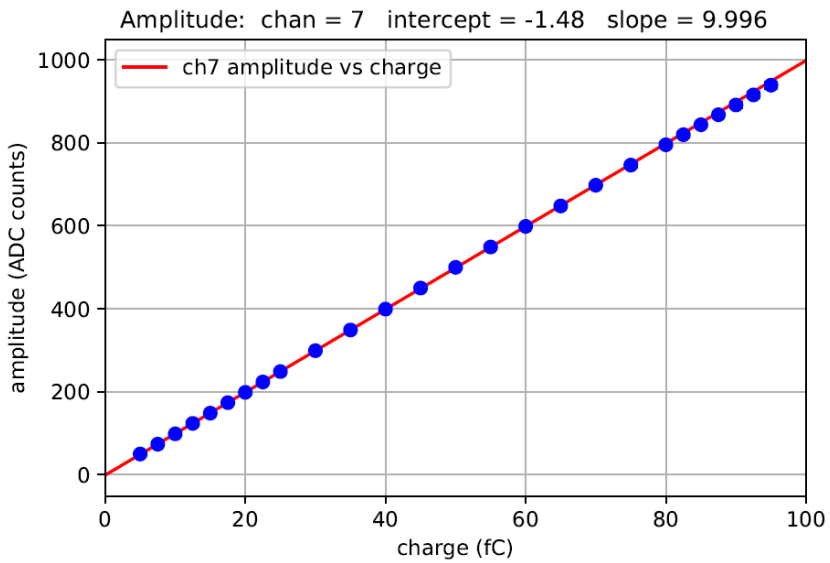
Pulse Fit (input = 90 mV)



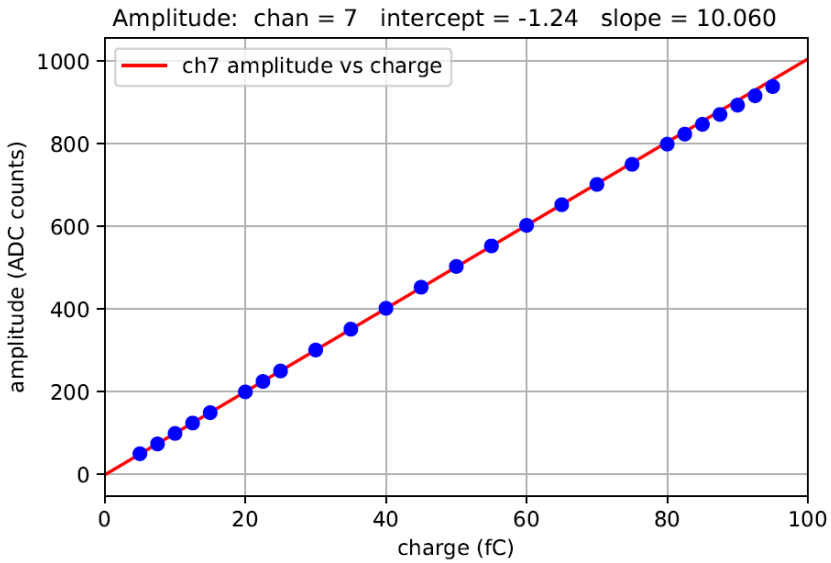


Pulse Fit Amplitude vs Input Charge

10 MHz

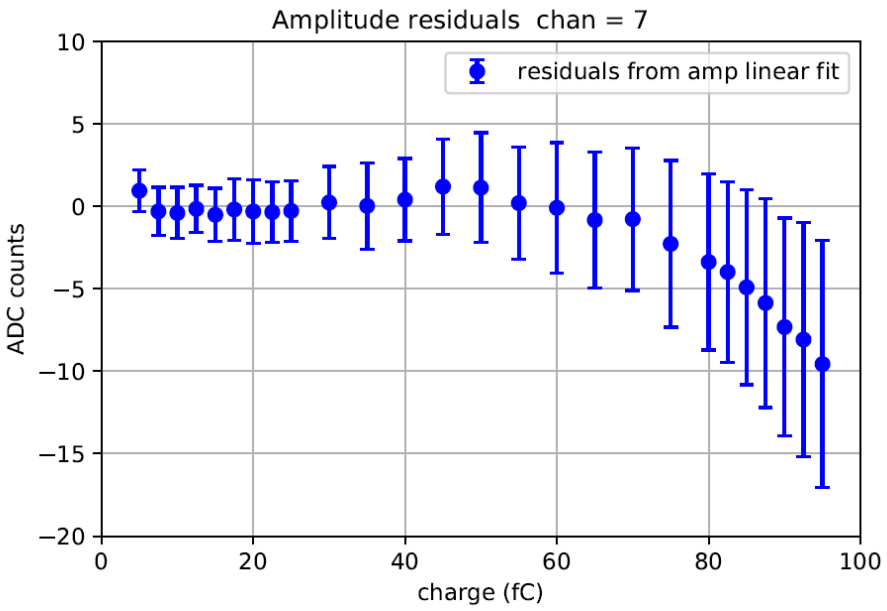


20 MHz

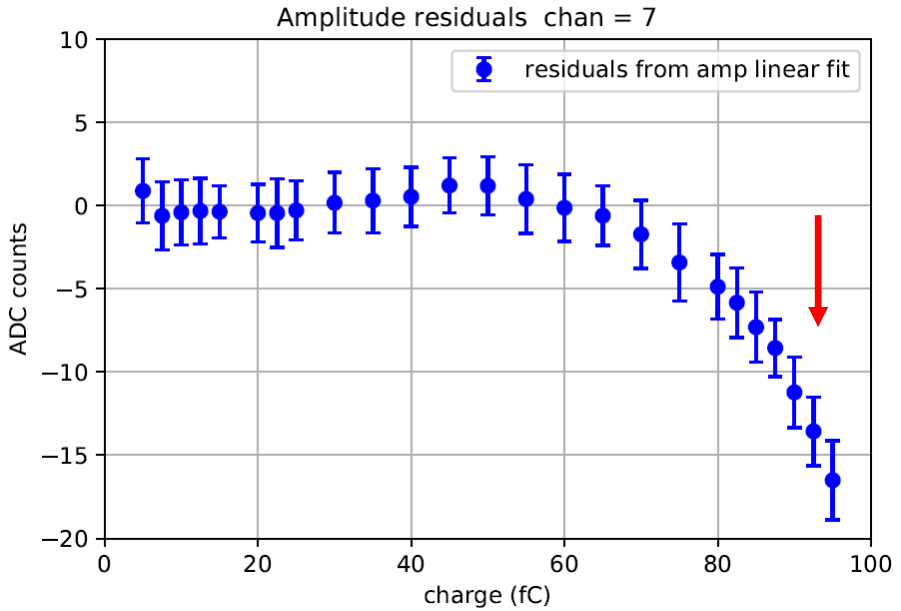


Amplitude Residuals from Linear Fit

10 MHz



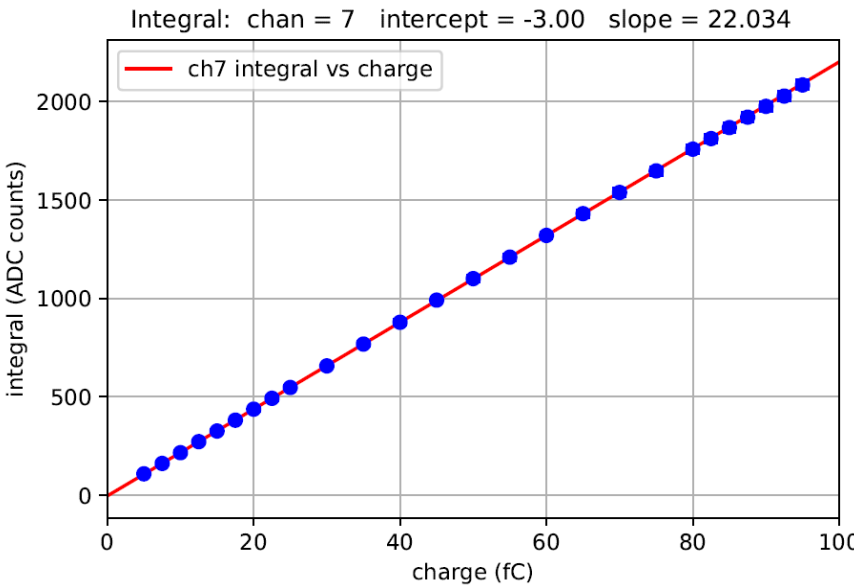
20 MHz



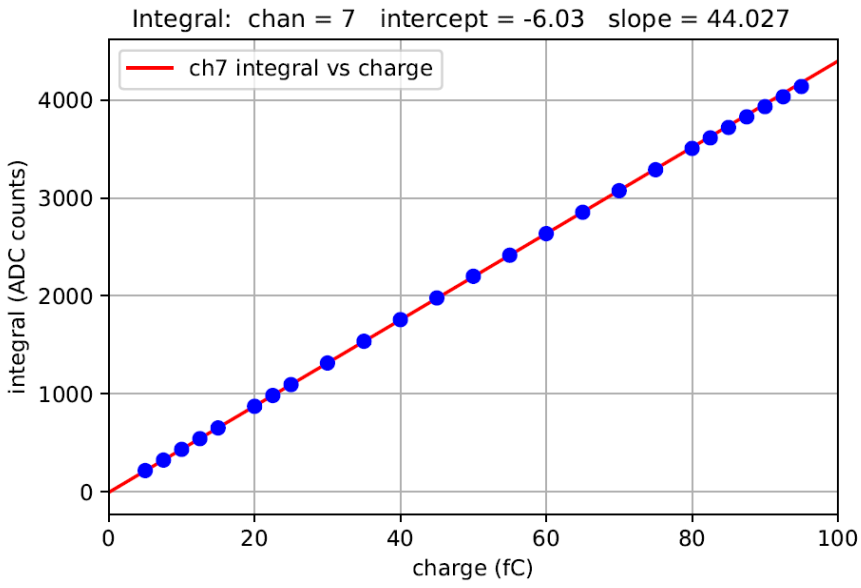
Do Linear fit up to 70 fC

Pulse Integral vs Input Charge

10 MHz

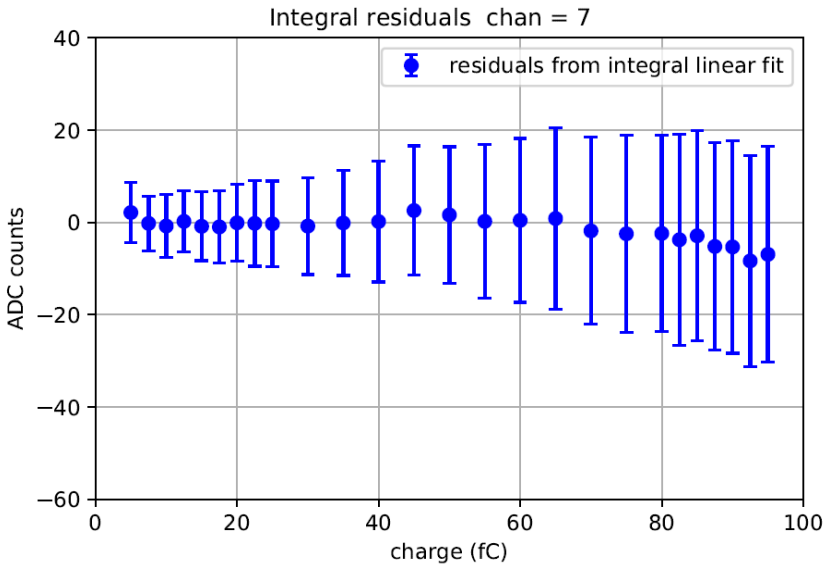


20 MHz

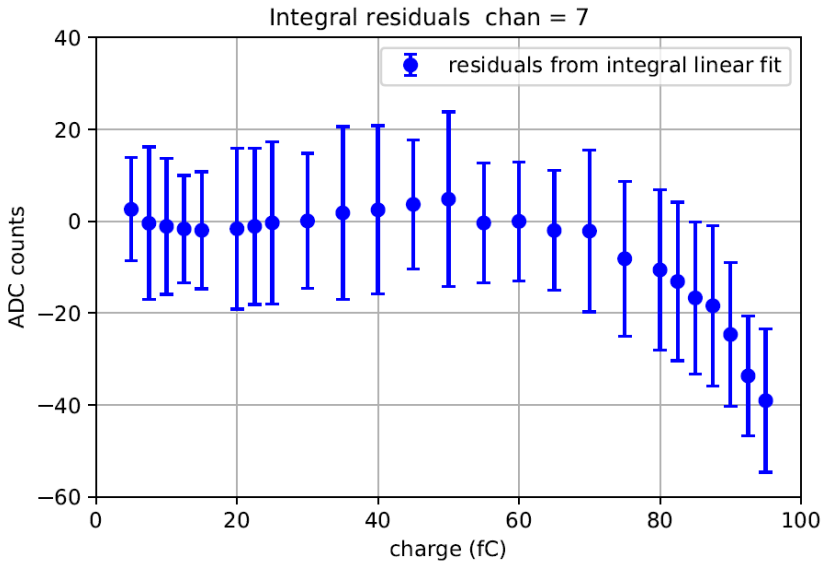


Integral Residuals from Linear Fit

10 MHz

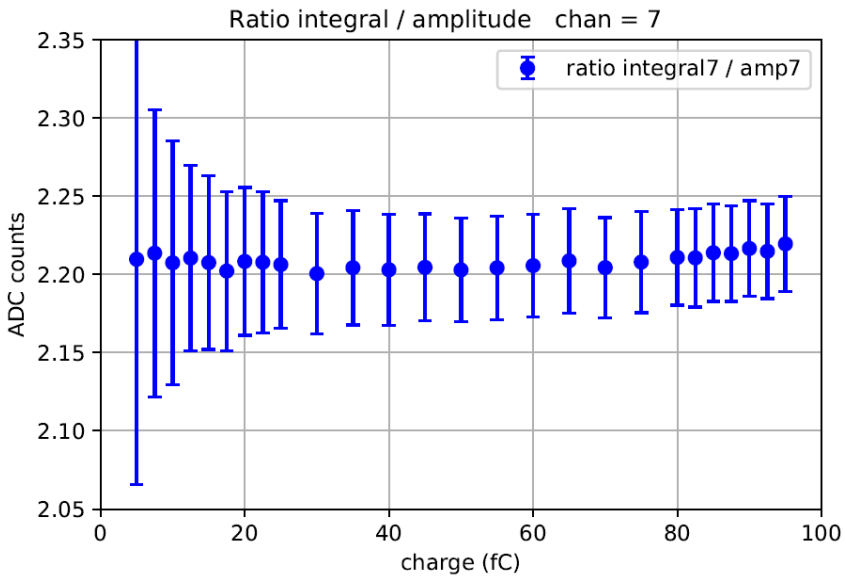


20 MHz

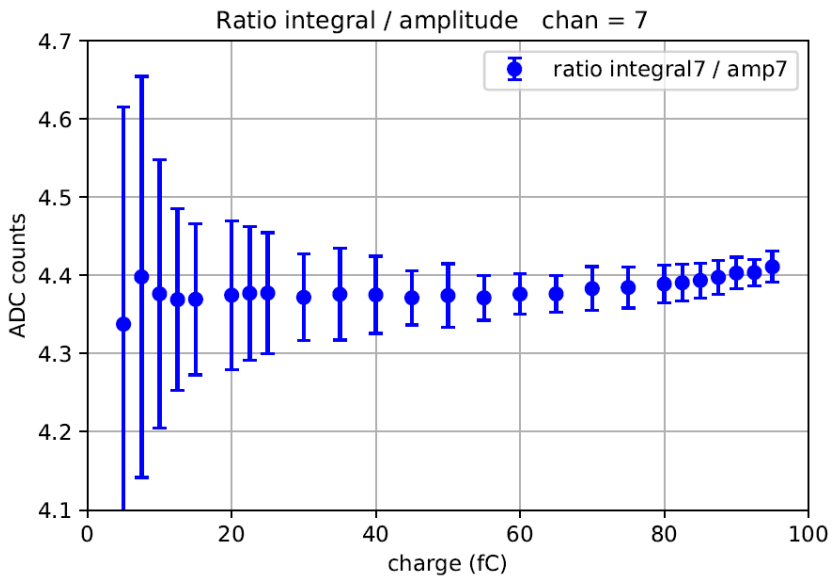


Ratio Integral/Amplitude

10 MHz



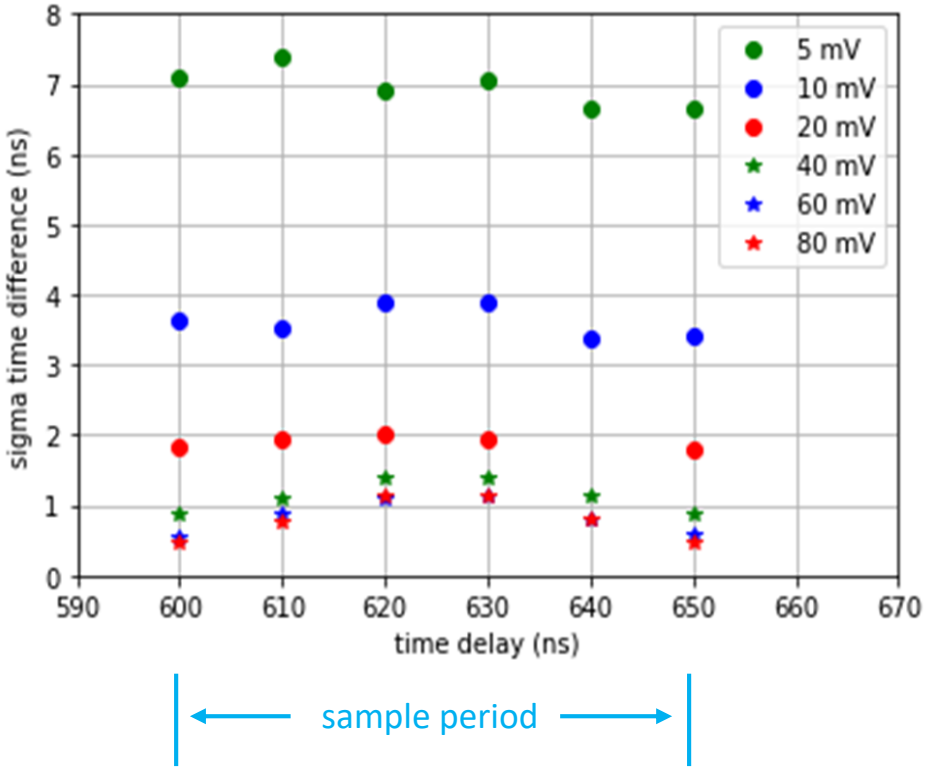
20 MHz



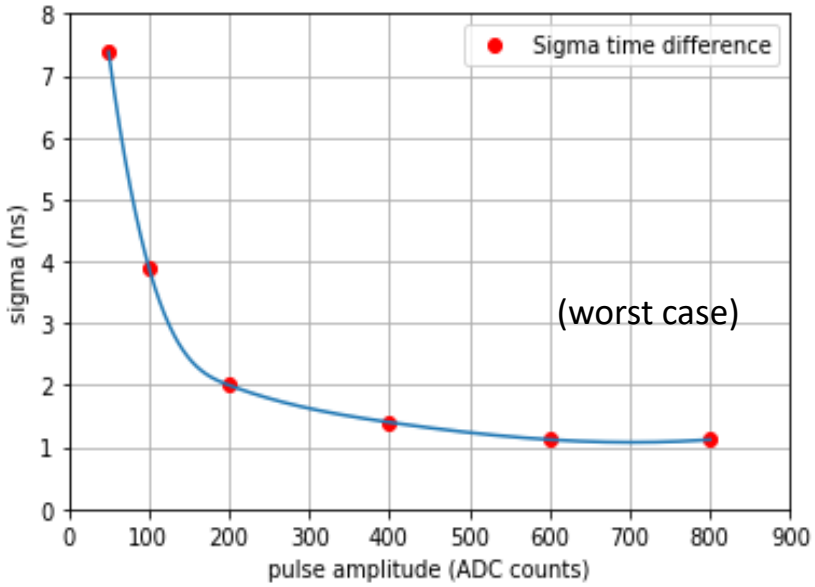
SAMPA Time Resolution Study 1

- Inject charges into 2 separate channels
- time difference between charge pulses is stable and adjustable
- Use ***Start Time*** parameter from the pulse fit to define time of pulse
- 20 MHz sampling results

σ(Δt) vs. Δt

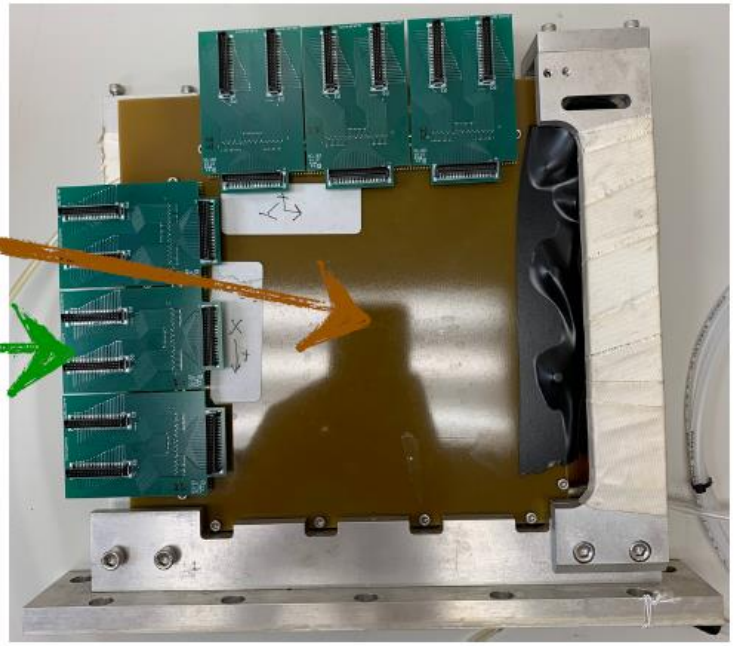


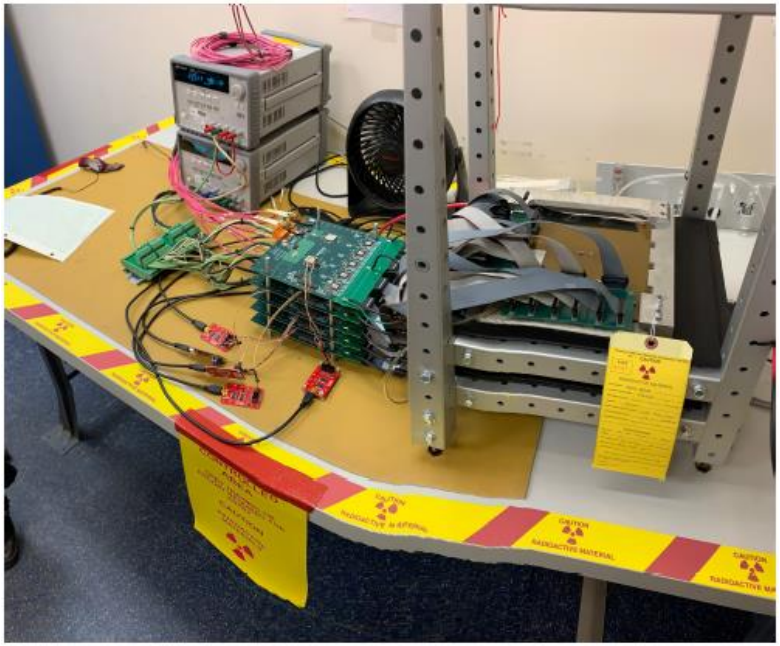
σ(Δt) vs. Pulse Amplitude



Hall C Prototype GEM Detector (Mississippi State)

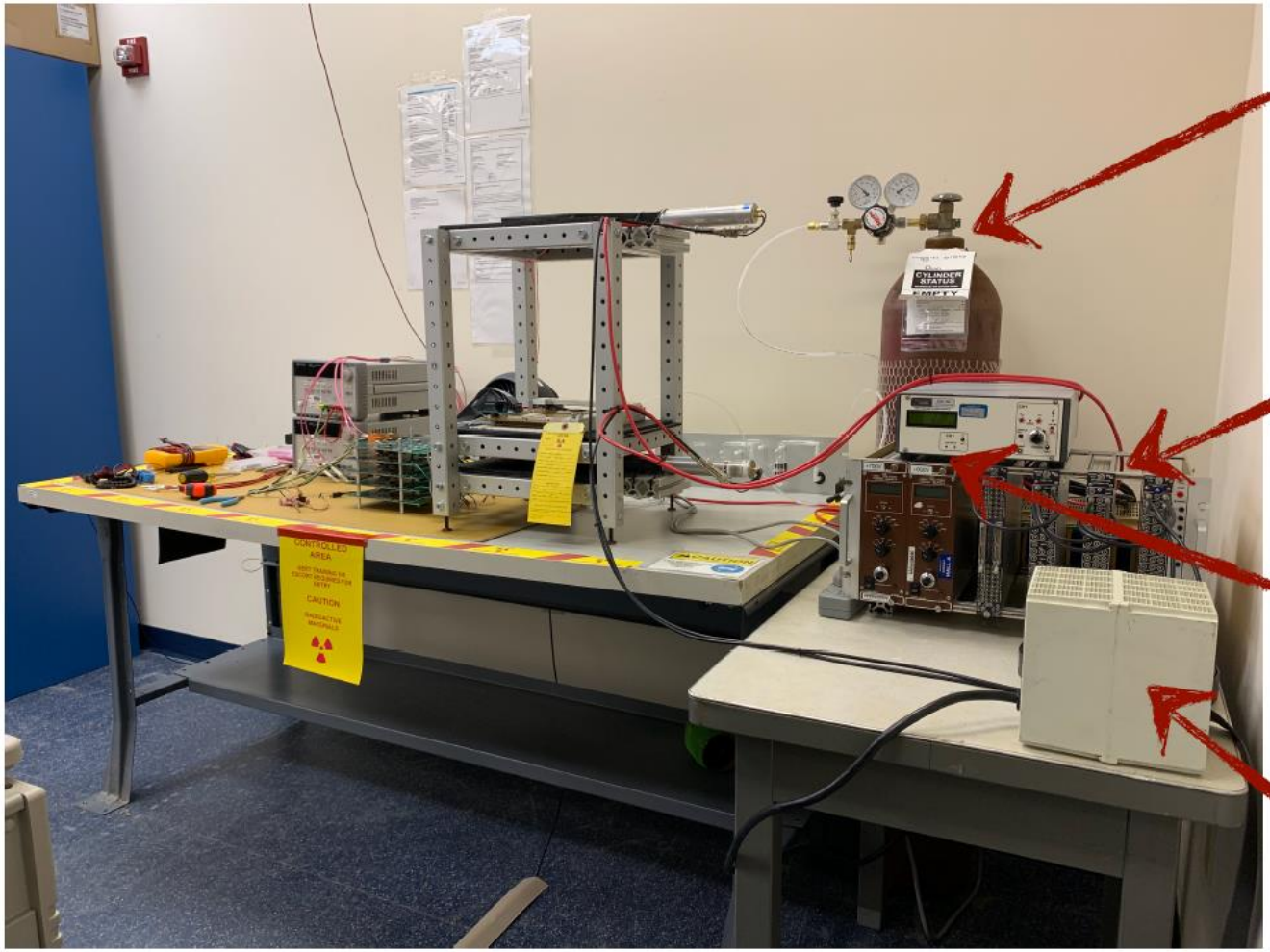
- Triple GEM (153.6mm x 153.6mm active area)
- X and Y readout 400µm pitch (X strips 80µm, Y strips 340 µm)
- 768 channels match well with our 800 channel SAMPA readout system





(I guess spacetime is curved after all)

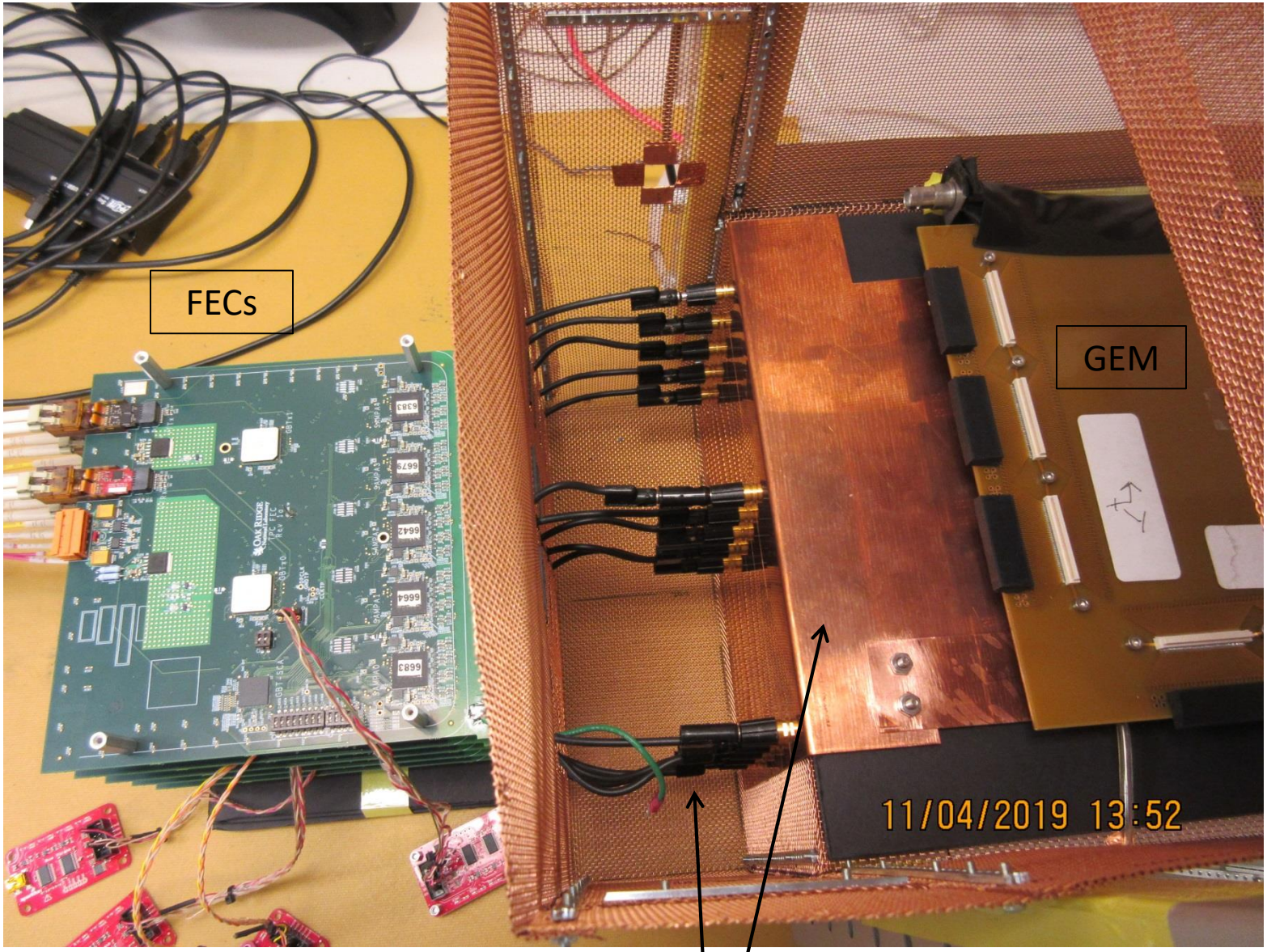
Prototype GEM Detector System

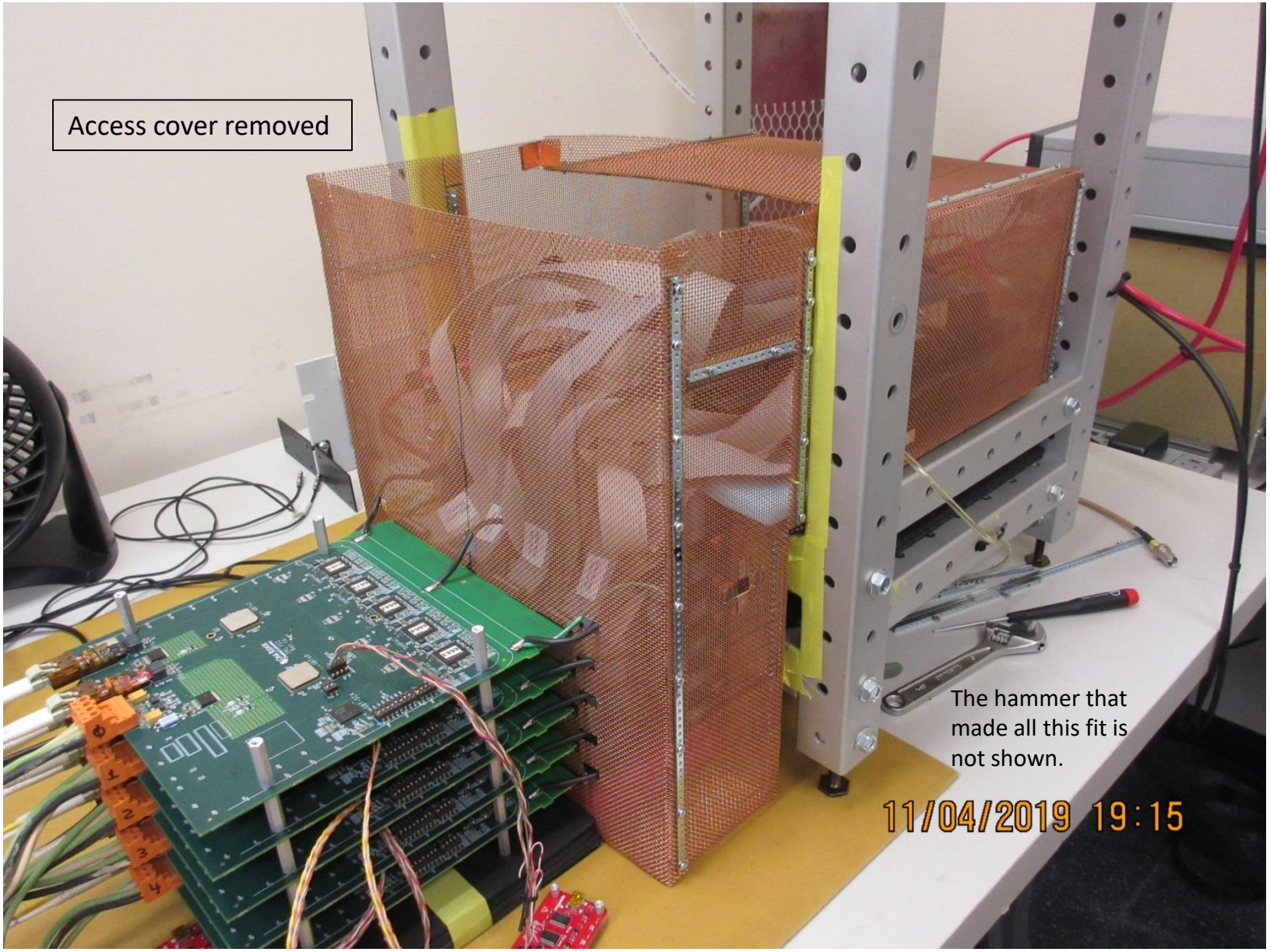


Thanks to Eric Pooser and Abigail Hellman for assembling this last summer.

Initial Readout of GEM with SAMPA

- Raw ADC mode (5 MHz)
- **NOISE!**
- Noise reduced significantly by improving GROUND connections between FECs and GEM
- Use **FFT** on raw ADC samples to investigate noise sources (e.g. switching power supply, lights, powered chassis,…). Eliminate what we can control.
- Evidence suggests that EMI is picked up by the cables from GEM to SAMPA front end cards or by the GEM itself. (Noise with test pulse card ~1 ADC count)
- Decide to shield only passive components (cables, GEM) in a Faraday cage
- Including FECs, cables, and GEM inside a single Faraday cage risks that EMI radiated from the FECs (multi GHz frequencies) is trapped within the cage, possible making the noise situation worse.

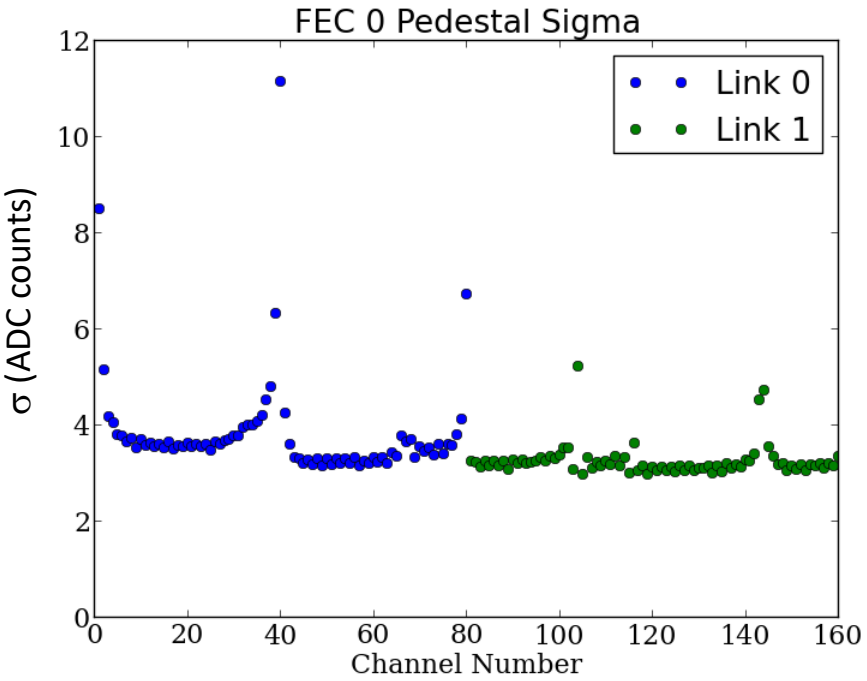

FECs
GEM
11/04/2019 13:52
FEC – GEM ground connections



Cables installed

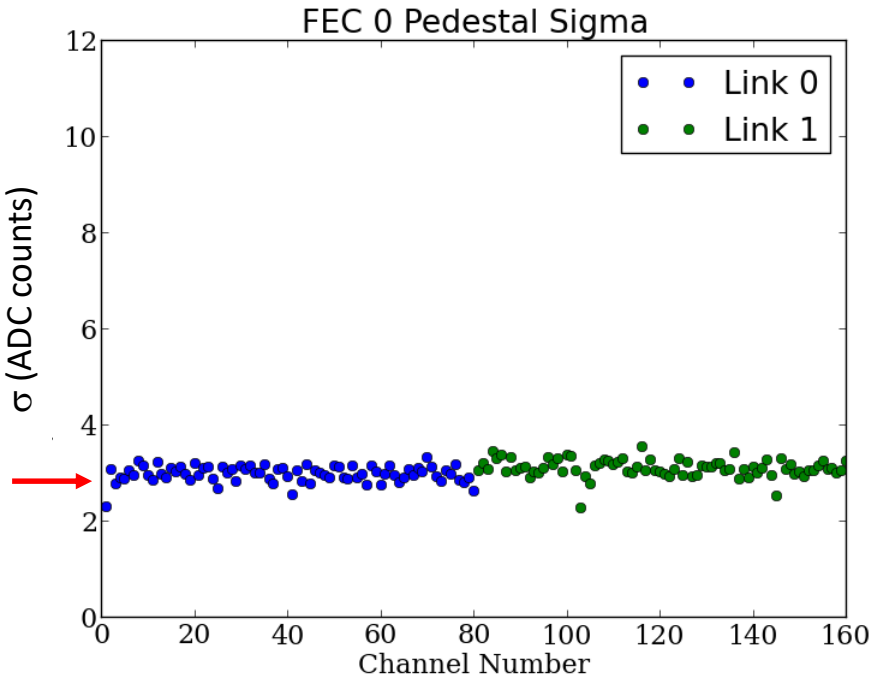
Results of Faraday Cage Shielding

Noise levels of all channels have been reduced and show remarkable uniformity.



All controllable noise sources removed; **NO Faraday cage**

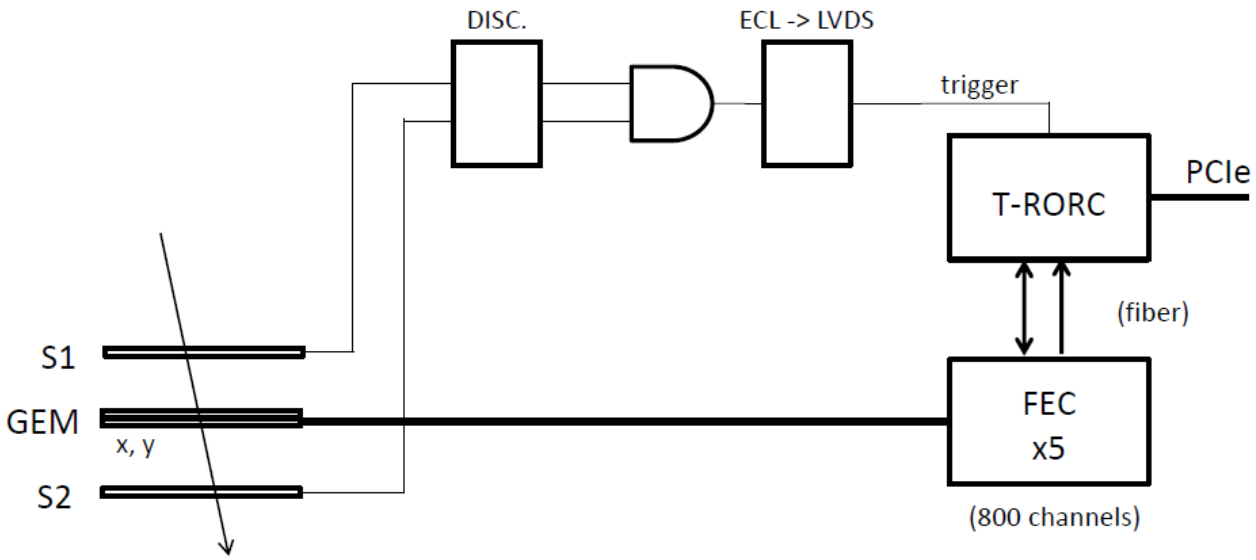
(Raw ADC mode)



All controllable noise sources removed; **Faraday cage installed**

~3 ADC count noise due to capacitance of cables and GEM strips

Cosmic Ray Test Setup



S1, S2 – plastic scintillators

GEM – 1x, 1y plane (384 channels each)

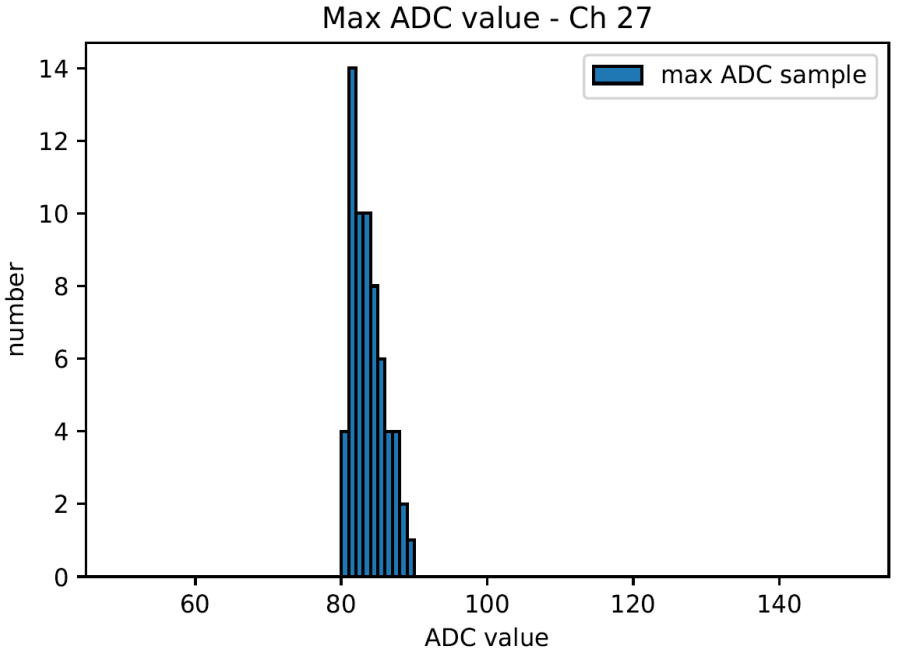
T-RORC – ALICE/ATLAS Read Out Receiver Card with GBT serialization protocol

FEC – ALICE Front End Card (JLAB version) – 5 SAMPA chips (160 channels)

The SAMPA chips are not triggered. Data is continuously streaming from the FECs to the T-RORC. Receipt of a trigger causes a programmable window of streamed data to be captured by the T-RORC. This data is transmitted to the PC memory and written to disk.

Cosmic Ray Data

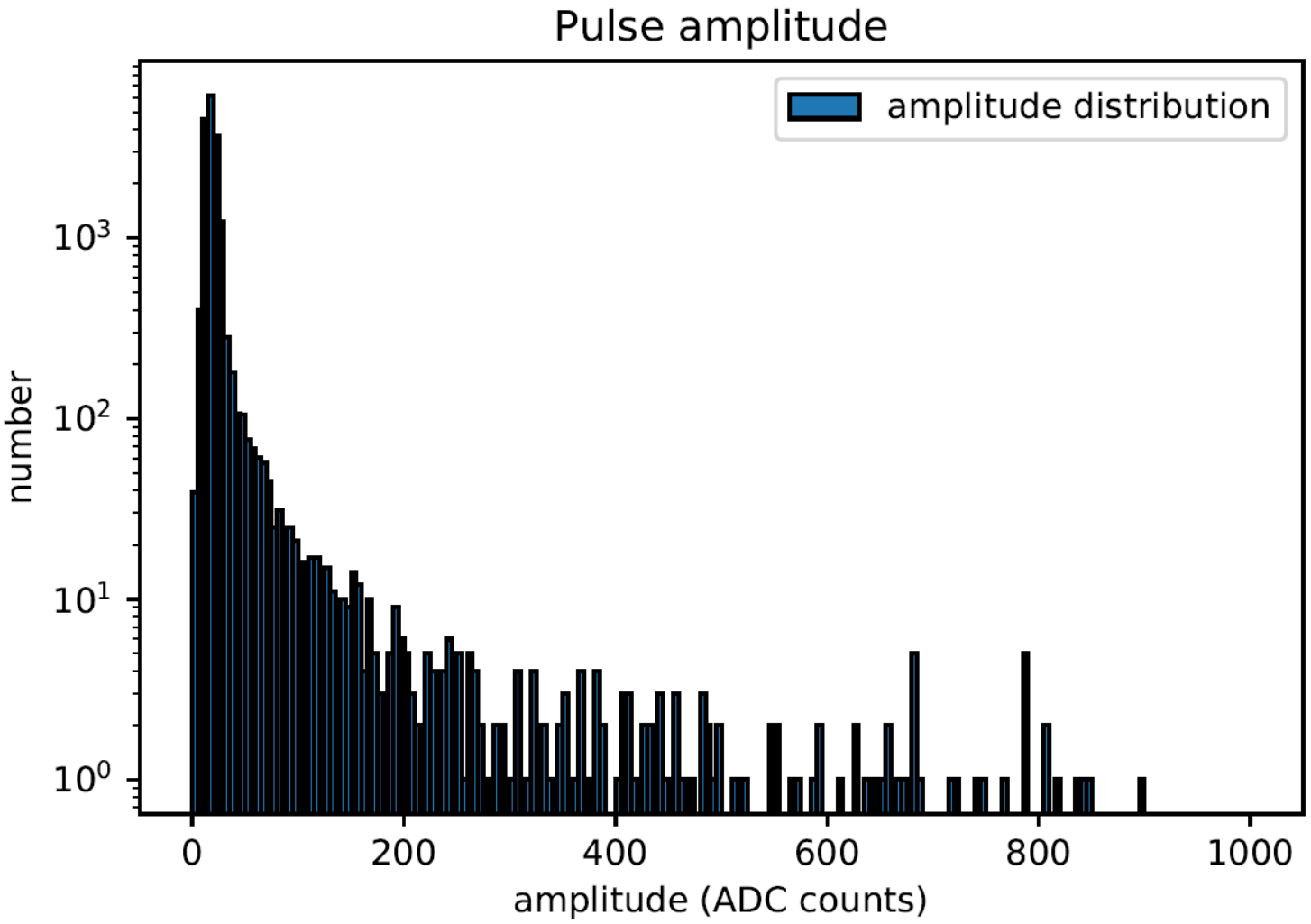
- Use Raw ADC mode run to determine pedestals (no cosmic trigger)
- Set SAMPA thresholds: **Threshold(chan) = Pedestal(chan) + 3*$\sigma_{Pedestal}$(chan)**
- Run in DSP mode (zero suppression) with cosmic trigger
- Low level noise pulses serve to verify programmed thresholds



pedestal = 71.48 σ = 2.80

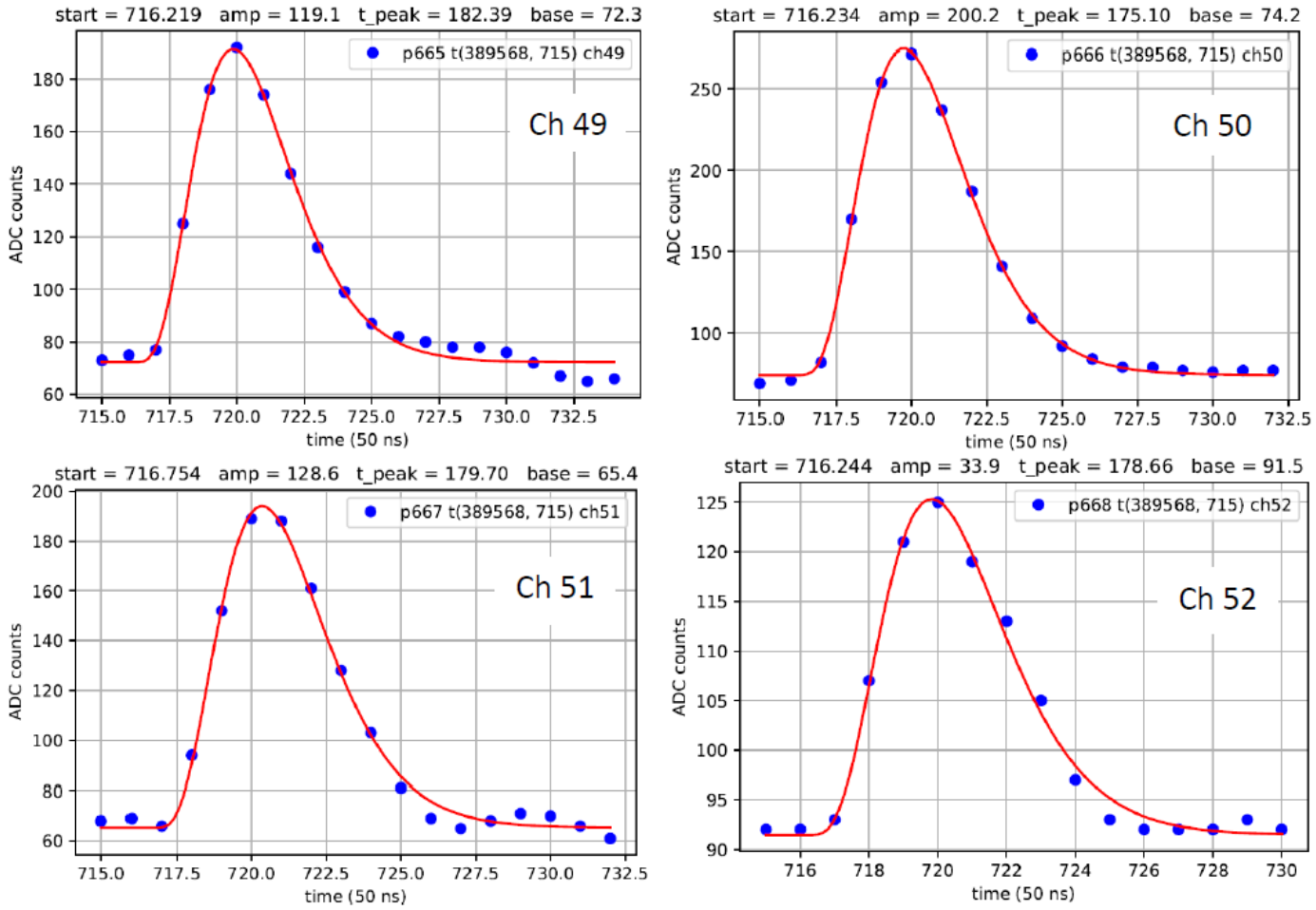
threshold = pedestal + 3*σ = 80

Cosmic Ray Data

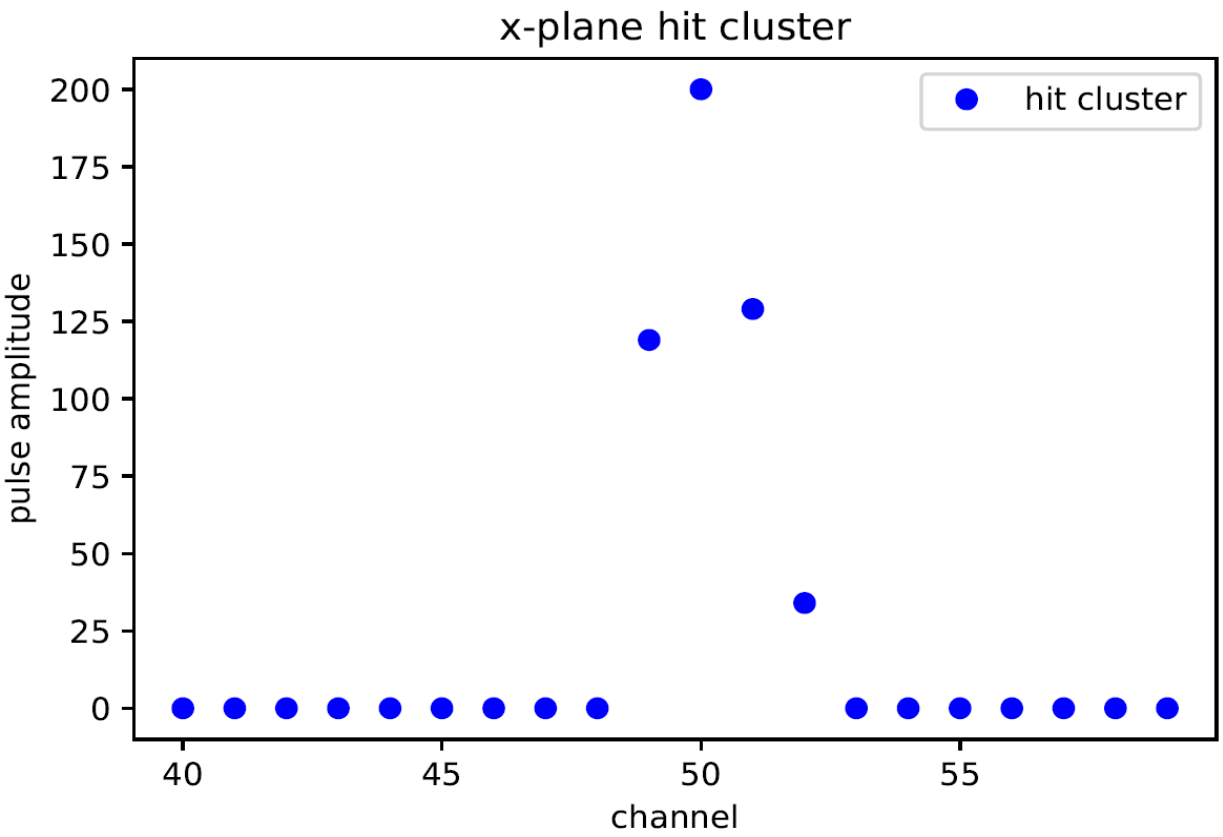


Cosmic Ray Data

Cosmic ray candidate – cluster of adjacent channel hits with close times

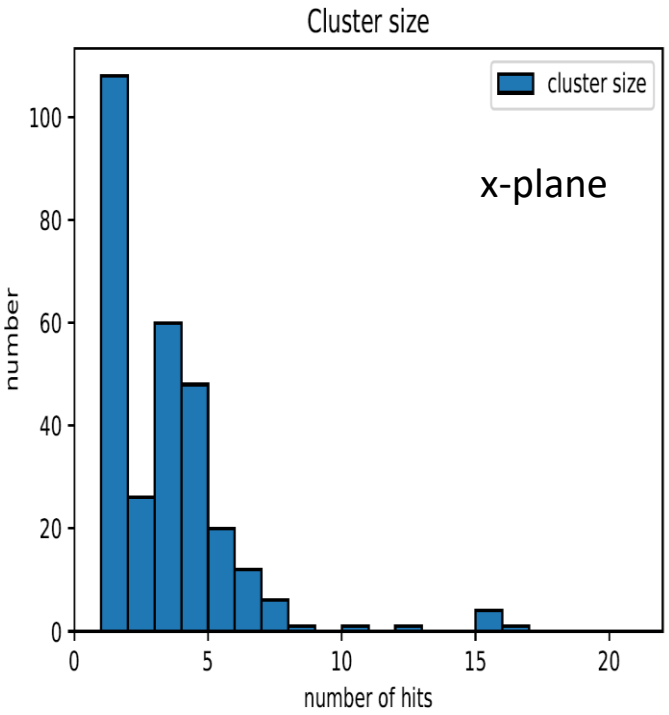


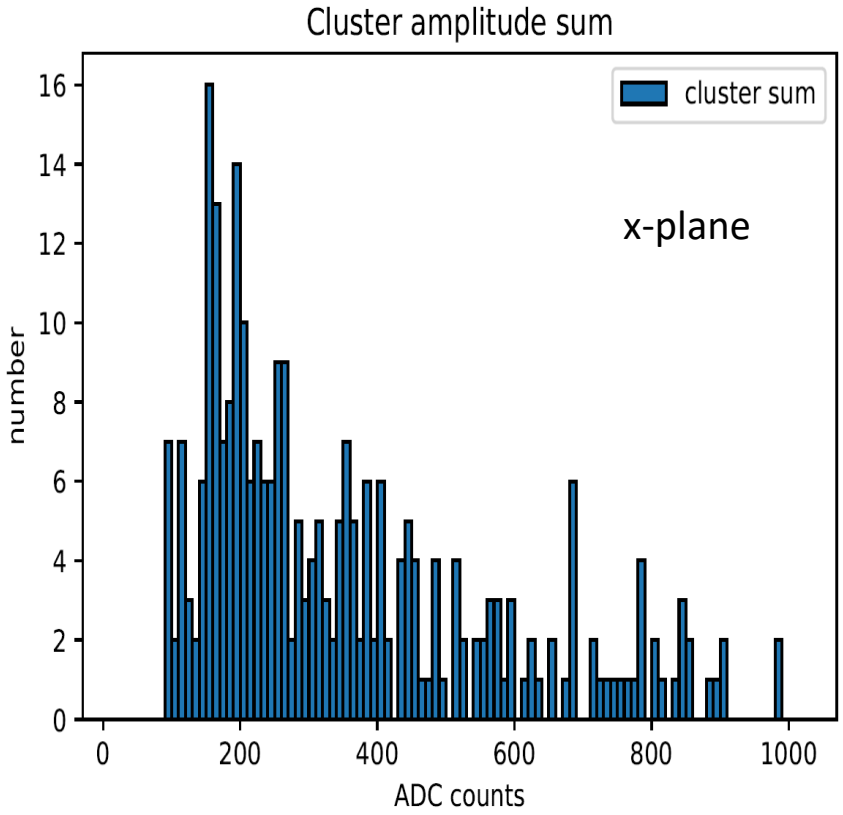
Cosmic Ray Data



Pulse amplitude sum = 482 (48 fC)

Cosmic Ray Data





Cosmic Ray Data

- Developed and coded algorithm for cluster finding in x & y planes. (All data analysis done in Python.)

- Check if distribution of amplitude sums for minimum ionizing cosmic rays is consistent with gain of GEM + SAMPA, and energy loss fluctuations in a thin absorber (Landau distribution)

- **x-plane cluster** should have a corresponding **y-plane cluster** with **close time**

- Working on automated matching of x and y clusters

- Compare cluster amplitude sum of x and y clusters from same particle. (Are they approximately equal?)

- Study timing resolution from matched x and y clusters

- Need more data

SAMPA Test Stand Roadmap

- GEM Readout
  - Continue study of GEM pulse data (e.g. pulse shape, time resolution of correlated hits)
  - Stream continuous GEM data over the network (need help of software heavyweights)

- JLab TDIS (Tagged Deep Inelastic Scattering)
  - Direct triggering of SAMPA chips (non-continuous mode)
  - Readout prototype mTPC (segmented TPC)
  - Construct FECs with new SAMPA V5 chip (80 ns shaping time)

- Integrate FELIX readout hardware/software
  - Use FELIX software to configure FEC (GBTx, GBT-SCA, SAMPA)
  - Modify FELIX firmware for GBT wide bus mode (no forward error correction)
  - Implement pulse feature extraction in FPGA
  - Couple FELIX readout to Jlab data acquisition software

Reference Slides

Useful Sources of Information

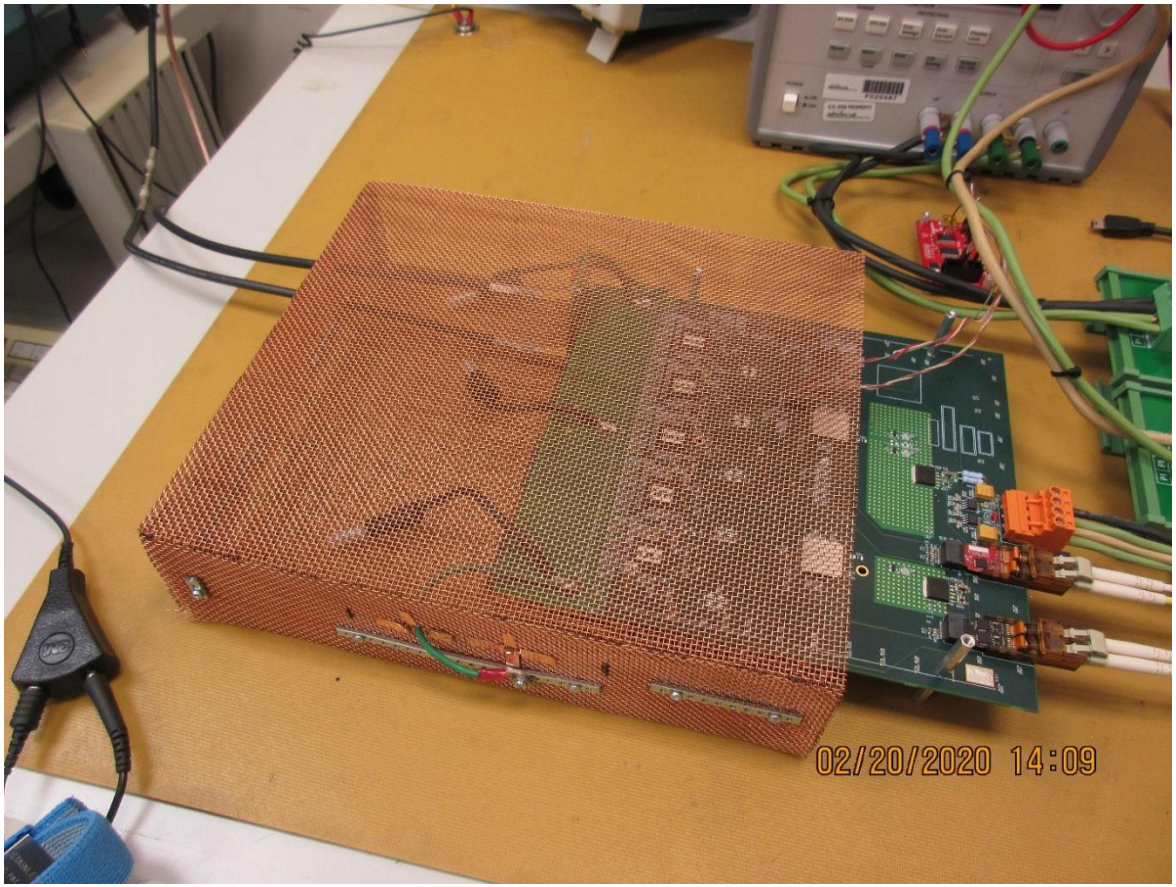
- TDRs for the Upgrade of ALICE
  - https://cds.cern.ch/record/1622286/files/ALICE-TDR-016.pdf
  - http://cds.cern.ch/record/1603472/files/ALICE-TDR-015.pdf

- Other
  - https://www.bnl.gov/aum2014/content/workshops/Workshop_1/bnl_david_silvermyr.pdf
  - http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7031978
  - http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7543104

- SAMPA chip prototype tests
  - http://iopscience.iop.org/article/10.1088/1748-0221/12/04/C04008/pdf
  - http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02088/pdf

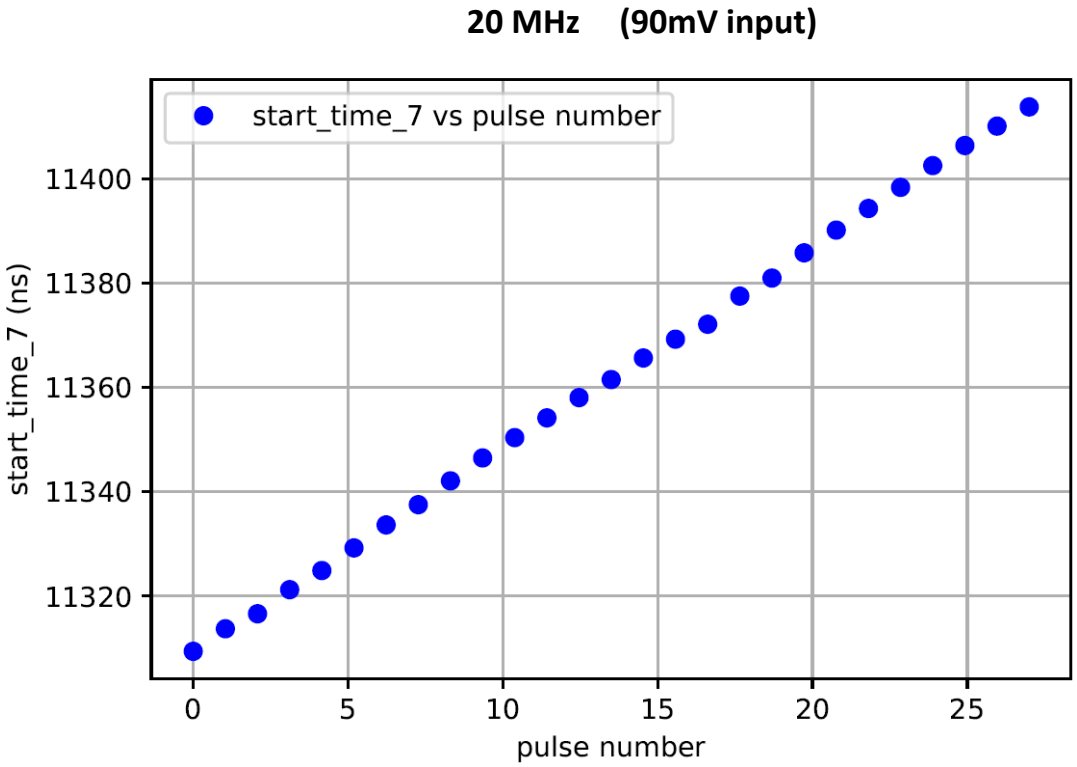
- Collection of links to SAMPA technical documents
  - https://docs.google.com/spreadsheets/d/16SnfEWtvvZYONnxmMhVzUo-St-ZtPRVV3Z6mfy13dRU/edit?usp=sharing

Setup for SAMPA Chip Measurements



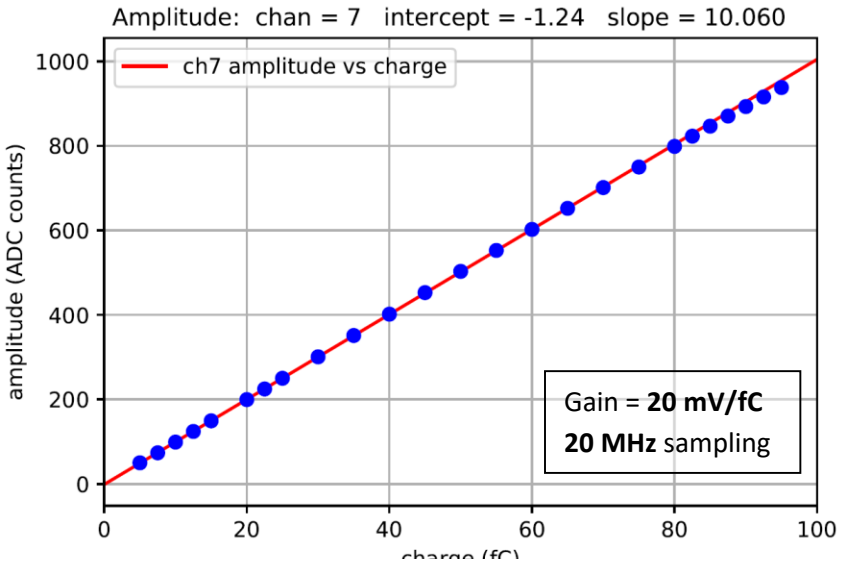
Front end of FEC and test pulse card are shielded from external noise with a small Faraday cage. Input pulses are applied through the pair of coaxial cables on the left.

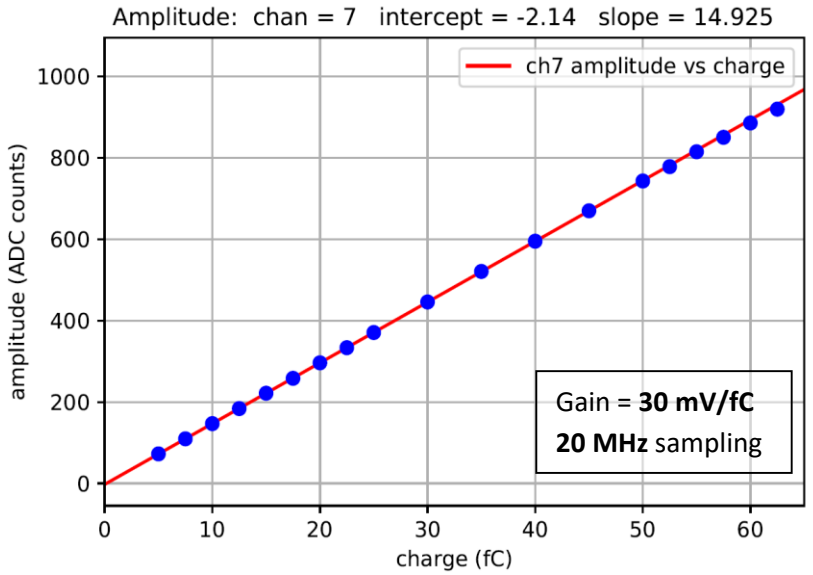
Pulse Walk Relative to ADC Sampling Clock

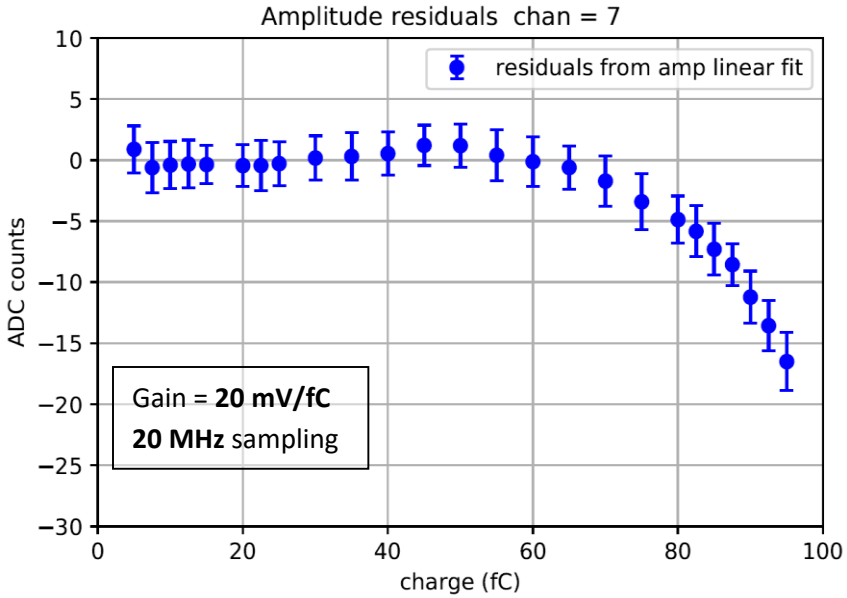


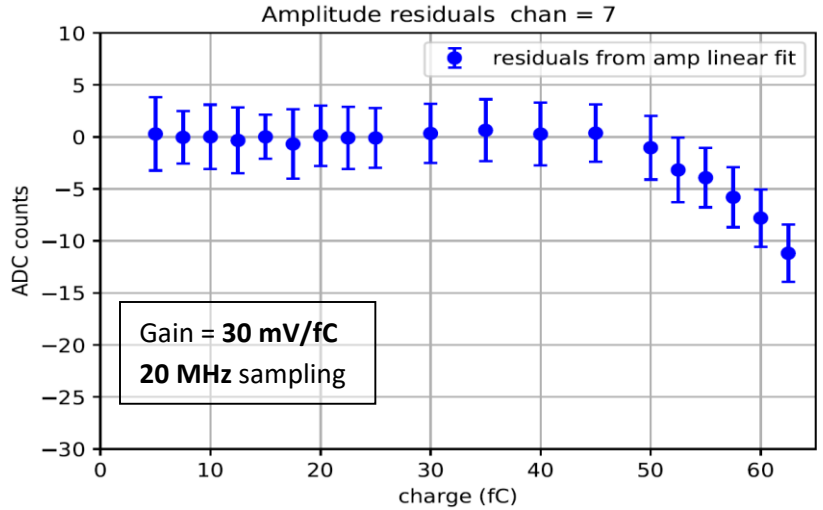
Pulse returns to initial phase relationship with sampling clock after 25 pulses (100 ns = 2 clock periods). Effectively we are placing pulses across the sampling clock period with a step size of 2 ns.

SAMPA Linearity - gain = 20, 30 mV/fC

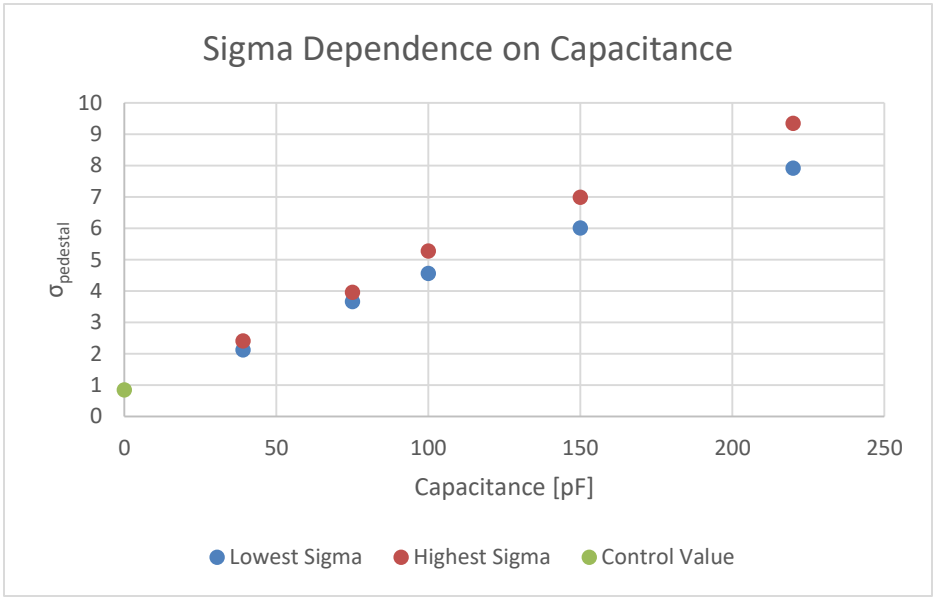








Effect of Input Capacitance on SAMPA Noise



Equivalent Noise Charge

$$\text{ENC} = \frac{\text{rms output noise(ADC counts)}}{\text{gain(ADC counts/fC)}}$$

In the linearity study the gain was determined to be 10.06 ADC counts/fC. For an rms noise of 1 ADC count (noting that 1 fC = 6241 electrons):

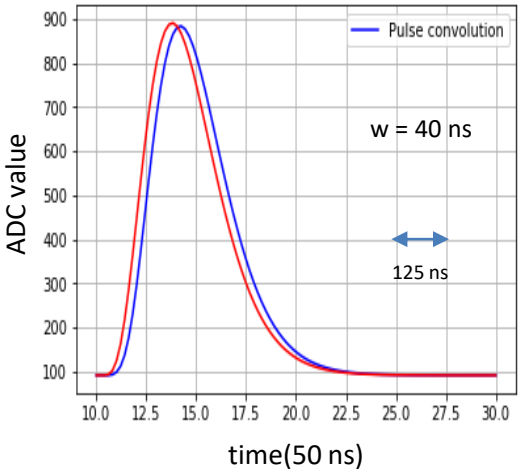
ENC(1) = 0.0994 fC = 620 electrons

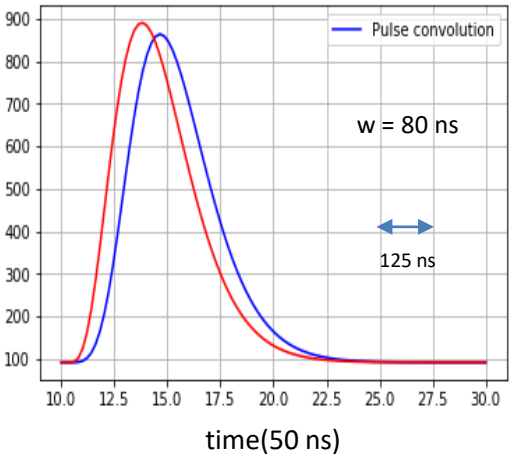
σ

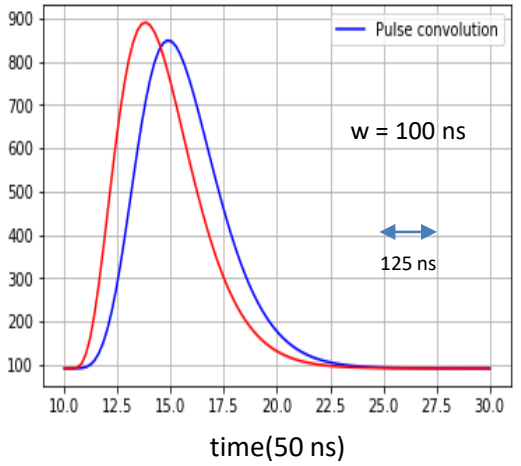
Cap [pF]	Ch. 1	Ch. 11	Ch. 21	Ch. 31	Ch. 39	Average
220	7.92	8.05	8.15	8.62	9.35	8.42
150	6.10	6.01	6.30	6.62	6.99	6.40
100	4.56	4.61	4.73	4.89	5.28	4.81
75	3.68	3.67	3.73	3.93	3.96	3.79
39	2.31	2.20	2.13	2.28	2.41	2.27

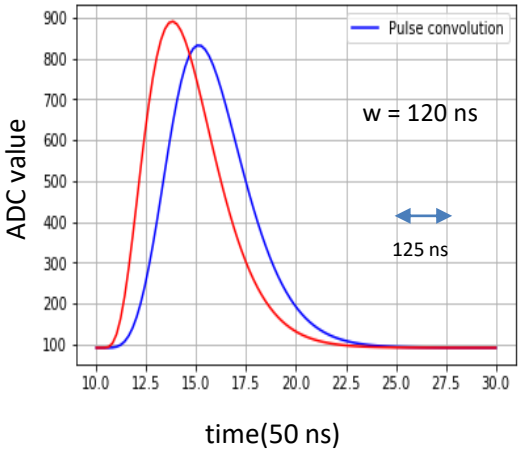
Cap [pF]	Average Charge (fC)	Average Number of Electrons
220	0.837	5224
150	0.636	3970
100	0.478	2984
75	0.377	2351
39	0.226	1408

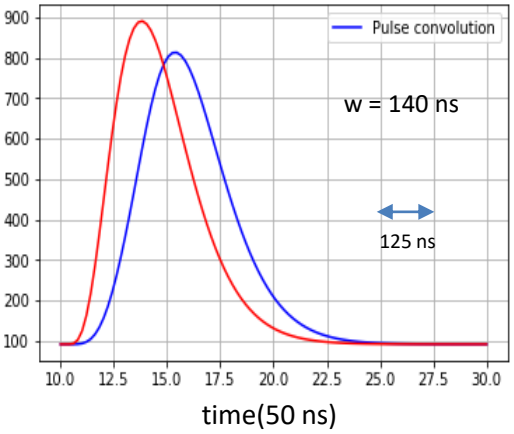
Effect of Charge Collection Time on SAMPA Pulse Shape





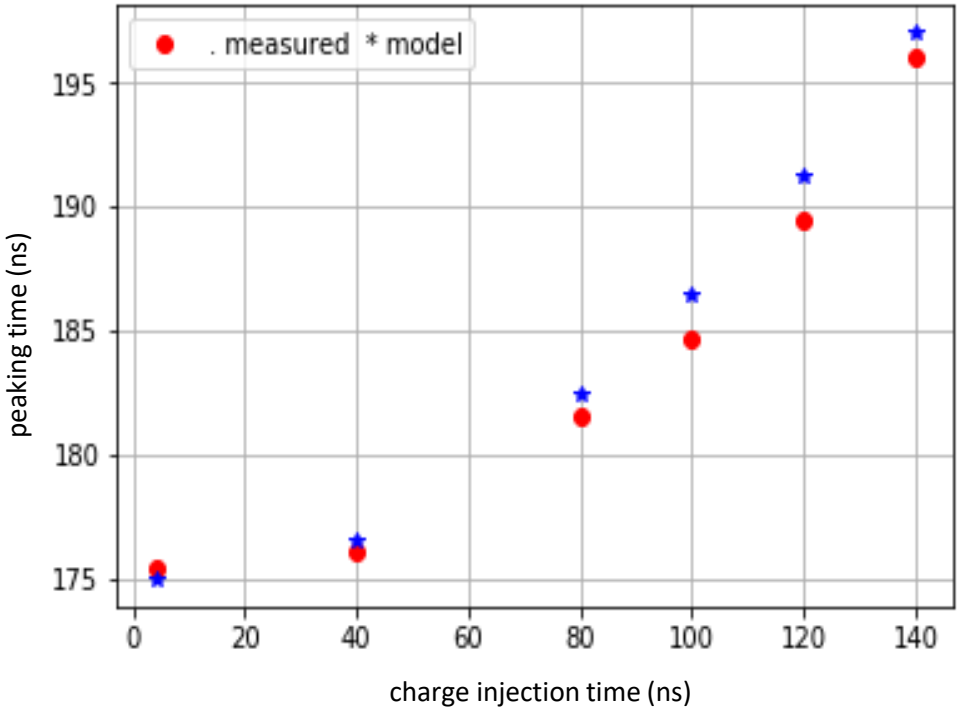






Predicted SAMPA pulses (blue) for injected charge that is uniformly distributed over the specified time periods. The total charge (80 fC) and the start time (10.3) are the same for all cases. The RED curves are the SAMPA impulse response (80 fC) and are shown in each plot for comparison. The horizontal scales are in units of 50 ns.

Effect of Charge Collection Time on SAMPA Pulse Shape

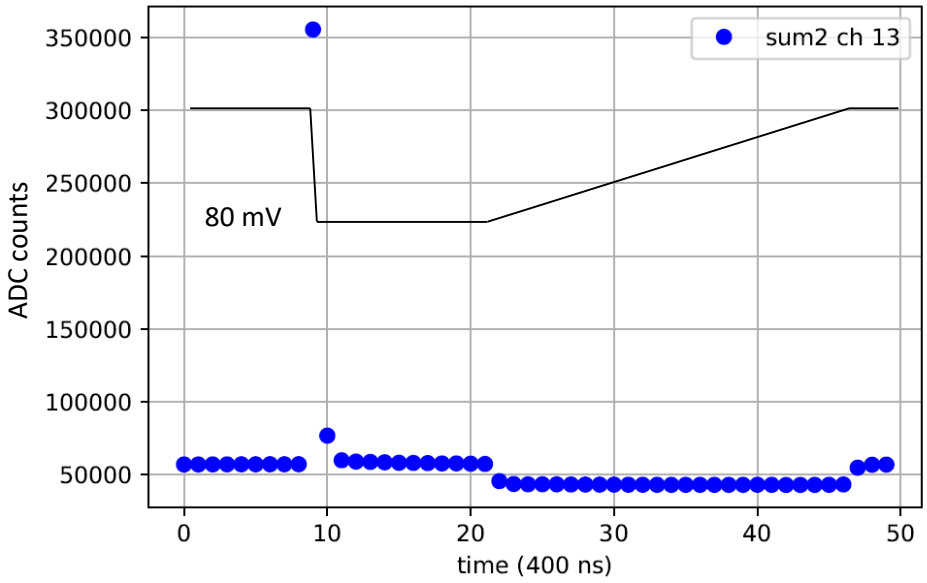


Comparison of peaking time fits for model and measured data for different charge injection periods. The fits are to the SAMPA impulse shape. The data above confirms that the SAMPA impulse shape function with increased peaking time is adequate to model extended charge collection times in a detector.

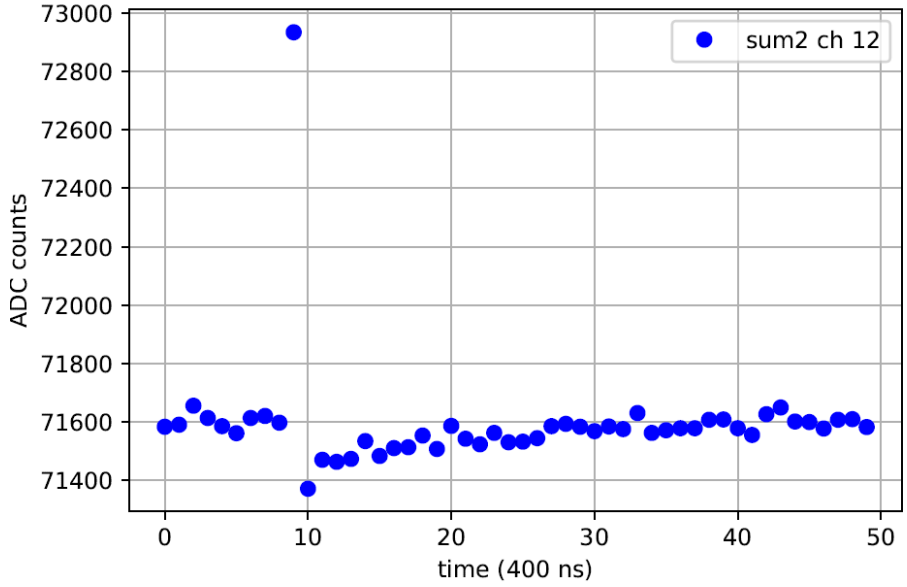
SAMPA Crosstalk Study

Apply a large amplitude (80 mV) pulse to a channel and inspect adjacent channels for a signal. Use DAS mode where raw ADC samples at 5 MHz are continuously streamed off chip for all channels. Visibility of crosstalk signal is enhanced by summing samples of many pulses (400). Two samples at 5 MHz essentially capture all of the pulse, so add consecutive samples in pairs (defining an effective sample period of 400 ns).

SAMPA Crosstalk



Driven Channel 13
amp(13) = 298434
(Driving waveform shown)

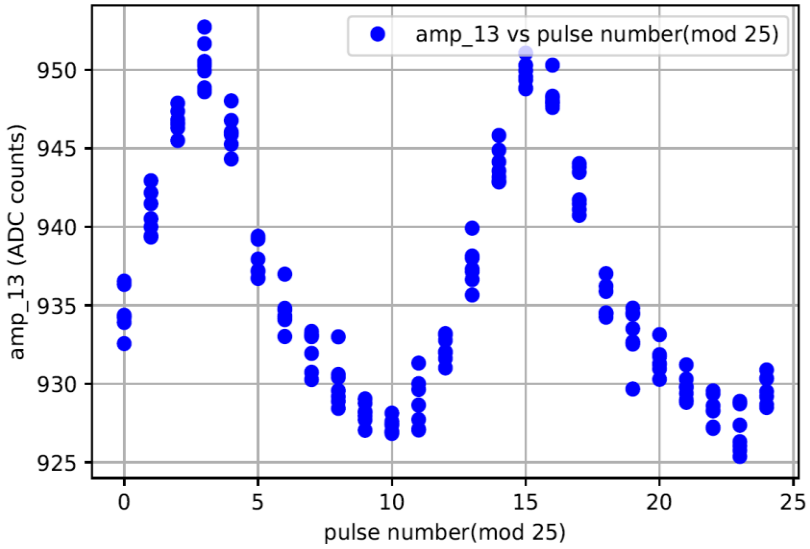


Adjacent Channel 12
amp(12) = 1330

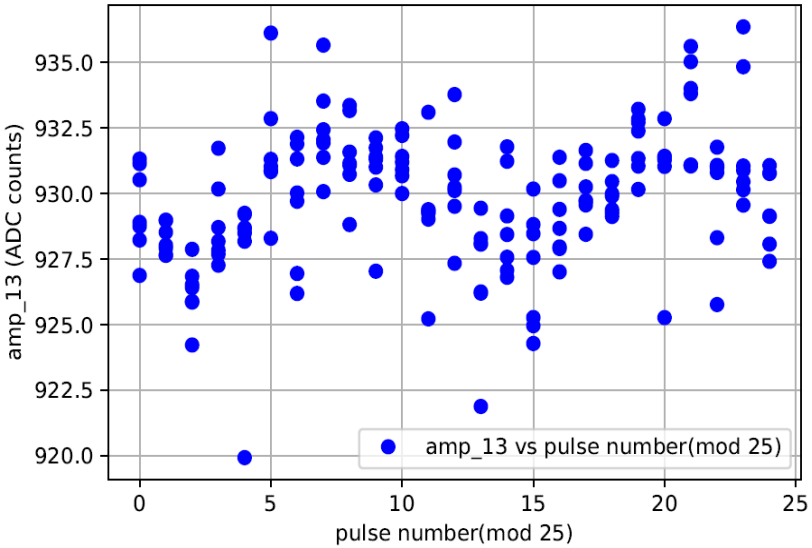
xtalk = amp(12)/amp(13)
= 0.45%

Effect of Pulse Time Shift Relative to Sampling Clock on Fit Amplitude

10 MHz

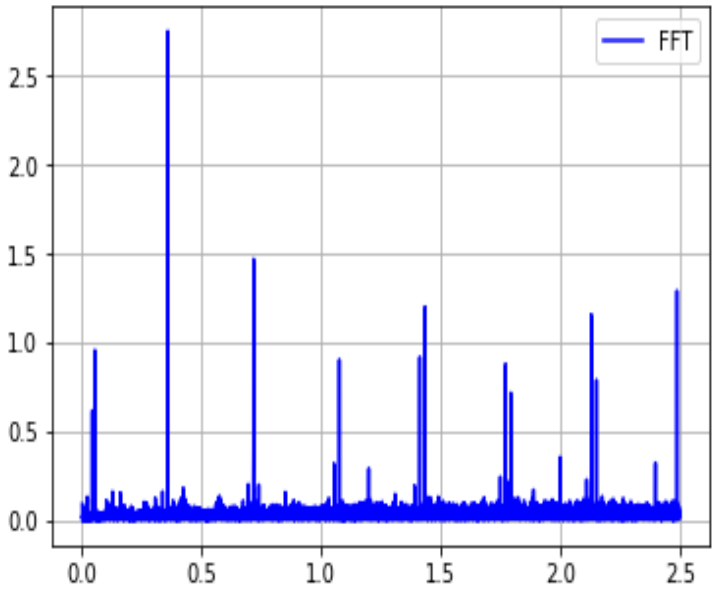


20 MHz

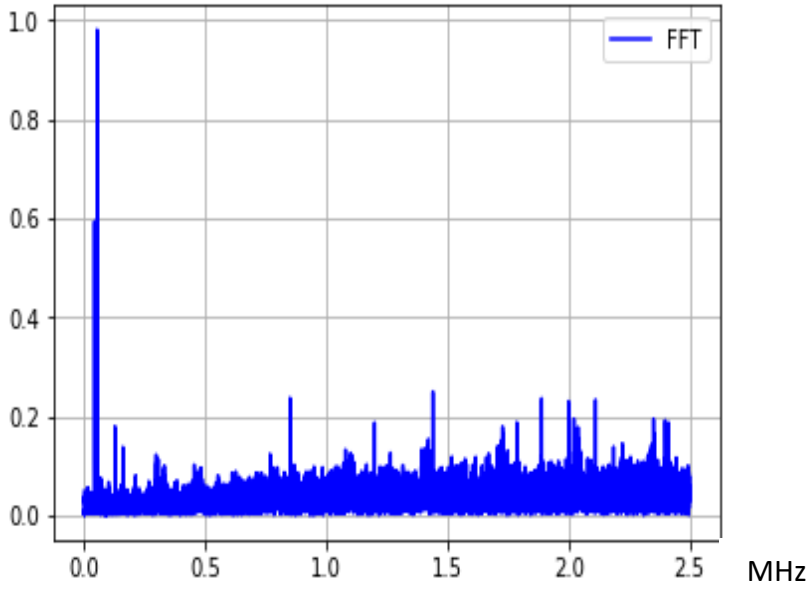


95 mV pulse input (gain = 20 mV/fC)

Using FFT to Study System Noise (Raw ADC mode)



Bus Pirates connected, USB hub powered



Bus Pirates disconnected, USB hub not powered

Pulse Integral

Computation of the Pulse Integral

Suppose a SAMPA pulse in zero suppression mode is represented by N sample values: ADC[0], ADC[1], … , ADC[N-1]. Assume we have requested that 3 pre-samples (samples before threshold crossing) and 7 post-samples (samples after return below threshold) be included so that the baseline (pedestal) can be identified for each pulse. The pre-samples are ADC[0], ADC[1], ADC[2]; the post-samples are ADC[N-7], ADC[N-6], ADC[N-5], ADC[N-4], ADC[N-3], ADC[N-2], ADC[N-1].

We estimate the baseline level as the average of the 6 outermost samples (2 pre, 4 post):

BASE_AVG = AVG(ADC[0], ADC[1], ADC[N-4], ADC[N-3], ADC[N-2], ADC[N-1])

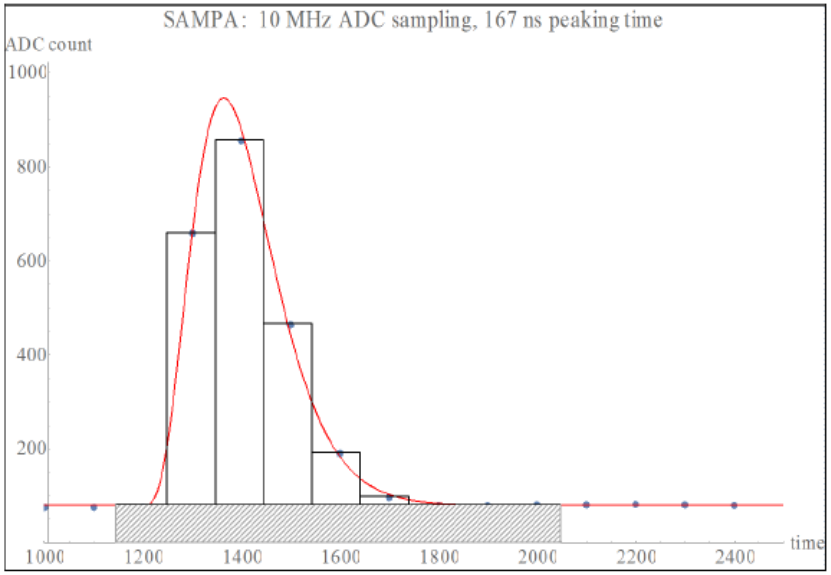
The remaining N-6 samples contribute to the pulse integral (ADC[2], … , ADC[N-5]).

Define the baseline sum as:

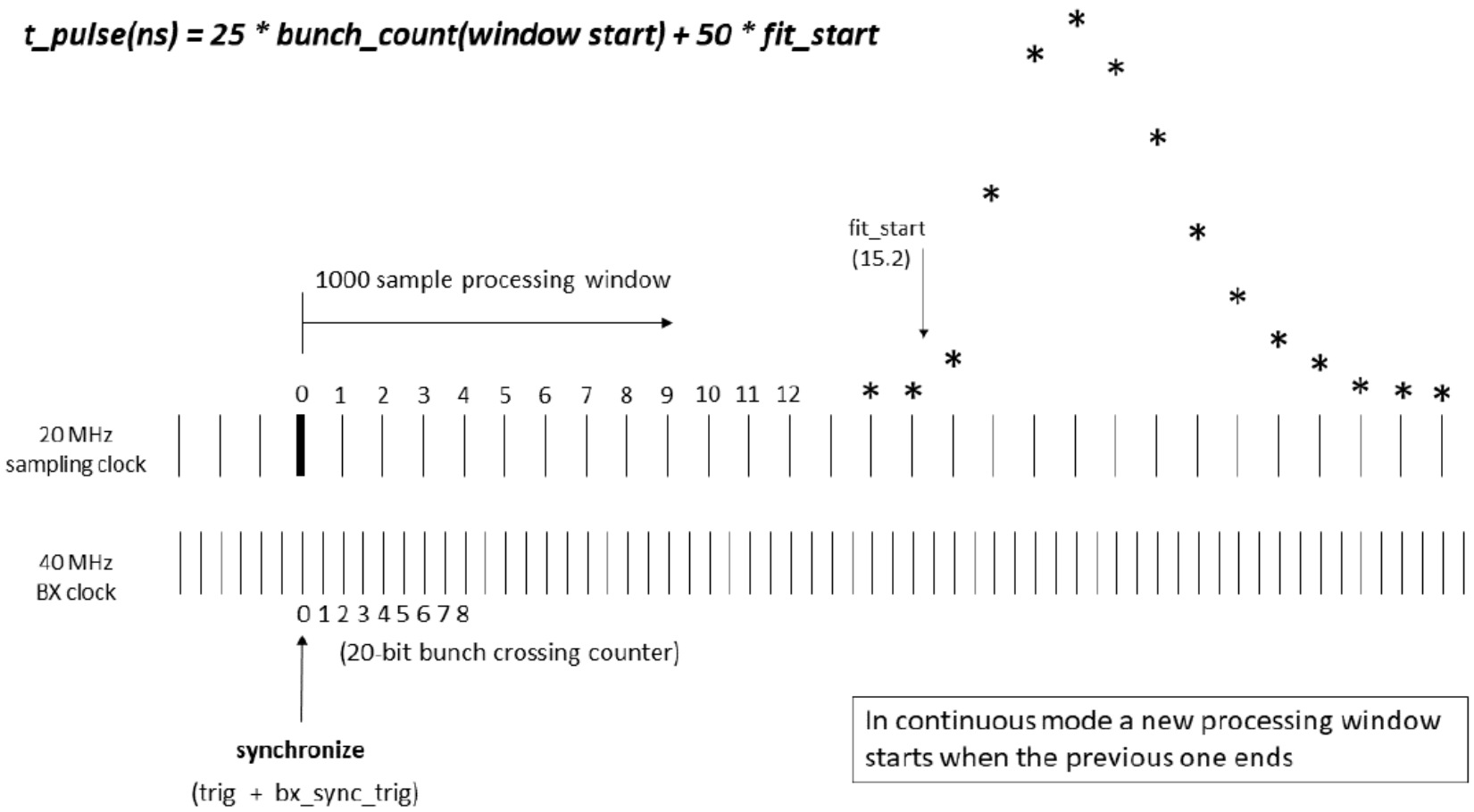
BASE_SUM = (N-6) * BASE_AVG

The estimate of the pulse integral is:

PULSE_INTEGRAL = SUM(ADC[2], … , ADC[N-5]) - BASE_SUM



Determining the Pulse Time



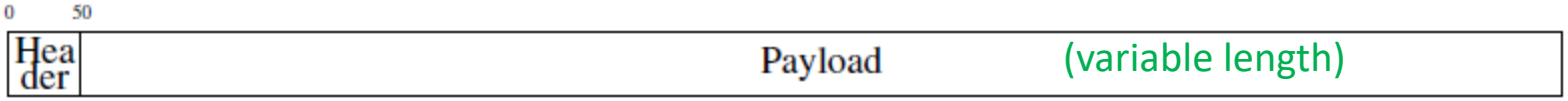
SAMPA Sync and Trigger inputs

- **hb_trg** - a pulse on this input causes the capture of the beam crossing count and a heartbeat packet is created
- **trg** - this is the event trigger when running in triggered mode. When running in continuous mode a pulse on this input causes a new time frame to be started and so is effective in synchronizing multiple devices.
- **bx_sync_trg** - a signal on this input will reset the bunch crossing counter and so serves to synchronize this counter across multiple devices

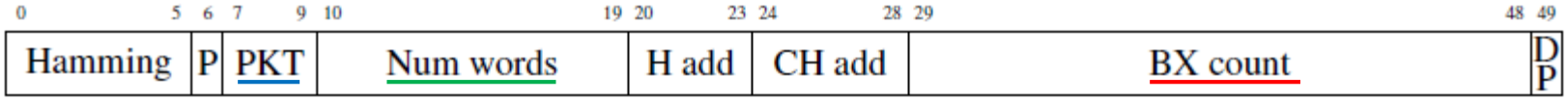
SAMPA packets

- Besides the data type packet (e.g. zero suppression encoding) the SAMPA can produce some special packets
- Heartbeat packet – generated as a result of a signal on the heartbeat trigger pin
  - No payload; conveys only bunch crossing count
  - Sent only on serial link 0
  - Highest priority; sent immediately after current packet has completed transmission
  - Used as a marker in the data stream

SAMPA packet



Packet header



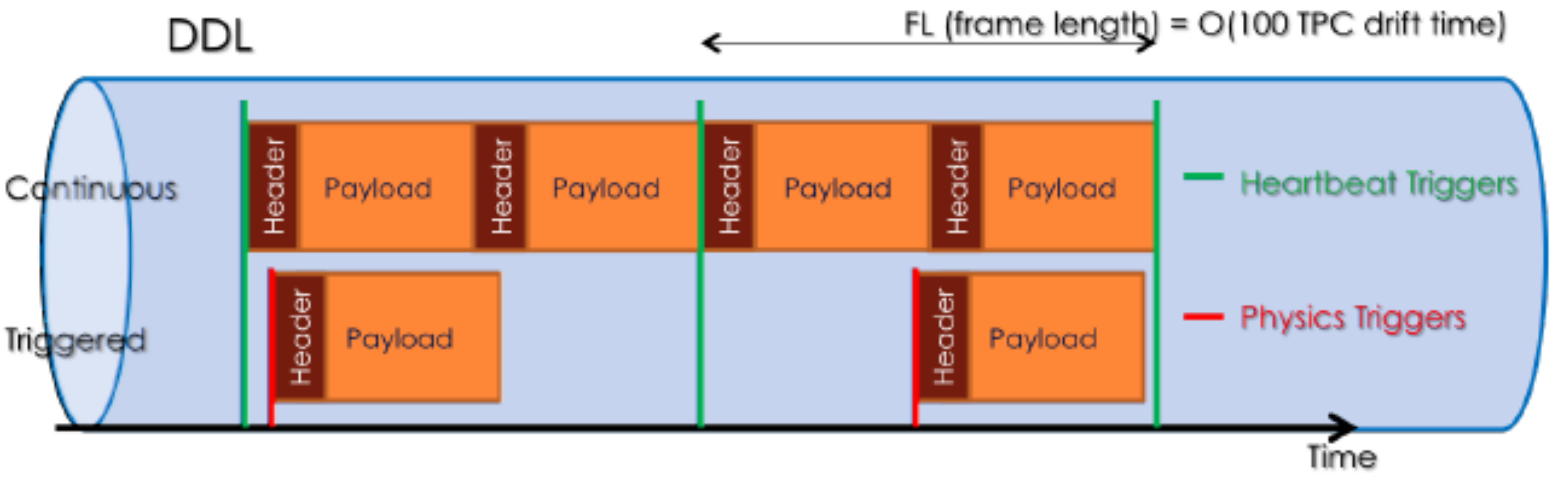
Name	Bits	Description
Hamming	6	Hamming code
P	1	Parity (odd) of header including hamming
PKT	3	Packet type, see table 2.6
Num words	10	Number of 10 bit words in data payload
H add	4	Hardware address of chip
CH add	5	Channel address
BX count	20	Bunch-crossing counter (40MHz counter)
DP	1	Parity (odd) of data payload

Time stamp

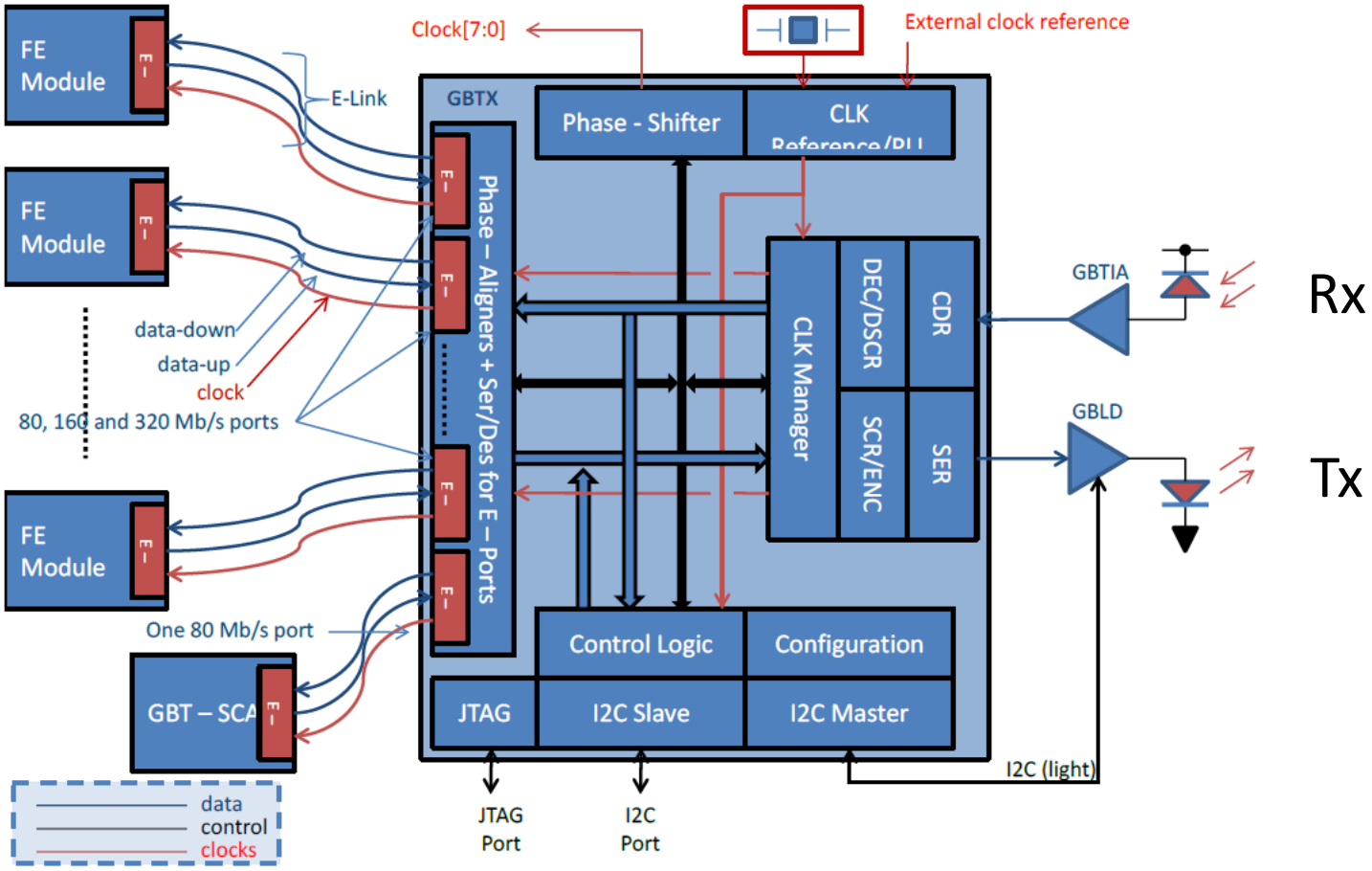
Linking Triggered and Continuous Data

- All data packets from both triggered and continuous sources are time stamped with bunch crossing number
- Heartbeat Trigger
  - Non-physics trigger generated by Central Trigger Processor (CTP)
  - Regular frequency, highest priority
  - All detector readout systems respond by inserting a “Heartbeat Event”
  - These events separate the data streams into pieces (heartbeat time frames) that are used in event building
  - Event building nodes get different frames; data associated with trigger near end of frame may extend to *next* frame, so at least part of the next frame must also be sent to node (unless small data loss allowed)
  - Can also be used as a synchronization event: by sending global time stamp with heartbeat trigger, detector readout unit can compare with its local time stamp and report/correct difference

Heartbeat Trigger



GBTX architecture

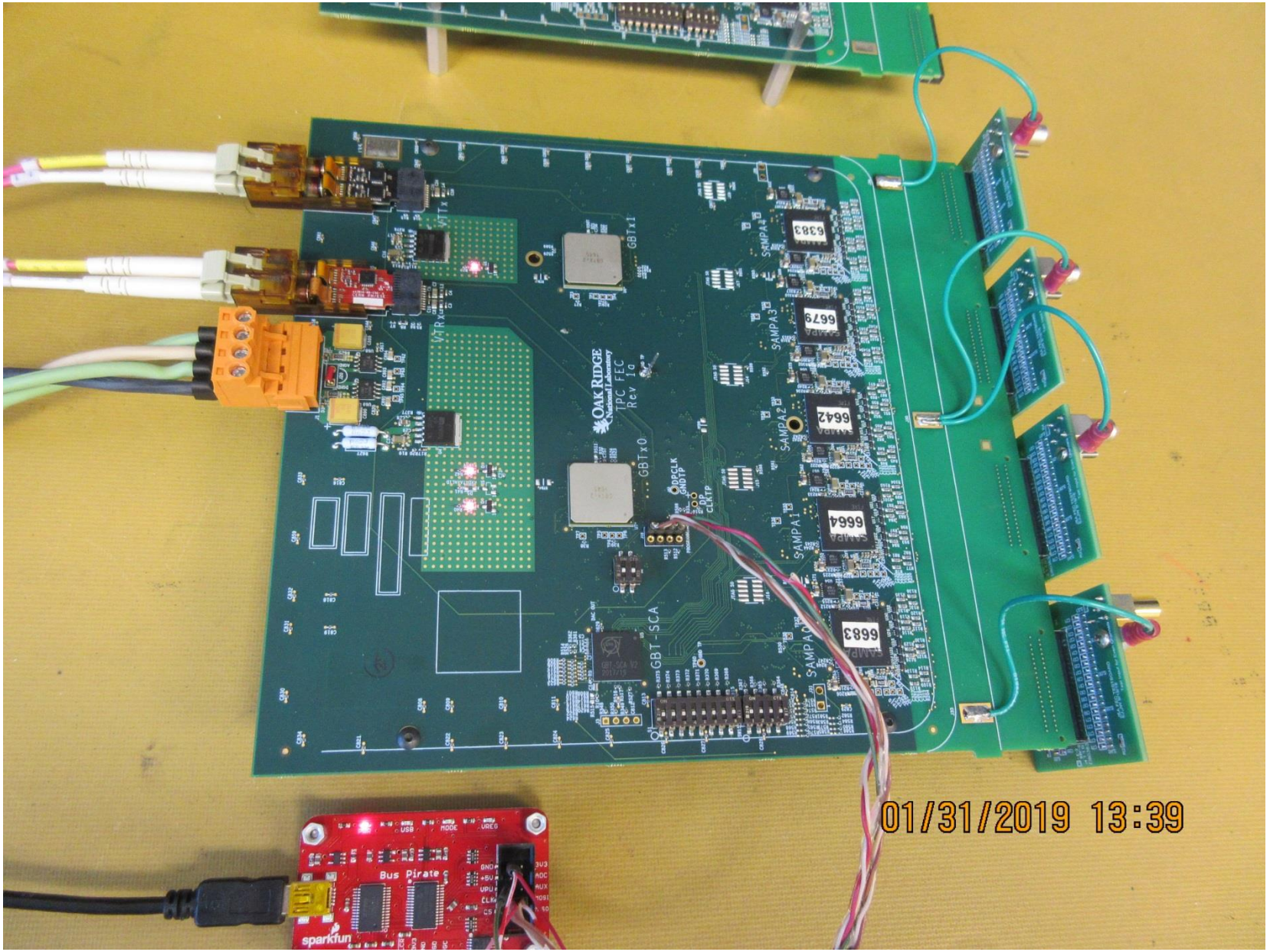


E-Link - Electrical serial link (SLVS)

GBTx E-Link Groups

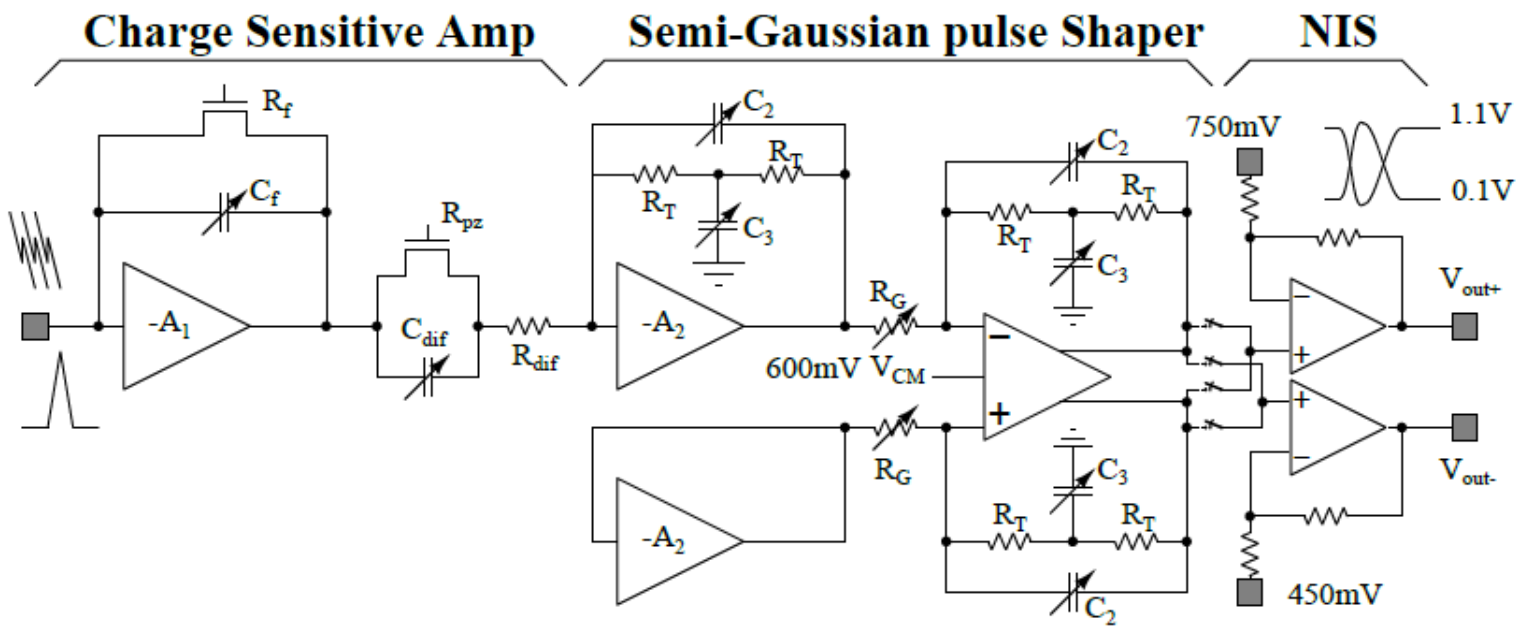
- 5 E-link groups for normal mode, 7 E-link groups for wide mode
- Each E-link group of GBT frame is assigned 16 bits of data in frame
- Flexible E-link speed (frame rate = 40 MHz)

type	# E-links in group	bits per E-link	E-link speed
8x	8	2	80 Mb/s
4x	4	4	160 Mb/s
2x	2	8	320 Mb/s



FEC with 4 test pulse cards installed

SAMPA Analog Front-end Details



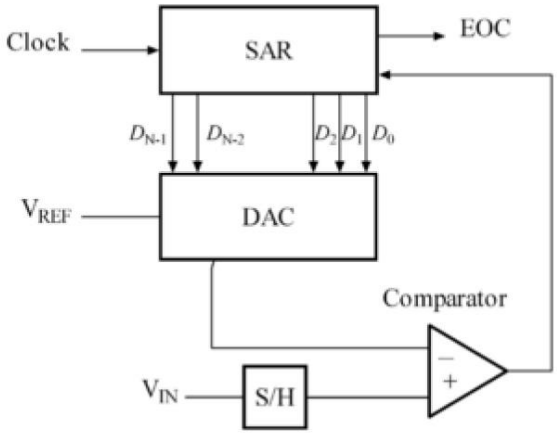
- Negative and positive polarity CSA with capacitive and resistive feedback connected in parallel
- Pole-Zero Cancellation network
- High pass filter
- Two bridged-T second order low pass filters
- Non-inverting stage

Analog Front-end Details

- First shaper is a scaled down version of the CSA and generates two first poles and one zero
- Copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage
- Second stage of the shaper is a fully differential second order bridged-T filter and it includes a Common-Mode feed back network
- Non-inverting stage adapts the DC voltage level of the shaper to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifier.

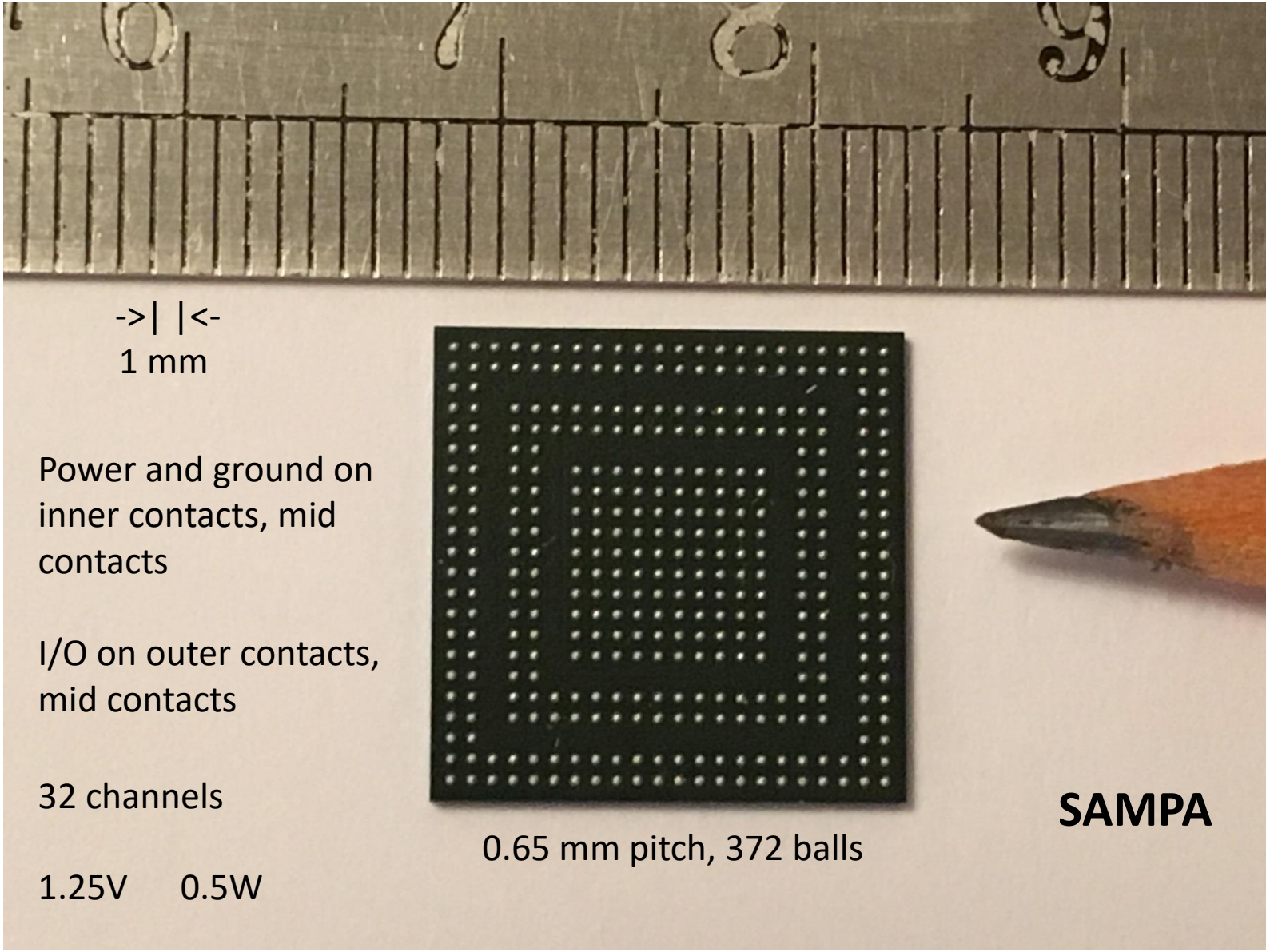
Gain	Shaping time
30mV/fC	160 ns
20mV/fC	160ns
4mV/fC	300 ns

Successive Approximation ADC

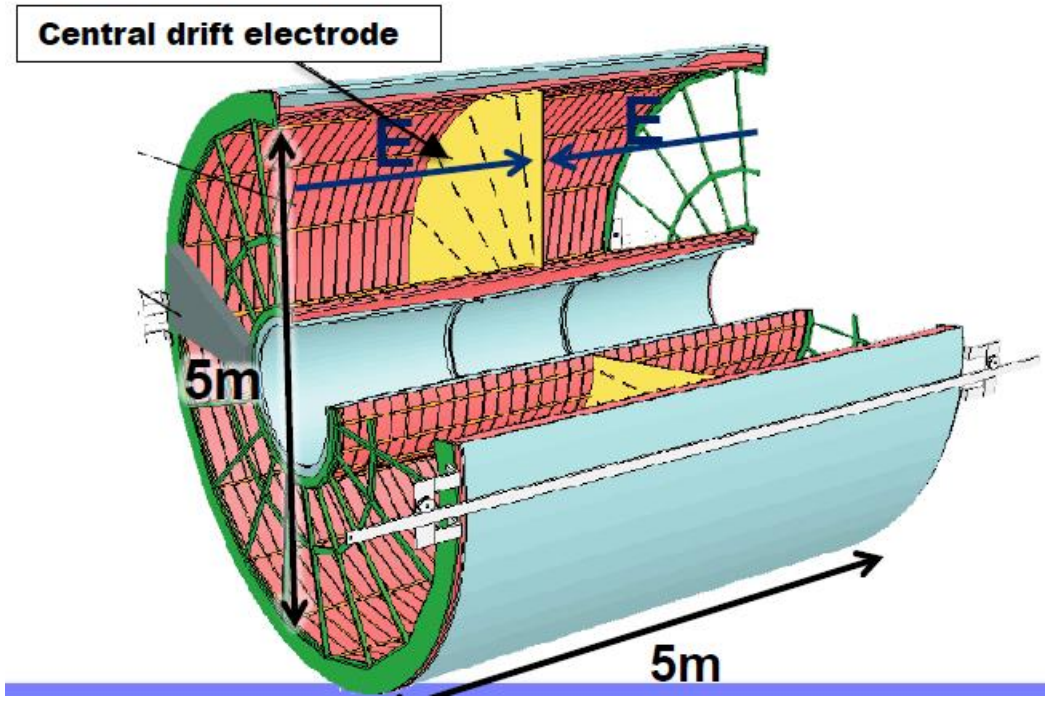


Successive Approximation ADC Block Diagram

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

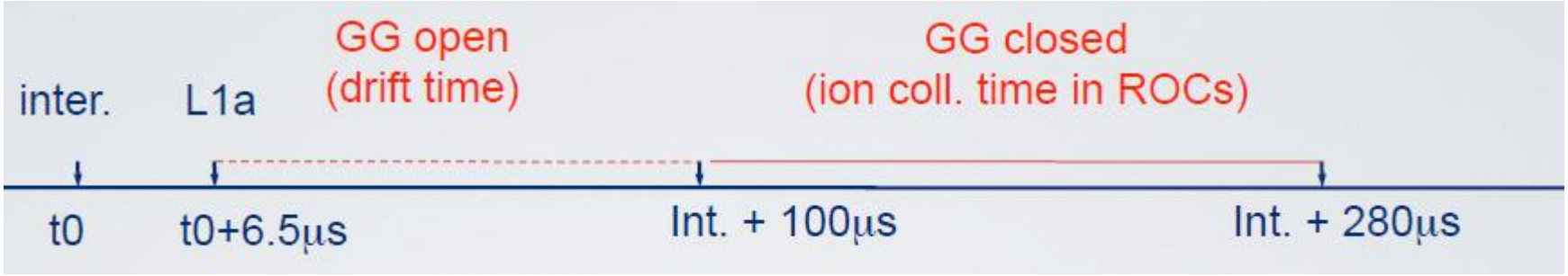

->| |<-
1 mm
Power and ground on inner contacts, mid contacts
I/O on outer contacts, mid contacts
32 channels
1.25V 0.5W
0.65 mm pitch, 372 balls
SAMPA

Background - ALICE TPC



Volume = 90 cubic meters (largest in world)
~ 100 us electron drift time (90% Ne – 10% CO2)
Current detector – MWPC (end plates) (0.5 M channels)

ALICE TPC



ROC = Read out chamber

Active Gating Grid - trigger causes grid to be transparent, allowing ionization electrons to pass into the amplification region. After 100 us, Gating Grid is biased with alternating voltage that renders grid opaque to electrons and ions. This protects the amplification region against unwanted ionization from the drift region, and prevents back-drifting ions from entering the drift volume (leading to drift-field distortion).

Trigger rate limited to 3.5 KHz

LHC Luminosity Upgrade

- LHC Run 3 (**2021**) → 50 KHz interaction rate (Pb-Pb)
- ~ 5 events (100 us * 50 KHz) concurrent in TPC volume
- TPC Gating grid would cause large loss of data
- Replace MWPC with **quad-layer GEM detectors** (resistant to backflow of ions into drift volume).
- Continuous readout of TPC data desirable (~1 TByte/s)
- **New ASIC developed** – requirements set to meet needs of both TPC and Muon chambers