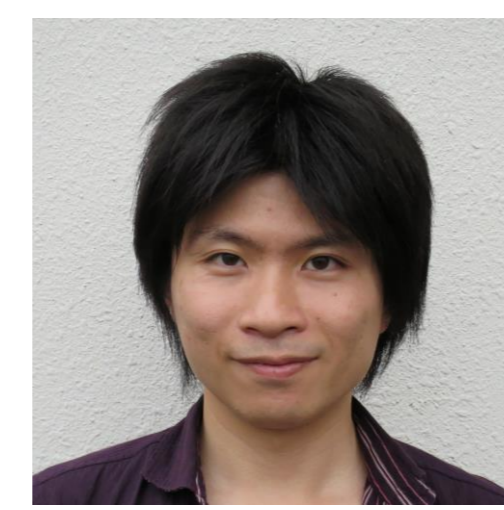


Gigabit Ethernet Daisy-Chain on FPGA for COMET Read-out Electronics

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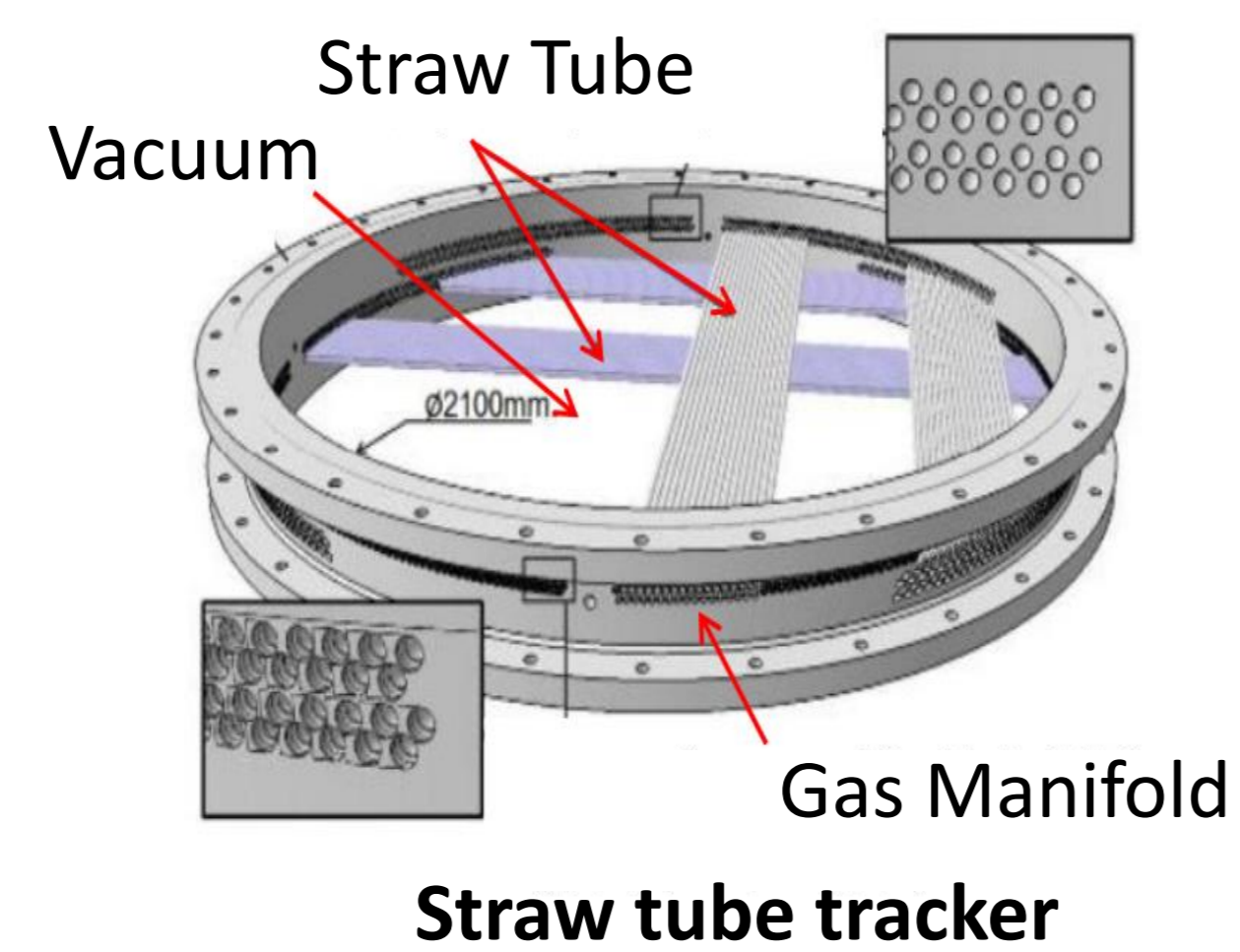


Introduction

[COMET Experiment]

The COMET experiment at J-PARC aims to search for the neutrinoless transition of a muon to an electron ($\mu-e$ conversion). Since $\mu-e$ conversion is strictly forbidden in the Standard Model, it would be the clear evidence of the new physics if it is found.

In order to suppress the background and to achieve the goal sensitivity, we adopt a straw tube tracker for the electron detector.

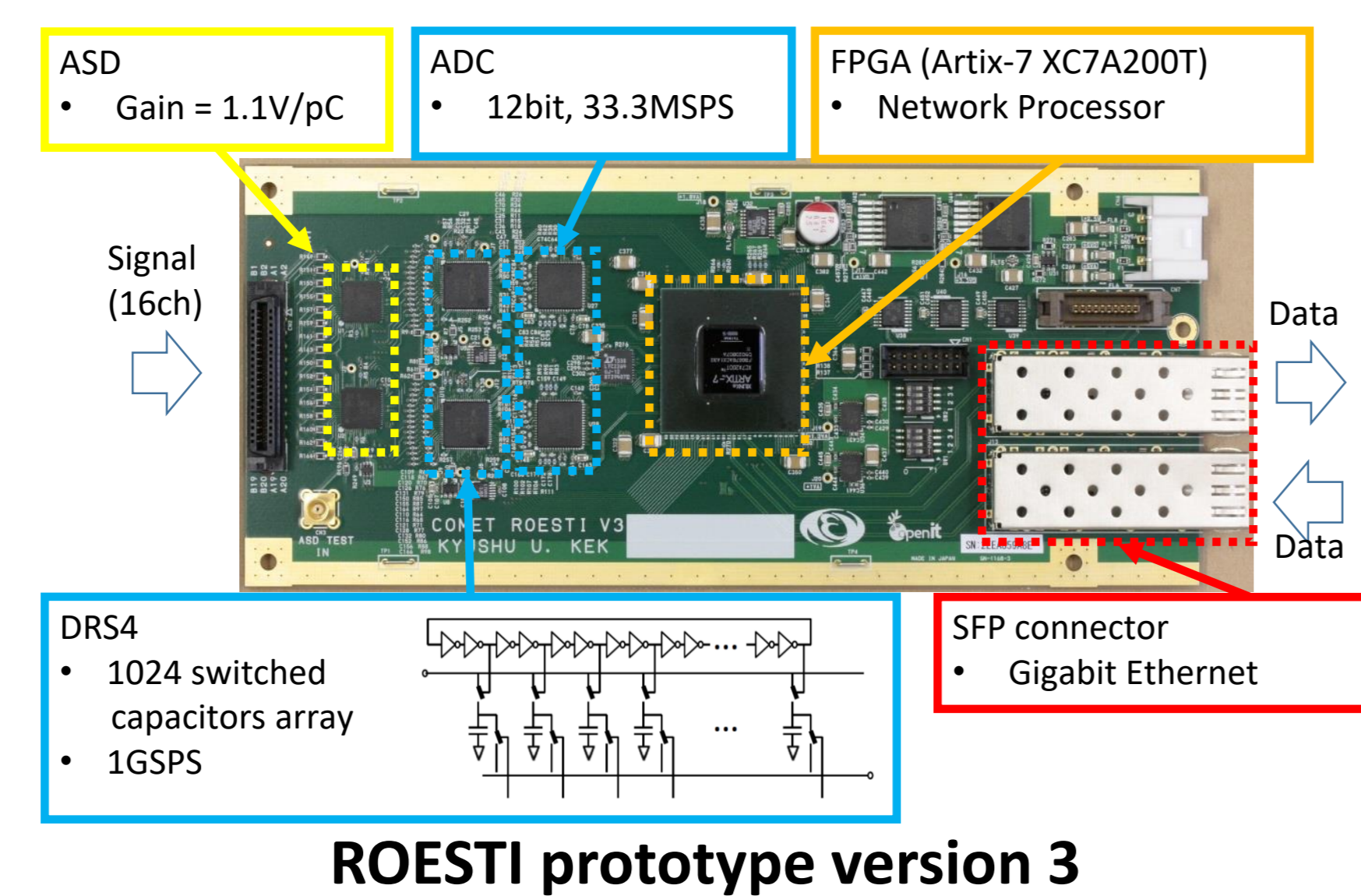


[Straw Tube Tracker]

Since the detector is composed of an extremely light material which is operational in a vacuum, an excellent momentum resolution of better than 200 keV/c is achieved.

[ROESTI]

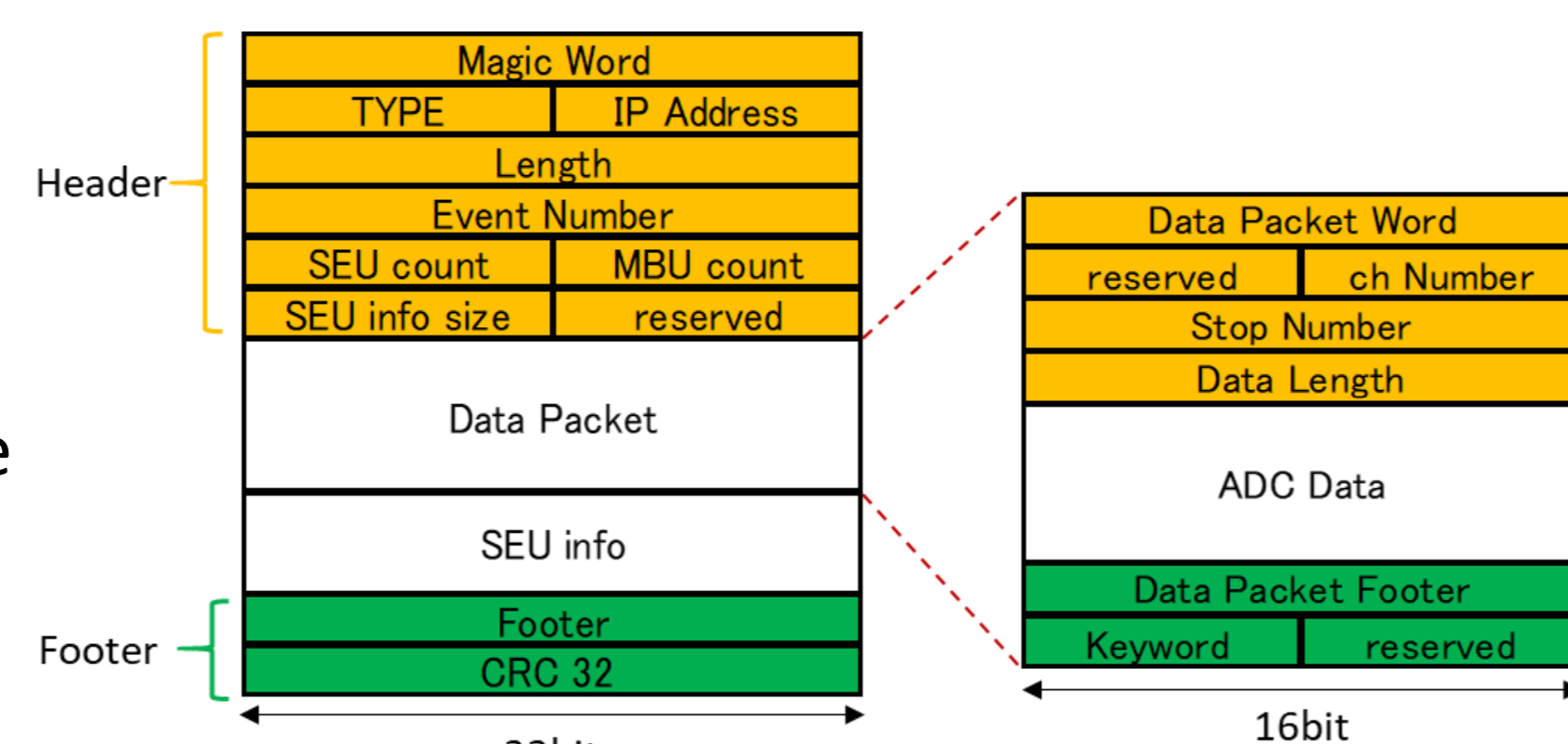
We have developed the readout electronics board called ROESTI (Read-Out Electronics for Straw Tube Instrument), which reads out the signal from the detector precisely.



ROESTI prototype version 3

In order to prevent the degradation of the detector signal, ROESTI needs to be installed in the gas manifold of the detector.

- The number of vacuum feedthroughs needs to be reduced due to space constraints and cost.
- Commercial network switches cannot be used due to space limitation and the radiation hardness.



Data structure for ROESTI

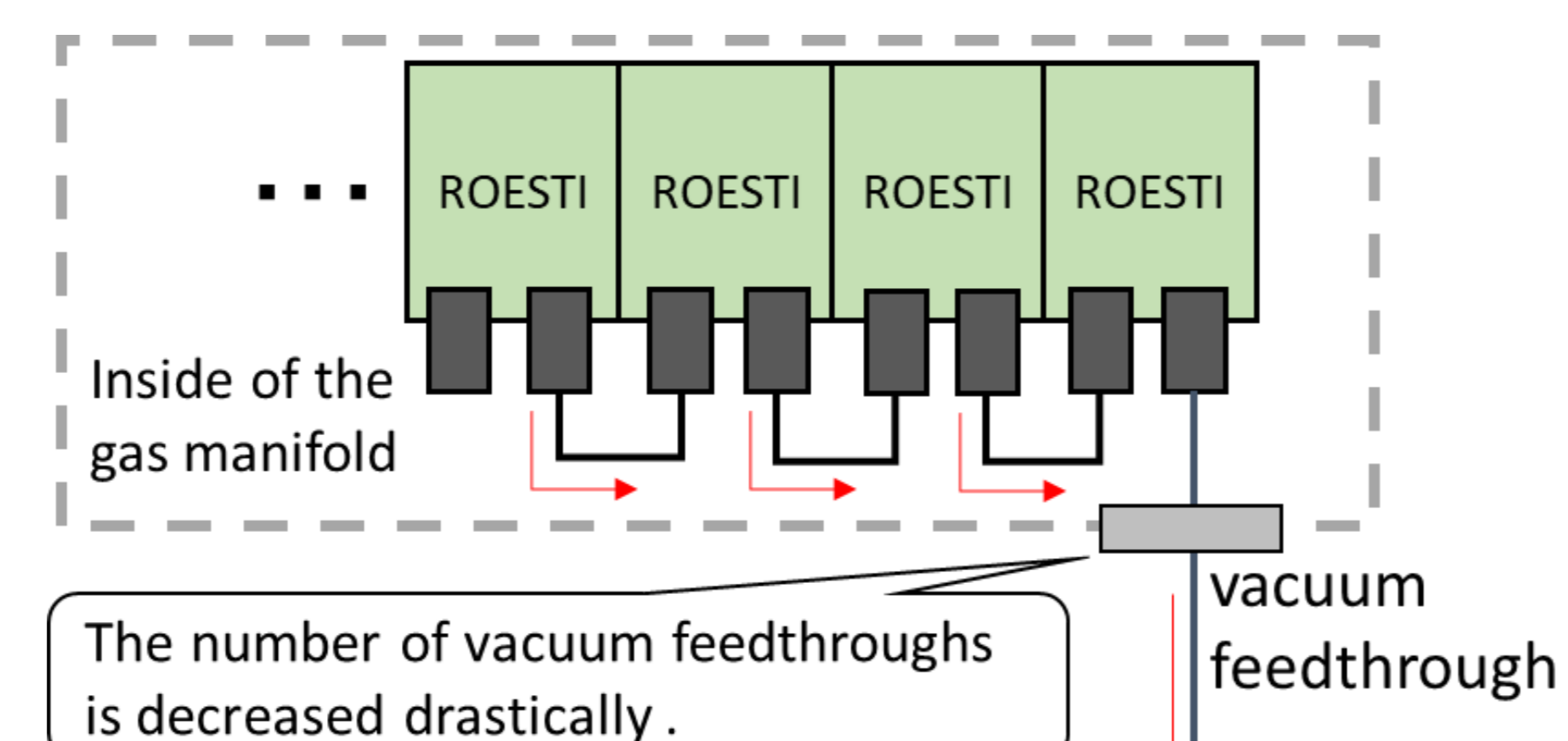
ROESTI needs to communicate with **daisy-chain**.

[Requirement functions of daisy-chain communication]

- Data transfer by TCP/Ethernet
- Slow Control for setting parameter

[Target performance of daisy-chain communication]

- Data transfer speed: close to the maximum rate of Gigabit Ethernet
- Data loss: reduce data loss as much as possible



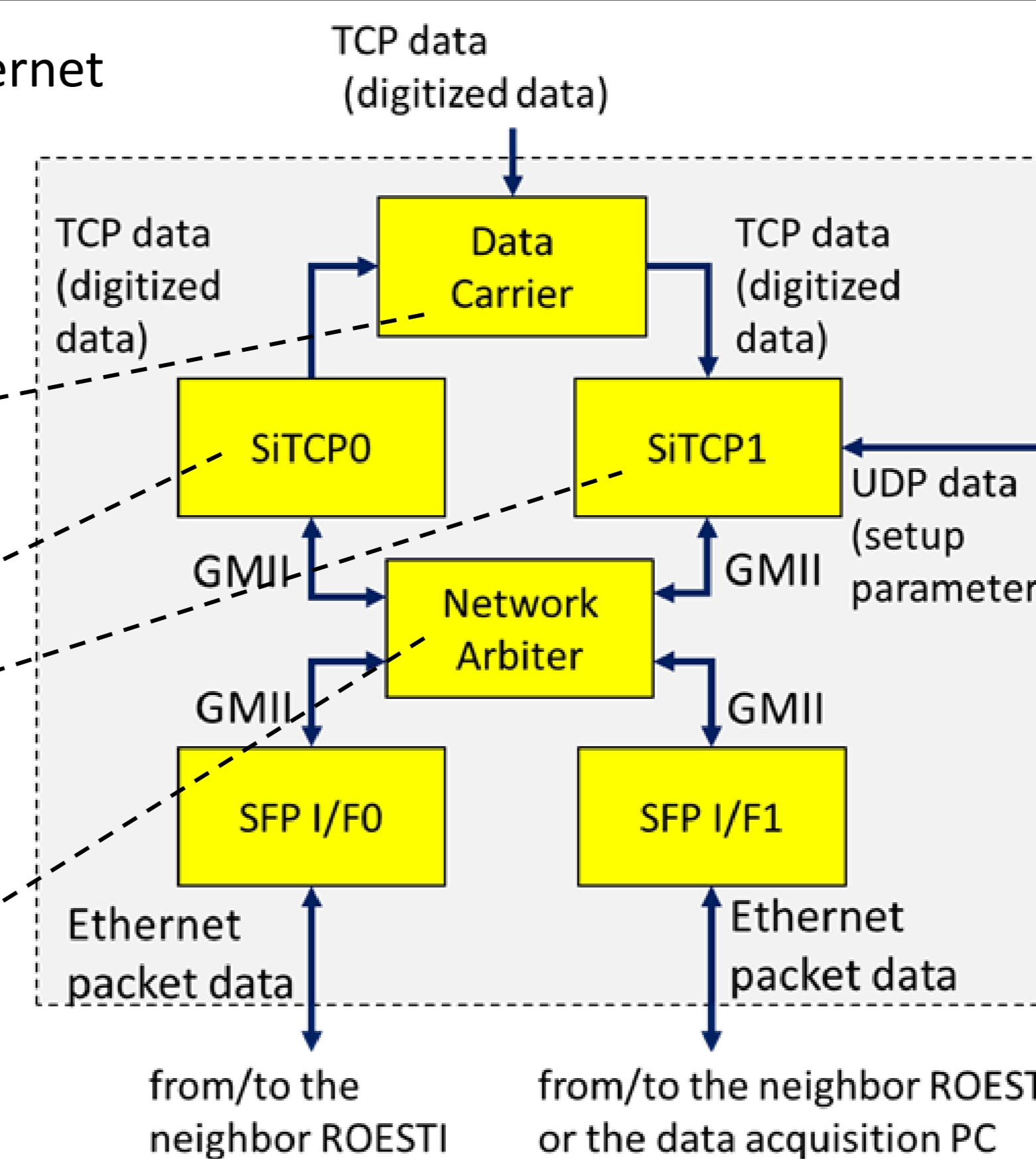
Daisy-chain communication

The number of vacuum feedthroughs is decreased drastically.

Daisy-Chain Implementation

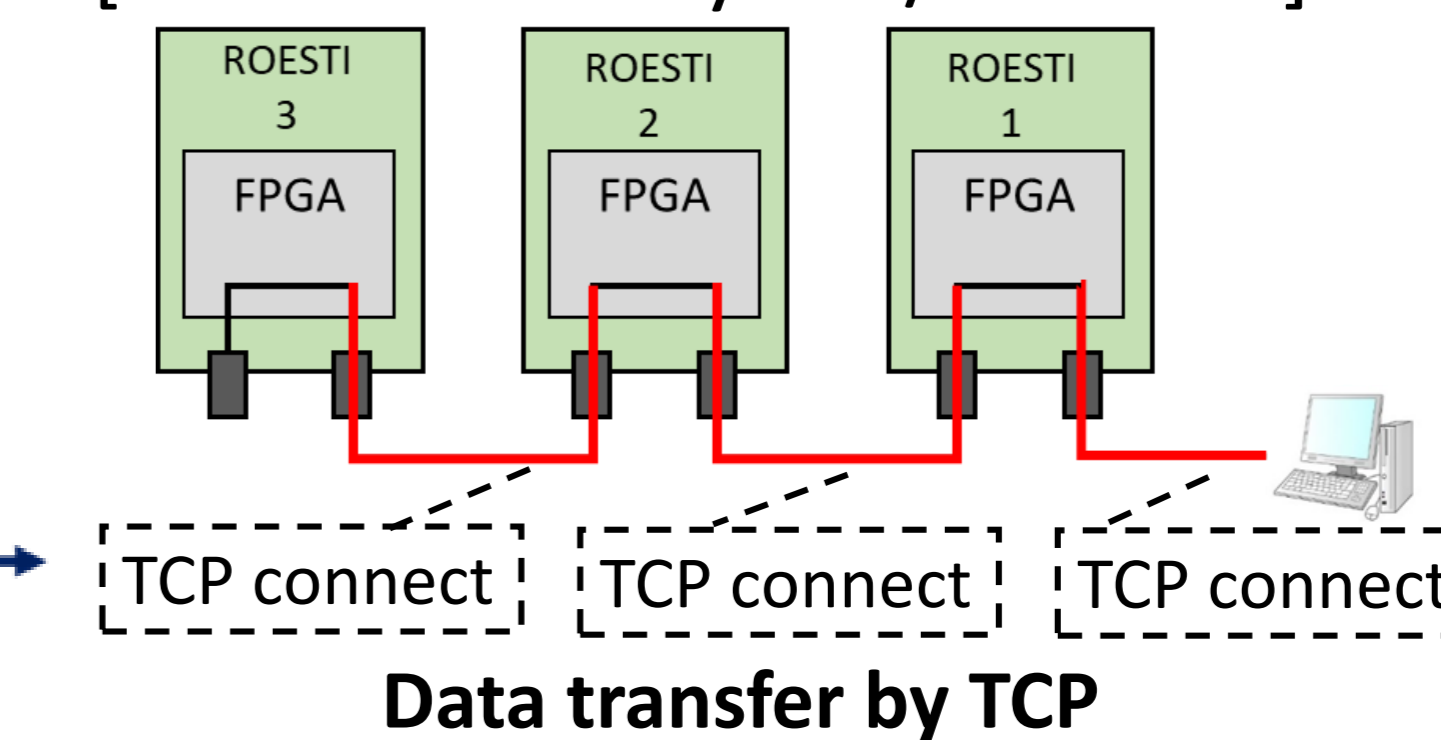
We implemented the Gigabit Ethernet daisy-chain function in the FPGA.

- by analyzing data, select transmission data (data of the own board or data of the previous board)
- a hard-ware based TCP processor for Gigabit Ethernet.
- slow control over UDP
- by analyzing MAC address, select the GMII data path.



Daisy-chain architecture in FPGA

[Data transfer by TCP/Ethernet]

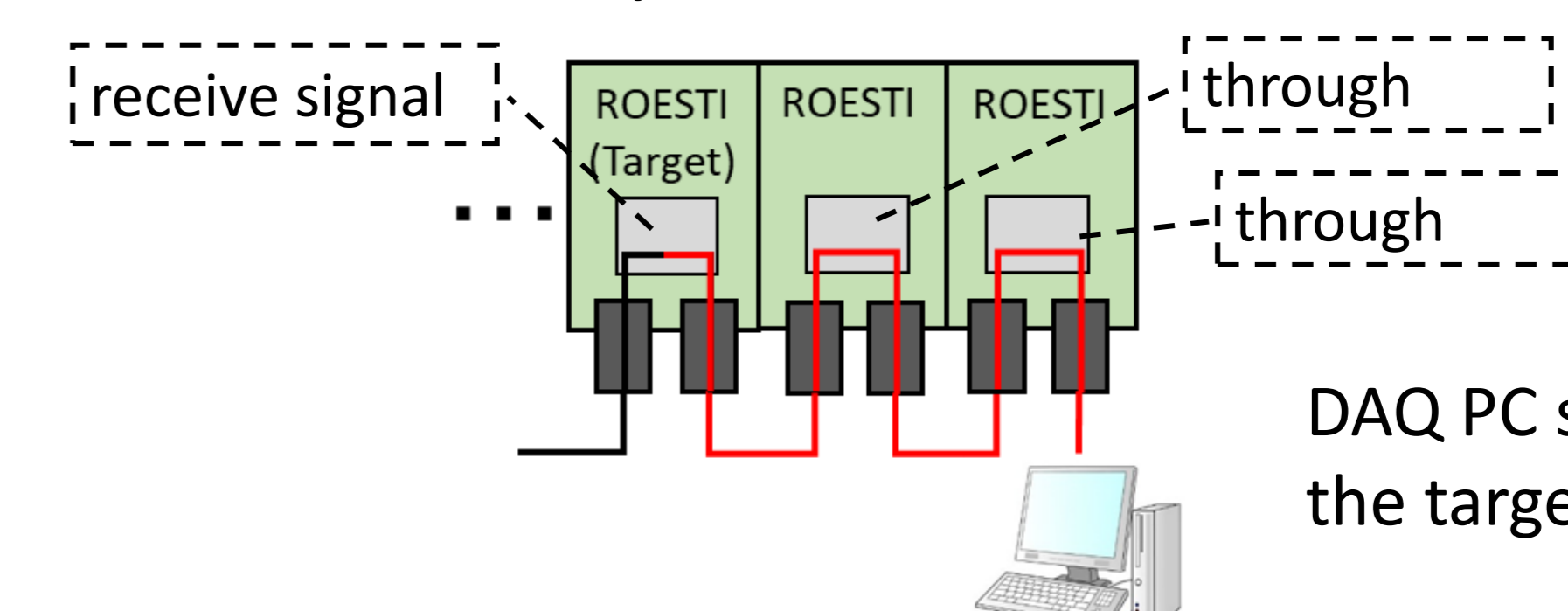


Data transfer by TCP

TCP connection between each ROESTIs or DAQ PC

- ROESTI prevents packet data collisions and TCP retransmission.
- achieve theoretical limit speed

[Slow Control by UDP/Ethernet]



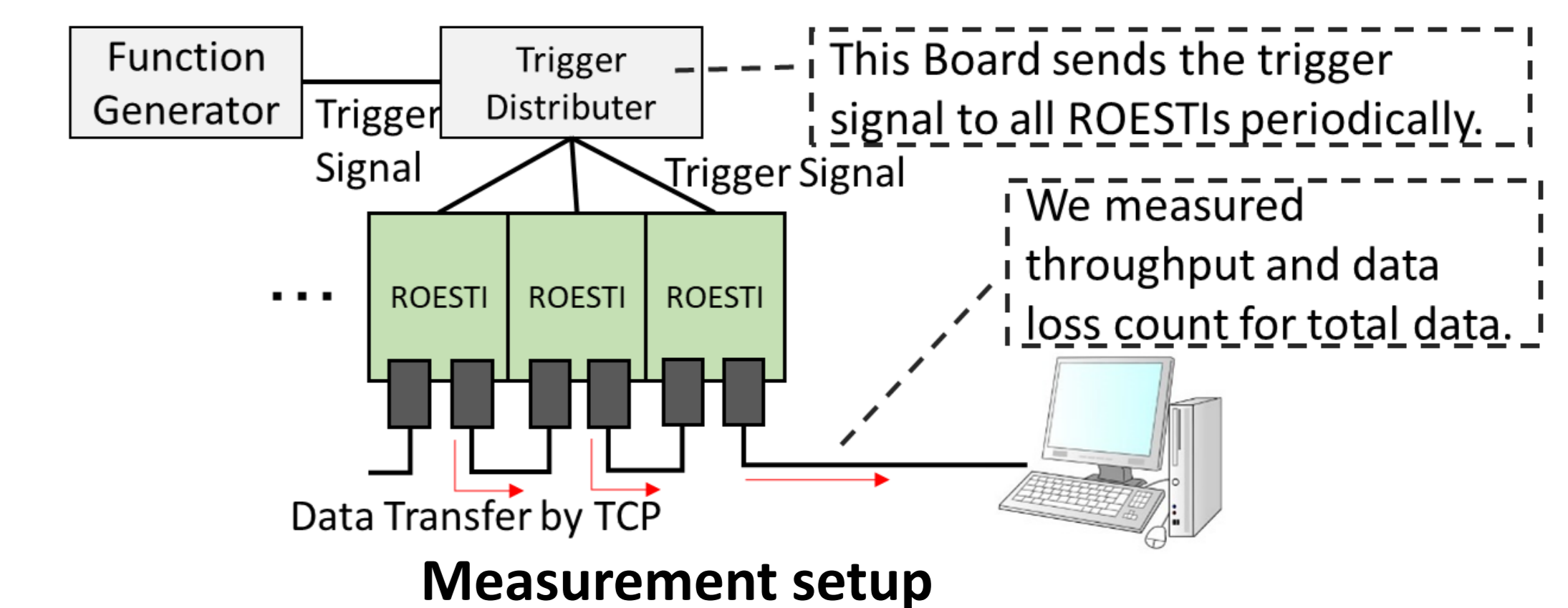
Slow control by UDP

DAQ PC sends slow control signal to the target ROESTI directly by UDP.

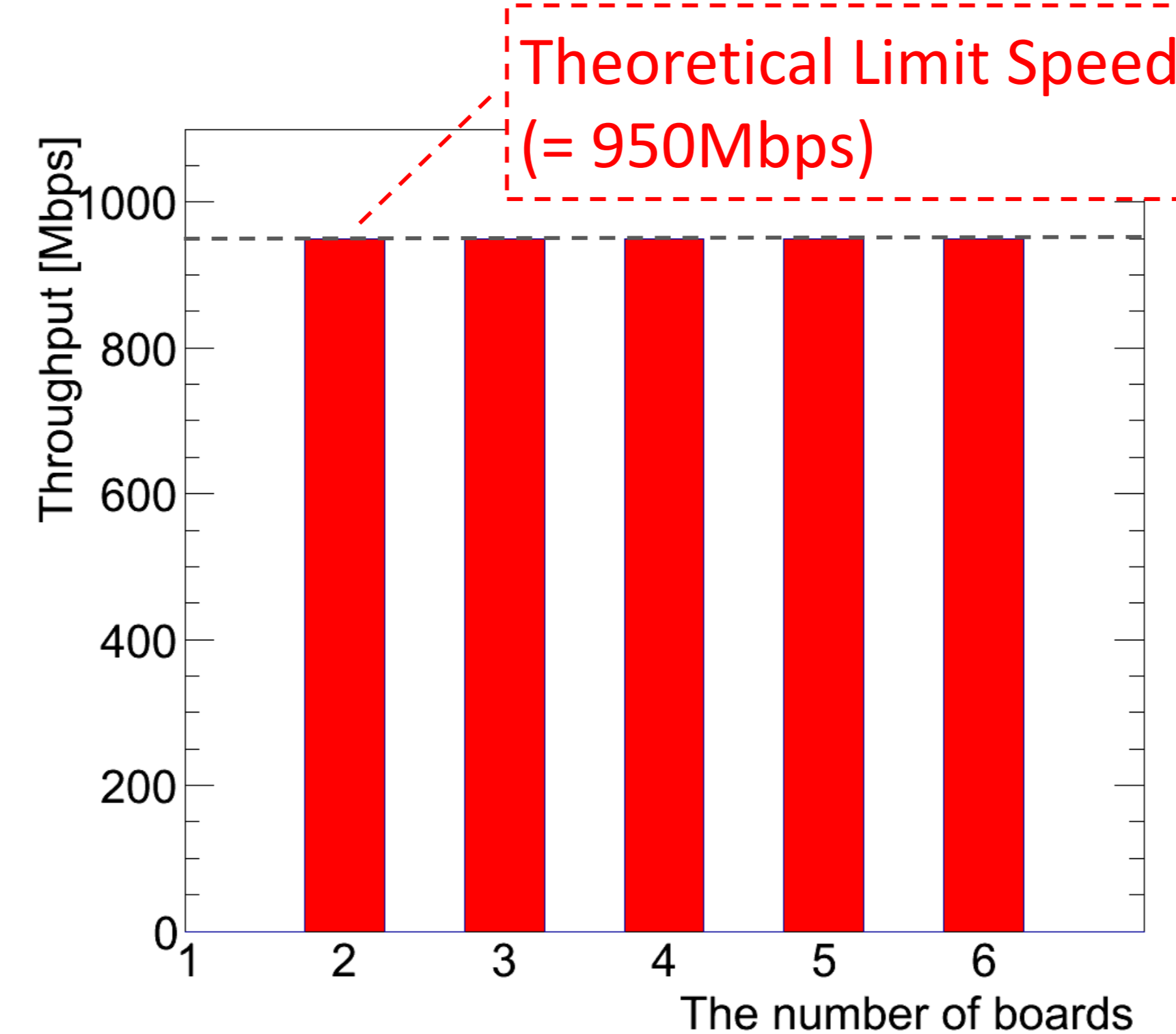
Measurement Result

Measurement of TCP data transfer function has been carried out with two to six ROESTIs. We obtained the following ideal results.

- In any number of boards, throughput of TCP data transfer was the theoretical limit speed, which was stable for a long time.
- In any number of boards, ROESTI could stably send 100% of the data for a long time when total data speed was less than theoretical limit speed.

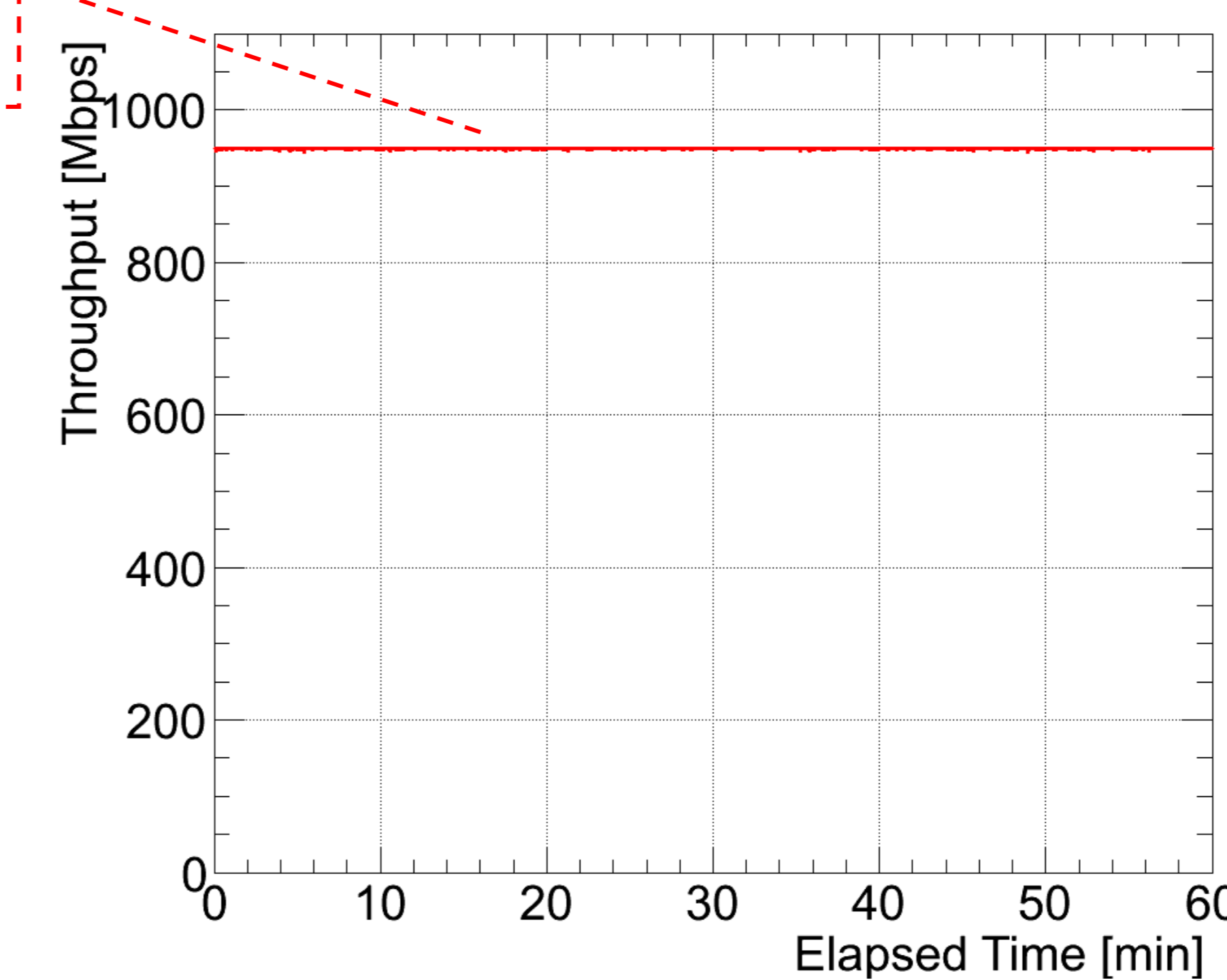


Measurement setup



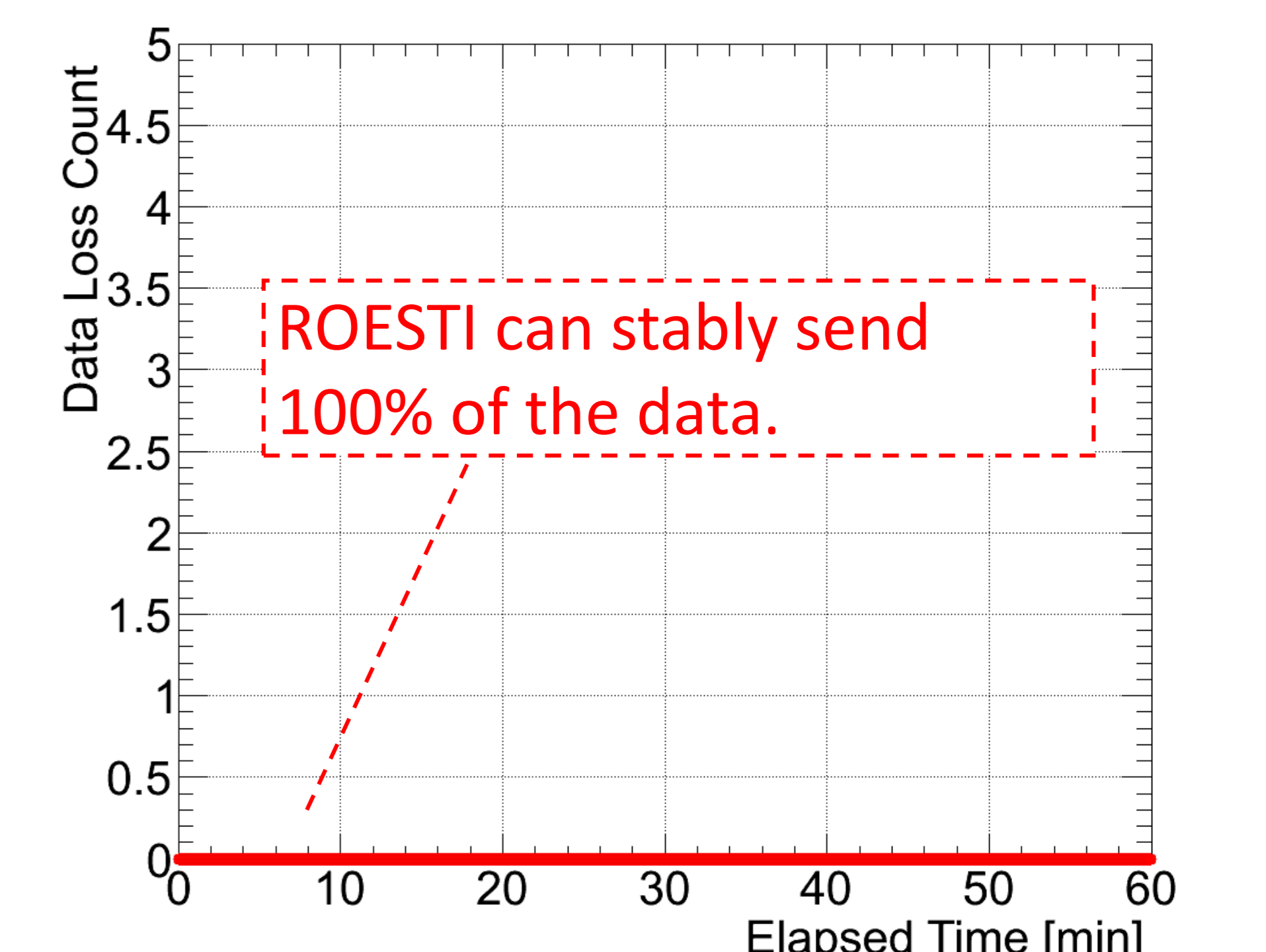
TCP throughput vs the number of boards

In any number of boards, throughput of TCP data transfer was theoretical limit speed.



Throughput vs elapsed time

In this measurement, we used six ROESTIs.



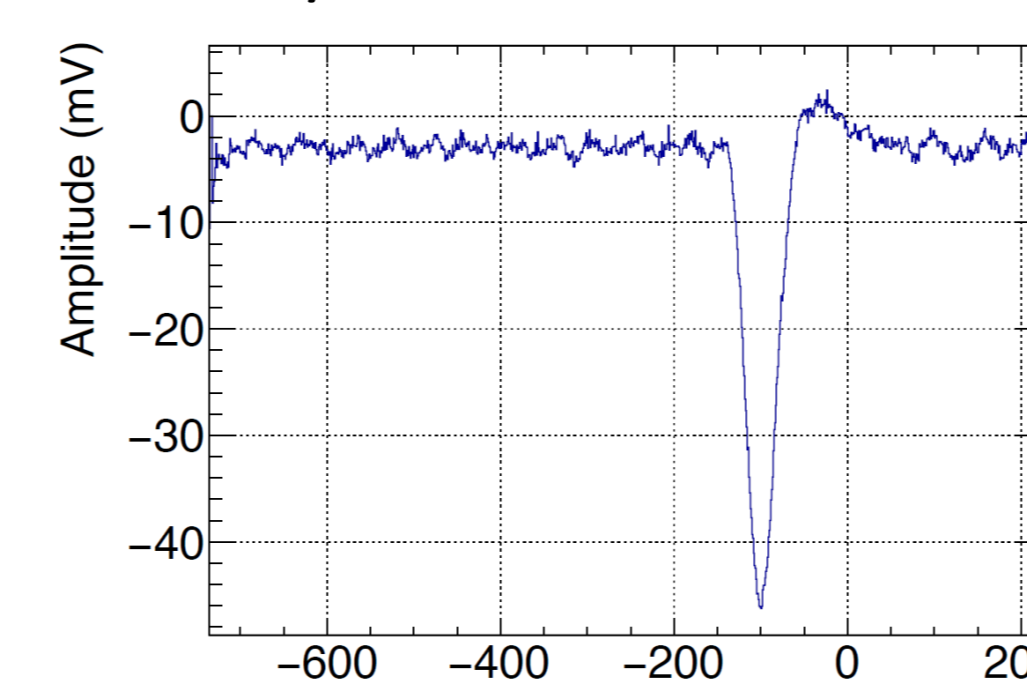
Data loss count vs elapsed time

In this measurement, we used six ROESTIs and total data transfer speed was set at 910 Mbps (almost theoretical limit speed).

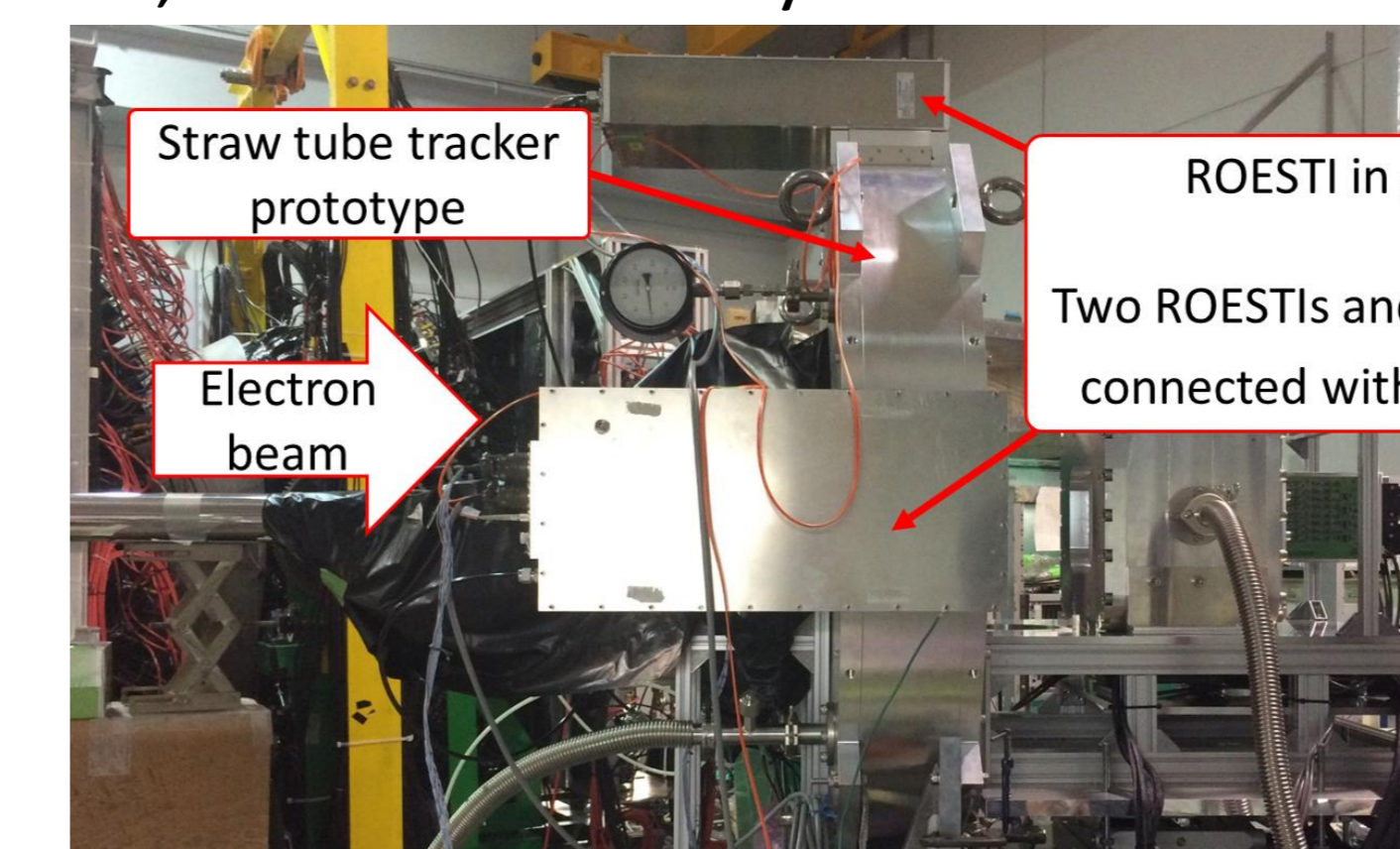
Beam TEST

Test-beam experiment was carried out at ELPH, Tohoku University.

- 100 MeV/c electron beam.



Waveform output



Picture of beam test

Conclusion

We have implemented the Gigabit Ethernet daisy-chain function in the FPGA of ROESTI.

We measured throughput, stability and data loss rate of the Gigabit Ethernet daisy-chain function. We obtained ideal results and found our Gigabit Ethernet daisy-chain function satisfied the target performance. We could also confirm that the daisy-chain function worked properly in the beam test at ELPH, Tohoku University. Therefore, we are going to adopt this function in the COMET experiment.