MicroTCA Technology Lab.

Jan Marjanovic for MicroTCA Tech Lab team
2020-10-14

22nd IEEE Real Time Conference
Vendor Product Presentation

MicroTCA TECHNOLOGY LAB
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES
DESY.

TRANSFER MTCA TO RESEARCH AND INDUSTRY

- Development: Hardware, FPGA, Software
- High-end test & measurement services
- System configuration & integration
  - LLRF turn-key-solution
  - Real-time image processing - (10) GigE Vision

MicroTCA Basic and Advanced training courses (focus on experimental physics):
https://techlab.desy.de/services/training/

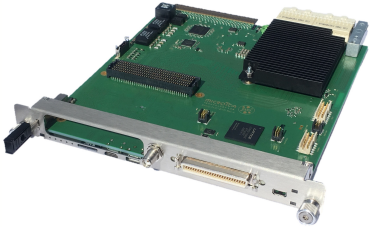
Outline

- Module Management Controller implementation
- High-performance FMC+ carrier (Zynq US+ MPSoC)
- Cost-optimized FMC carrier (Zynq 7000)

MMC Stamp

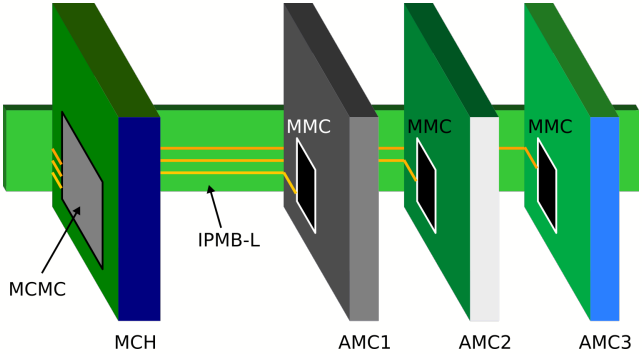
DAMC-FMC2ZUP

DAMC-FMC1Z7IO



Management in MicroTCA

One of most important features of MicroTCA is out-of-band management interface.

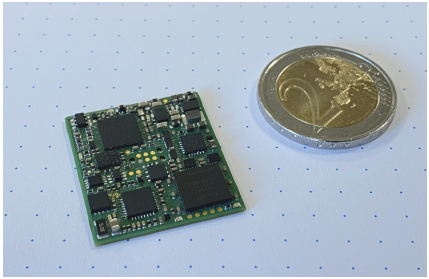


MicroTCA Carrier Management Controller (MCMC) (part of MicroTCA Carrier Hub - MCH) connects to Module Management Controller (MMC) on Advanced Mezzanine Card (AMC) over IPMB-L

for more information: http://www.rehlich.com/MicroTCA_IPMI_management

MMC Stamp

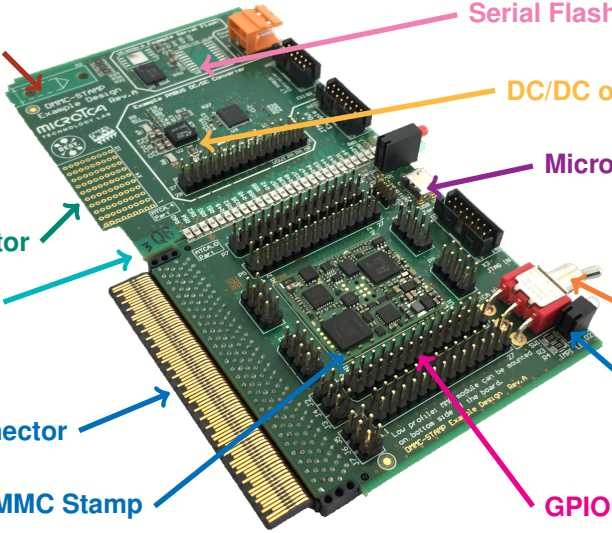
- Module Management Controller on a single board (SoM), ready-to-use, based on ARM Cortex-M4
- Full IPMI handling (LEDs, Power, PMBUS)
- FMC, RTM and FPGA control
- Tested with N.A.T. and Vadatech MCHs
- In future: Automated IPMI test suite
- HPM firmware update: MMC, FPGA flashes
- USB virtual COM port for MMC and FPGAs
- Solder-on component, firmware preprogrammed
- SDK available
- Firmware deployed to hundreds of boards at DESY and worldwide



https://techlab.desy.de/products/module_management_controller/mmc_stamp/

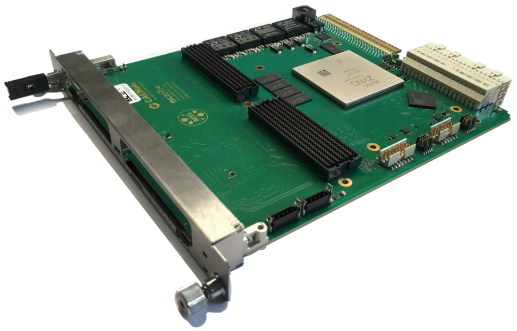
DMCS (University of Technology Lodz) also contributed to the development

MMC Stamp Starter Kit



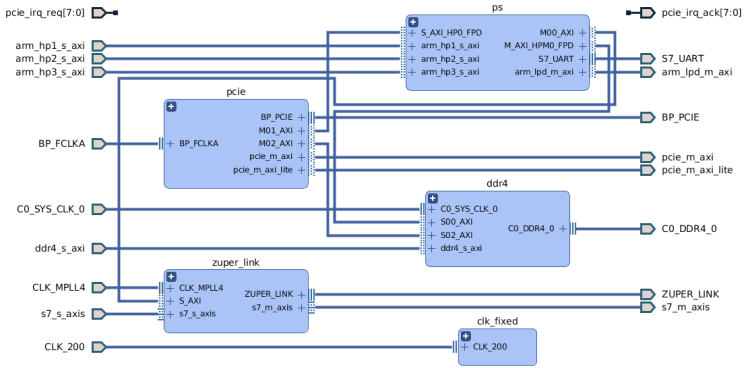
DAMC-FMC2ZUP

- Advanced Mezzanine Card (AMC.0), compatible with MicroTCA.4
- Xilinx Zynq UltraScale+ MPSoC
  XCZU11EG: 653k logic cells, 2928 DSP
- 52 transceivers (32 GTH, 16 GTY, 4 GTR)
- Quad-core ARM® Cortex-A53 and dual-core ARM® Cortex-R5
- 4GB DDR4 (PS) + 1GB DDR4 (PL)
- White Rabbit support
- PCIe Gen3 x4, x8 in supported systems, can be used as a PCIe root complex
- DisplayPort and USB to front panel
- Variant with XCZU19EG



https://techlab.desy.de/products/amc/damc_fmc2zup/

Board Support Package



Includes FPGA part (Vivado project) and Yocto Linux.
Contact us for more information/access: `mtca-techlab@desy.de`

PCI Express gen 3 x8

Most MicroTCA crates support PCIe x4, some also support x8

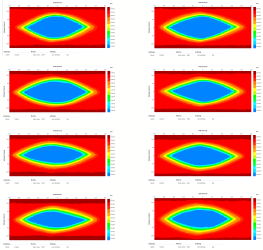
PCIe Link Status Menu

	AMC1	AMC2	AMC3	AMC4	AMC5		AMC6		OPT1
	4..11	4..11	4..11	4..11	4..7	8..11	4..7	8..11	
	-	-	x8	-	-	-	-	-	x8
Link Speed	-	-	8 GT/s	-	-	-	-	-	8 GT/s

DAMC-FMC2ZUP

optical uplink

Signal integrity in FPGA at 8 GT/s



DMA transfer (1 GB) with Xilinx DMA (xdma)

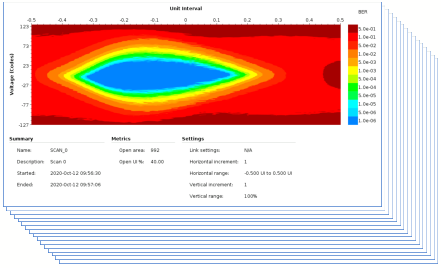
Width	Data rate	CPU	Mem	Access	Throughput
x4	8 GT/s	CCT AM G64/472	PL	Read	**2028** MB/s
x4	8 GT/s	CCT AM G64/472	PL	Write	**2948** MB/s
x4	8 GT/s	CCT AM G64/472	PS	Read	**2001** MB/s
x4	8 GT/s	CCT AM G64/472	PS	Write	**3006** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PL	Read	**1762** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PL	Write	**3304** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PS	Read	**1687** MB/s
x8	8 GT/s	Fujitsu PRIMERGY TX2550	PS	Write	**3415** MB/s

Preliminary measurements, will be improved in the future

FMC and FMC+ (400 Gbps)

- FMC+ slot
  - full LA and HA banks
  - DP[0:15] to GTY
  - DP[16:23] to GTH
- FMC slot
  - full LA and HA banks
  - DP[0:7] to GTH

16 lanes (GTYE4), 25 Gbps, PRBS31



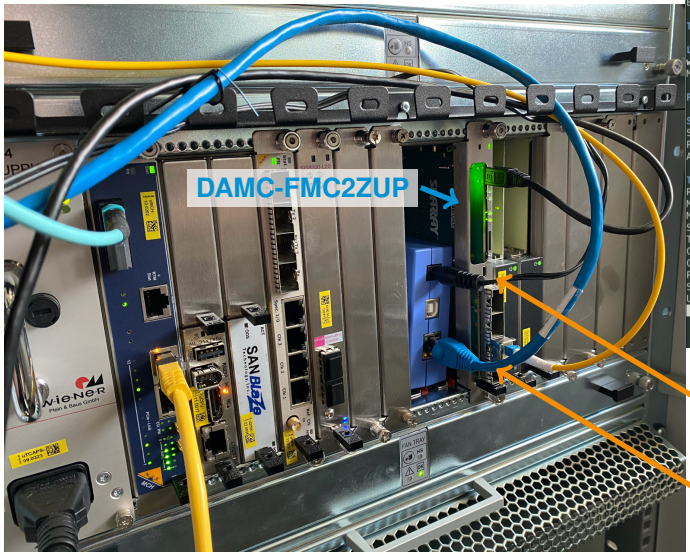
Test with an FMC+ loopback card

25 Gbps

Link Group 0 (16)							Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 0	Quad_128/MGT_X0Y4/TX (xczu11_0)	Quad_128/MGT_X0Y4/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 1	Quad_128/MGT_X0Y5/TX (xczu11_0)	Quad_128/MGT_X0Y5/RX (xczu11_0)	25.372 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 2	Quad_128/MGT_X0Y6/TX (xczu11_0)	Quad_128/MGT_X0Y6/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 3	Quad_128/MGT_X0Y7/TX (xczu11_0)	Quad_128/MGT_X0Y7/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 4	Quad_129/MGT_X0Y8/TX (xczu11_0)	Quad_129/MGT_X0Y8/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 5	Quad_129/MGT_X0Y9/TX (xczu11_0)	Quad_129/MGT_X0Y9/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 6	Quad_129/MGT_X0Y10/TX (xczu11_0)	Quad_129/MGT_X0Y10/RX (xczu11_0)	25.324 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 7	Quad_129/MGT_X0Y11/TX (xczu11_0)	Quad_129/MGT_X0Y11/RX (xczu11_0)	25.327 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 8	Quad_130/MGT_X0Y12/TX (xczu11_0)	Quad_130/MGT_X0Y12/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 9	Quad_130/MGT_X0Y13/TX (xczu11_0)	Quad_130/MGT_X0Y13/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 10	Quad_130/MGT_X0Y14/TX (xczu11_0)	Quad_130/MGT_X0Y14/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 11	Quad_130/MGT_X0Y15/TX (xczu11_0)	Quad_130/MGT_X0Y15/RX (xczu11_0)	25.319 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 12	Quad_131/MGT_X0Y16/TX (xczu11_0)	Quad_131/MGT_X0Y16/RX (xczu11_0)	25.313 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 13	Quad_131/MGT_X0Y17/TX (xczu11_0)	Quad_131/MGT_X0Y17/RX (xczu11_0)	25.312 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 14	Quad_131/MGT_X0Y18/TX (xczu11_0)	Quad_131/MGT_X0Y18/RX (xczu11_0)	25.315 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)
Link 15	Quad_131/MGT_X0Y19/TX (xczu11_0)	Quad_131/MGT_X0Y19/RX (xczu11_0)	25.340 Gbps	1.286E14	0E0	7.779E-15	Reset	PRBS 31-bit	PRBS 31-bit	3.08 dB (01100)	0.00 dB (00000)	950 mV (11000)

Bit Error Rate lower than 1E-14

White Rabbit



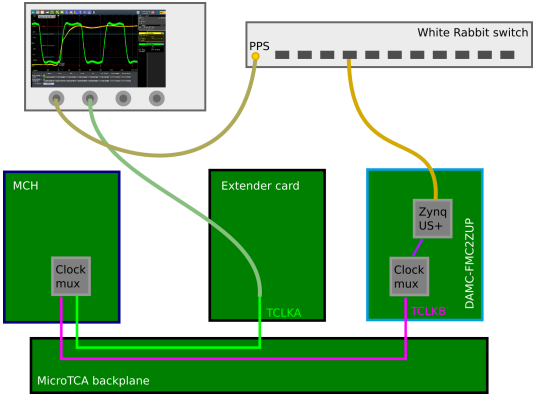

```
WR PTP Core Sync Monitor wrpc-v4.2
Esc = exit

TAI Time:                    Thu, May 18, 2017, 12:07:16

Link status:
wru1: Link up    (RX: 539, TX: 329) IPv4: 192.168.20.10 (static assignment)
Mode: WR Slave    Locked Calibrated

PTP status: slave

Synchronization status:
Servo state:                 TRACK_PHASE
Phase tracking:              ON
Aux clock 0 status:          enabled

Timing parameters:
Round-trip time (mu):                743439 ps
Master-slave delay:                  370167 ps
Master PHY delays:           TX:     224037 ps, RX:     235977 ps
Slave PHY delays:            TX:          0 ps, RX:       8800 ps
Total link asymmetry:                -3105 ps
Cable rtt delay:                    274625 ps
Clock offset:                           -3 ps
Phase setpoint:                      15667 ps
Skew:                                    2 ps
Update counter:                        105
```

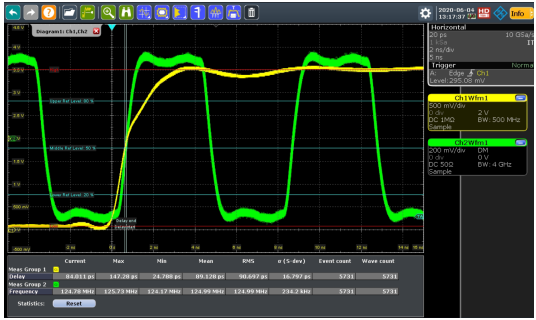
one GTH connected to the Front Panel
(special cable needed)

or **connection over FMC-4SFP+**

White Rabbit

With flexible clocking architecture, both on the card itself and in crate, we can distribute clock and triggers to other cards.



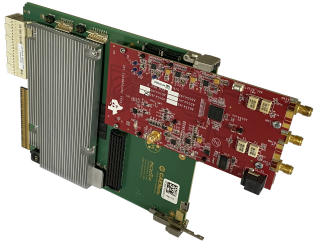


jitter = 16.8 ps, meas time = 1.5 h

Applications

ADS54J60EVM

- 1 GSPS, 16-bit ADC
- 2 channels
- JESD204B (at 10 Gbps)
- subclass 1 for sync



DFMC-DSx00

- 500/800 MSPS, 12-bit ADC
- 2 channels
- LVDS interface
- very low latency

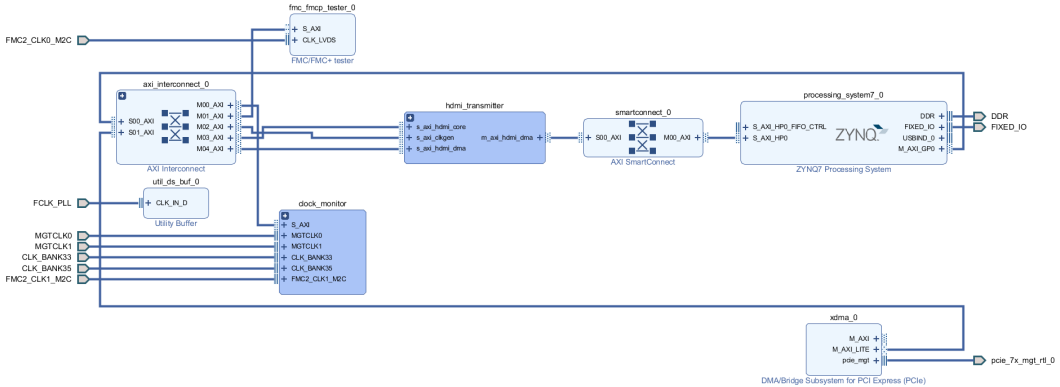
Latency comparison of ADCs with different interfaces,
https://indico.desy.de/indico/event/25669/session/2/contribution/52

DAMC-FMC1Z7IO

- Advanced Mezzanine Card, compatible with MicroTCA.4
- Xilinx Zynq-7000 SoC (XC7Z030, XC7Z035 and XC7Z045)
- 48 bidirectional IOs: 3.3V and true 5V
- FMC slot (full LA bank, 2/4 MGTs)
- PCIe x2 Gen2 (x4 optional)
- Dual core ARM processor
- HDMI and USB to front panel
- Zone 3 Class D1.1

https://techlab.desy.de/products/amc/damc_fmc1z7io/

Board Support Package



In development, contact us for early access: `mtca-techlab@desy.de`

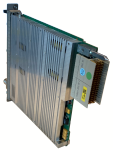
Applications

DRTM-AD84 - Rear Transition Module

- 8 channel 10 MSPS, 16 bit ADC
- 4 channel 1 MSPS, 16 bit DAC

DRTM-PZT4 - Rear Transition Module

- 4 channel piezo driver



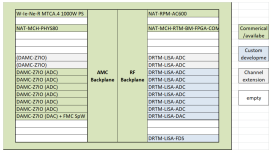
LISA phasemeter EGSE

- LISA = Laser Interferometer Space Antenna
- ground support for phasemeter (40 ch readout)
- Collaboration with University of Hamburg

Gefördert durch:
Bundesministerium für Wirtschaft und Energie
aufgrund eines Beschlusses des Deutschen Bundestages

Based on MicroTCA.4.1

RF backplane is used to distribute pilot tone and ADC clocks



Thank you

Come visit our booth (live demos):
https://us02web.zoom.us/j/99778824656
?pwd=cVVuUU5mdmorS3FzbHIvWUdON1Zpdz09

https://techlab.desy.de
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