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System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC

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For the High-Luminosity LHC era, the trigger and data acquisition system of the Compact Muon Solenoid experiment will be entirely replaced. Novel design choices have been explored, including ATCA prototyping platforms with SoC controllers and newly available interconnect technologies with serial optical links with data rates up to 28 Gb/s. Trigger data analysis will be performed through sophisticated algorithms, including widespread use of Machine Learning, in large FPGAs, such as the Xilinx UltraScale family. The system will process over 50 Tb/s of detector data with an event rate of 750 kHz. The system design and prototyping will be described and examples of trigger algorithms reviewed.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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