Radiation tolerance of online trigger system for COMET Phase-I

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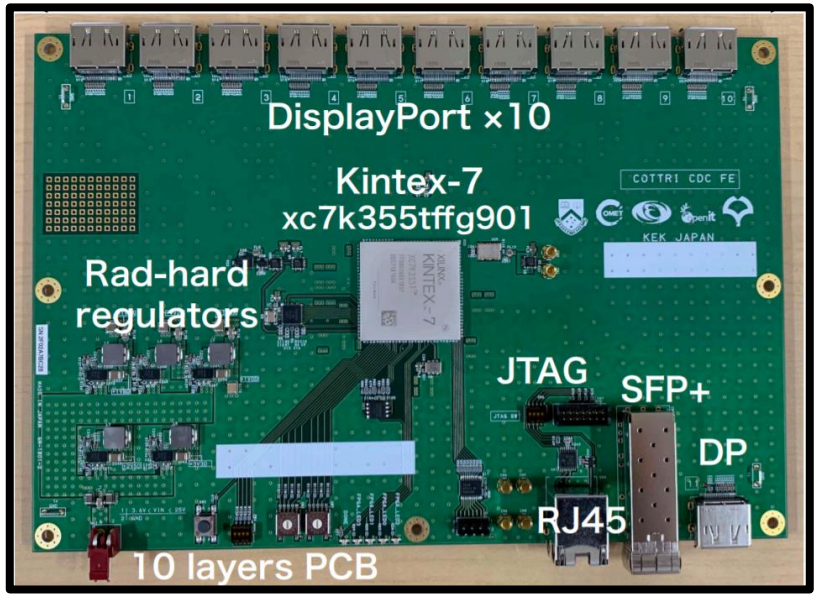
Summary

Purpose

The COMET experiment is searching for neutrinoless muon to electron conversion (a signal for new physics) at new sensitivity levels. This requires an online trigger system tolerant to high radiation levels to reach sensitivity levels.
→ **Aim:** Evaluate trigger board performance in high radiation environment.



Measurements

- Soft error rates measured in configuration memory, block memory and multi-gigabit data link of front-end trigger board, subject to neutron fluence level $(1.0 \pm 0.3) \times 10^{12}\ n \cdot cm^{-2}$
- Multi-gigabit link performance important for the trigger system operation and had not been measured for COMET Phase-I yet.

Conclusions

- Configuration memory soft errors show greatest impact compared to other areas.
- A conservative estimate of dead time due to firmware resets (necessary due to soft errors not fixable through code) is estimated to be (3.7 ± 1.2) % for the entire COTTRI front-end system.
- Block memory multi-bit errors not insignificant, however multiple solutions can be used to suppress these rates. Expected effect on trigger data is 24 ± 8 multi-bit errors during Phase-I.

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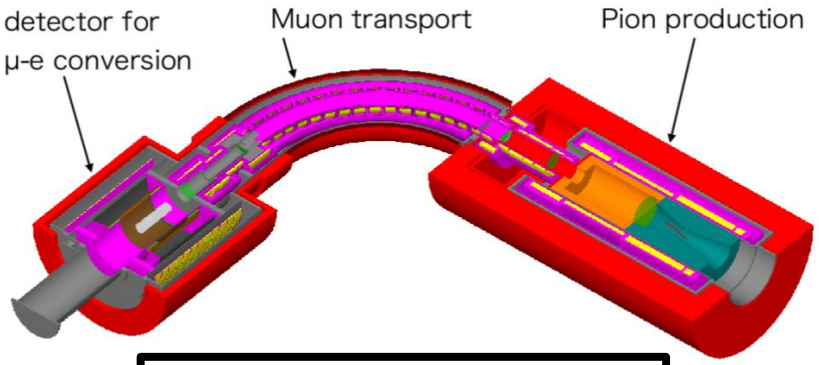
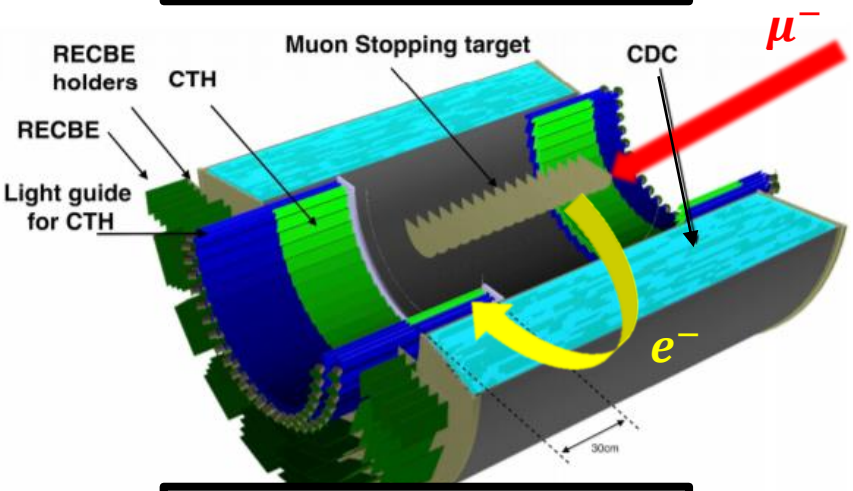
COMET

(**CO**herent **M**uon to **E**lectron **T**ransition)



COMET Phase-I Layout



CyDet Cross-section

[1] Images from G.Adamov, *et.al*, "COMET Phase-I Technical Design Report", 2020(3)

Searching for charged lepton flavour violation process:

$$\mu^- N \rightarrow e^- N$$

Observation signals **new physics**: COMET will measure at new sensitivity levels ($\approx 3 \times 10^{-15}$ in Phase-I)

Overview of Phase-I

- Phase-I data collected over **150 days**
- Pions produced using high intensity 8 GeV pulsed proton beam at J-PARC facilities in Tokai, Japan.
- Muons produced in transport solenoid through pion decay → will be world's highest intensity muon beam.
- Muon beam directed into Al stopping targets at centre of CyDet (**CYL**indrical **DET**ector) for capture.
- **High radiation levels** inside detector solenoid

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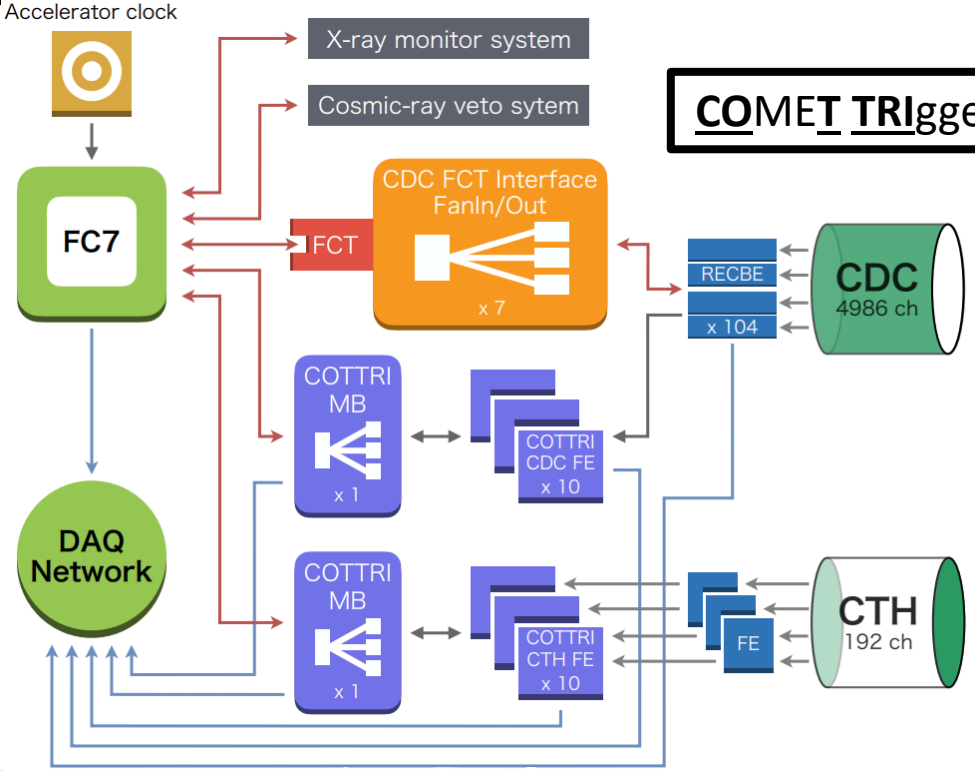
COTTRI



Overview of COMET Phase-I online trigger system

*For more details see Y.Nakazawa et.al *"An FPGA-based Trigger System with Online Track Recognition in COMET Phase-I"* also present at this conference.

[1] Images from G.Adamov, *et.al*, "COMET Phase-I Technical Design Report", 2020(3)

Overview of COTTRI Trigger System

- Located inside detector solenoid
  - 1 T magnetic field strength
  - Up to 10^{12} n · cm^{-2} neutron fluence during data collection (includes safety factor of 5)
    → **Purpose of this study**
  - Up to 1 kGy gamma radiation during data collection (includes safety factor of 5)
- Requirements*:
  - 13 kHz trigger rate
  - 7 μs latency
    - Measured: 3.1 – 3.2 μs
- Trigger window 1 μs
- 2-bit ADC used in hit classification for CDC
- 480 RECBE Channels per CDC COTTRI Front-End (**FE**) board
- 4-fold coincidence trigger in CTH achieved through amplification/discrimination electronics

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COTTRI

- Use of commercial FPGA chips
- FE boards implemented with radiation tolerant regulators
- Multi-gigabit data transfer **important** → facilitates communication:
  - RECBE to COTTRI FE
  - COTTRI FE to COTTRI Merger-board
- Communication:
  - Multi-gigabit data links – Aurora 8B/10 B protocol [2]
  - Firmware download – RJ45
  - DAQ – SFP+

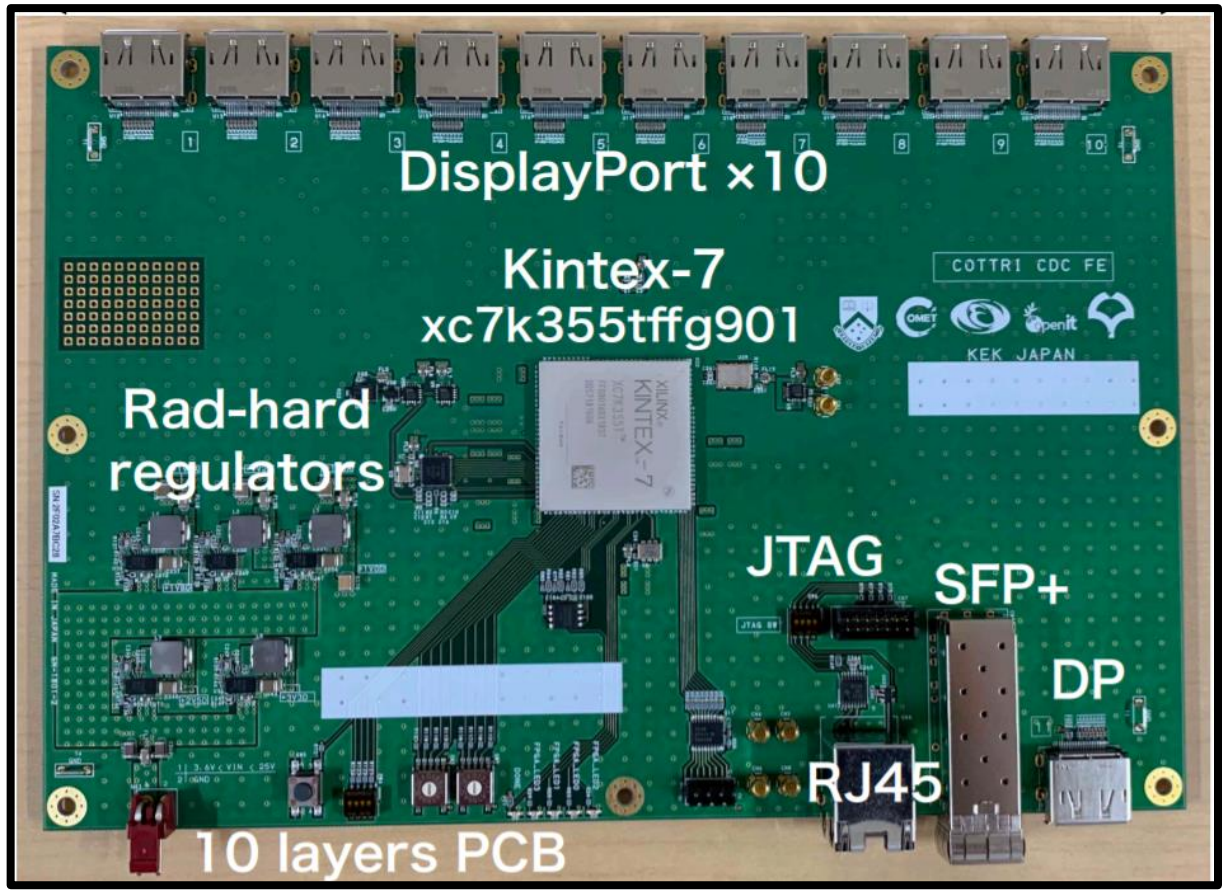

Image of one CDC COTTRI Front-End (**FE**) Board

[2] Xilinx Inc., Aurora 8B/10B, https://www.xilinx.com/products/intellectual-property/aurora8b10b.html

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Radiation Errors

- Variety of soft errors through neutron interactions with the silicon material.
- Charge carriers can alter susceptible transistor states by generating electron-hole pairs.

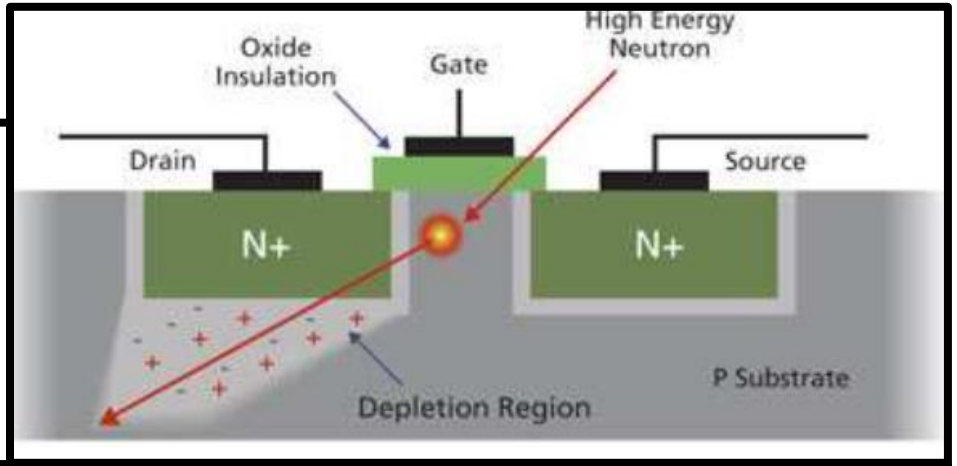

Diagram of neutron radiation causing soft error in transistor gate (image from [3]).

Types of error

- Single Event Upset (**SEU**)
  - Any bit errors caused by the neutron radiation
  - Generally rectified by using error-correction code (**ECC**).
- Multi-Bit Error (**MBE**)
  - More than one bit error occurring within a given address register.
- Unrecoverable Error (**URE**)
  - Any register error or communication error requiring full firmware redownload to rectify.

[3] M.Mason, 2006, "Cosmic rays damage automotive electronics", EE Times, https://www.eetimes.com/cosmic-rays-damage-automotive-electronics/, Accessed: 13/10/20

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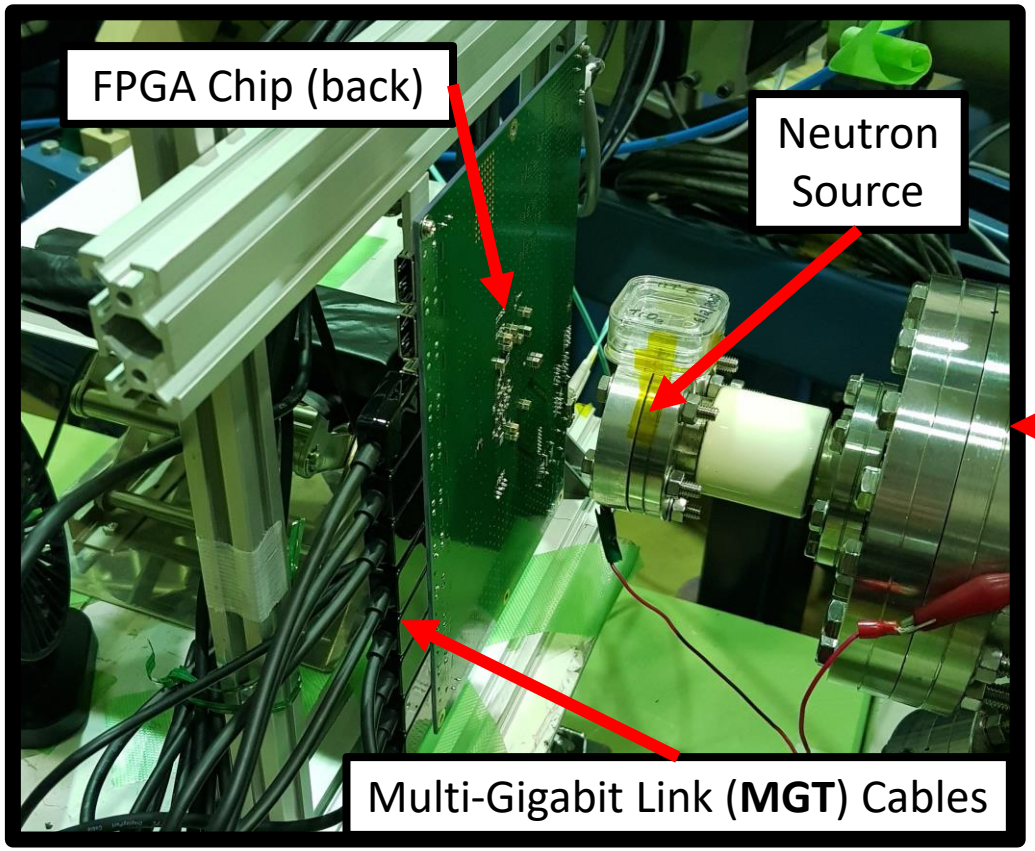
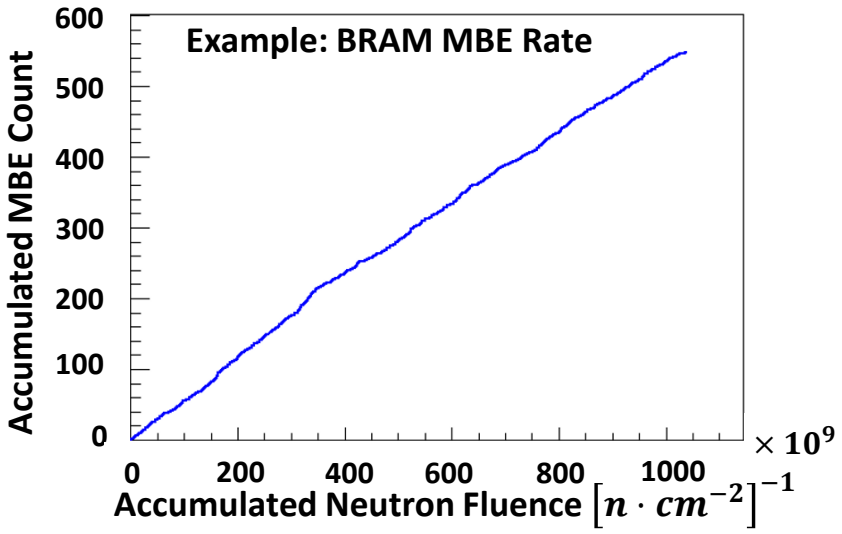
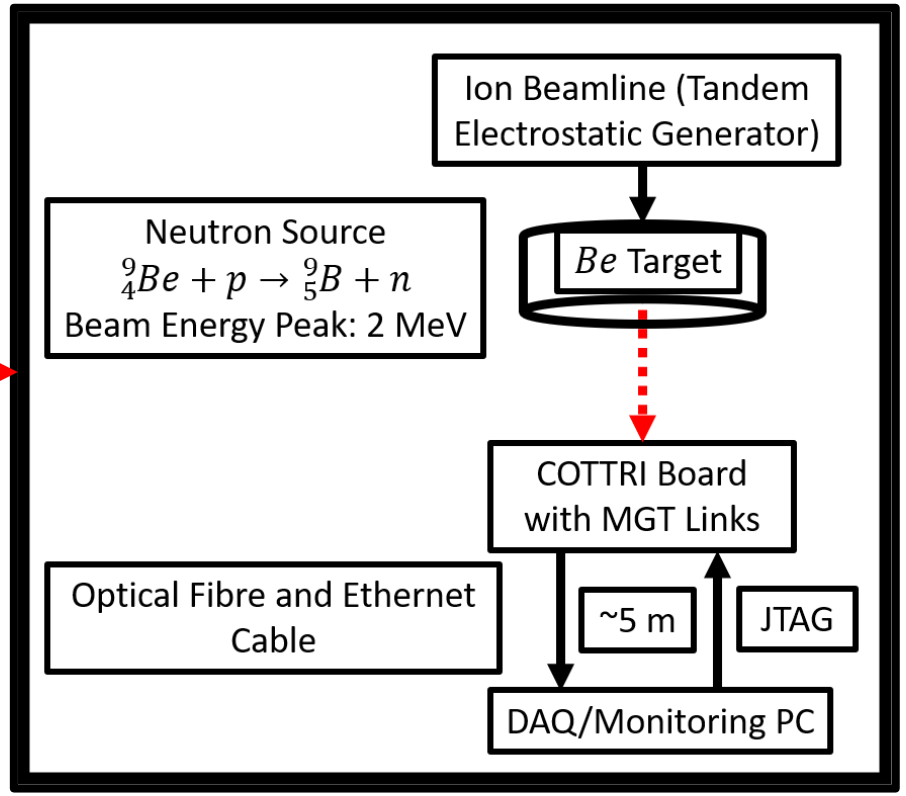
Measurement Setup

Irradiated COTTRI FE Board at the Accelerator and Particle Beam Experiment Facility at Kobe University

Total Neutron Fluence (1 MeV Equivalent)
$(1.0 \pm 0.3) \times 10^{12}\ \mathrm{n} \cdot \mathrm{cm}^{-2}$







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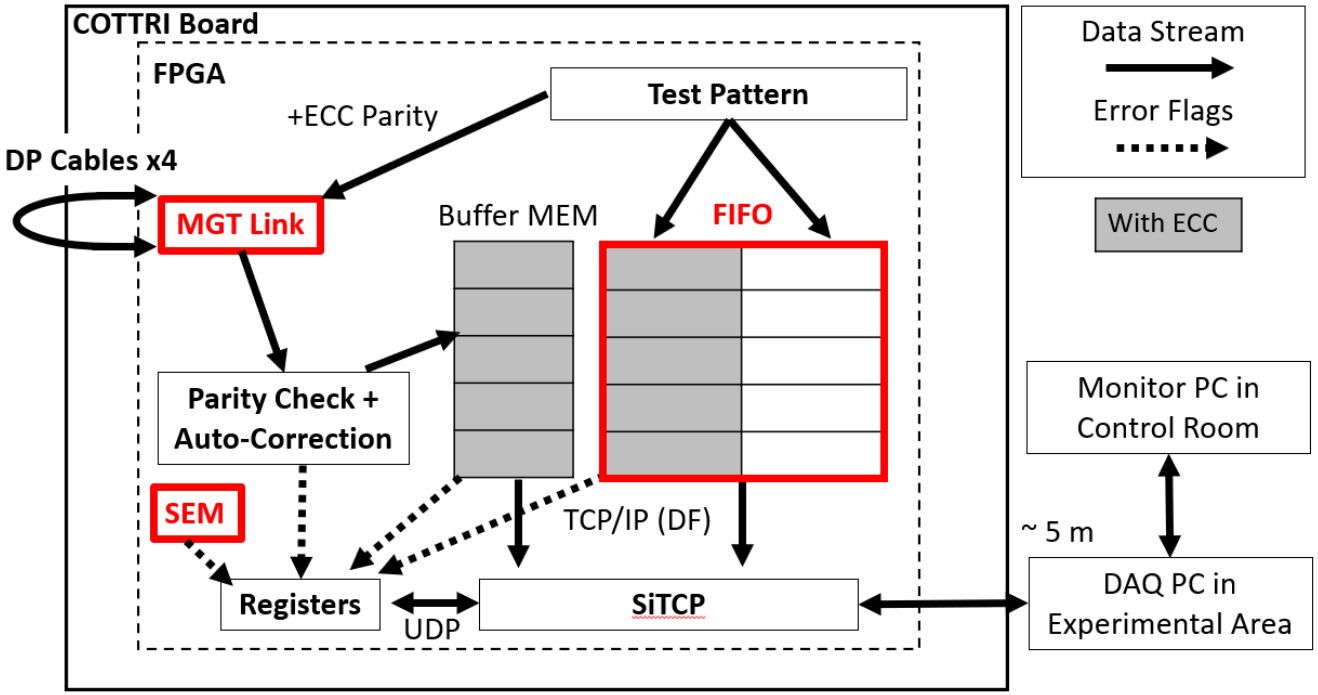
Measurement Firmware



FPGA used: **Xilinx Kintex-7** (XC7K355T) [4]

[2] Xilinx Inc., Aurora 8B/10B, https://www.xilinx.com/products/intellectual-property/aurora8b10b.html
[4] Xilinx Inc., Kintex-7, https://www.xilinx.com/products/silicon-devices/fpga/kintex-7.html
[5] Xilinx Inc., Soft Error Mitigation (SEM) Core, https://www.xilinx.com/products/intellectual-property/sem.html
[6] T. Uchida, "Hardware-Based TCP Processor for GigabitEthernet", IEEE Transactions on Nuclear Science 55.3(2008), pp. 1631–1637

Three Key Areas

- **Configuration memory (CRAM)**
  - Utilising Xilinx Soft Error Mitigation (**SEM**) module [5]
  - CRAM URE detection critical as full DAQ redownload required.
- **Block memory (BRAM)**
  - Utilising FIFO Error Correcting Code (**ECC**)
  - ECC applied to half of BRAM to check performance
- **Multi-gigabit link (MGT)**
  - Transmission uses Aurora 8B/10B protocol [2]
  - Parity code for auto-correcting bit flips
- Data also sent offline to DAQ PC via SiTCP connection [6]

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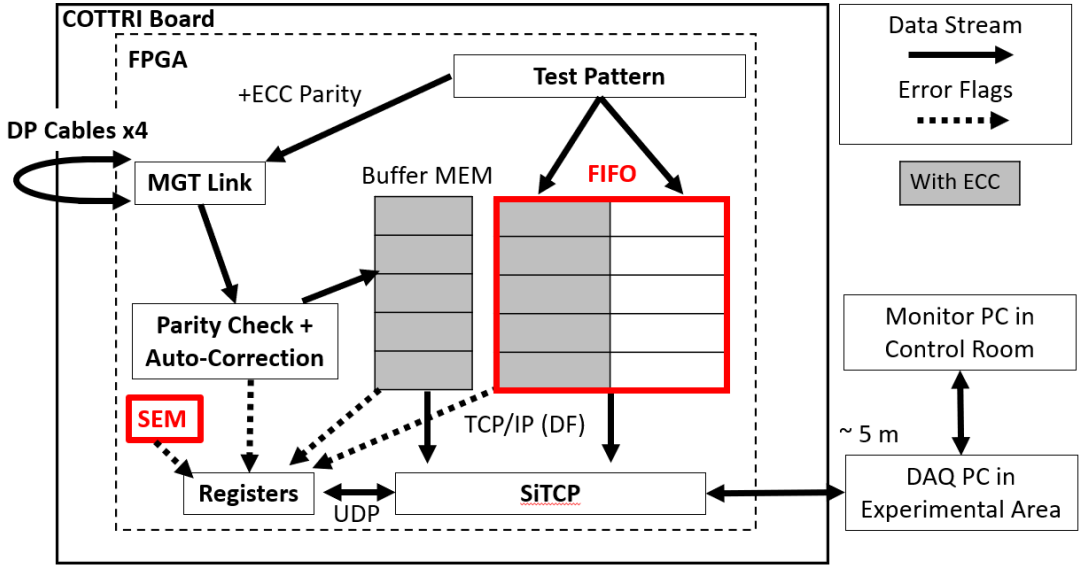
CRAM and BRAM

- **CRAM (SEM)**
  - SEM gives flag upon SEU/URE
  - Connection loss also counted as URE by monitoring connection between DAQ PC and COTTRI board
  - Counter for SEU/URE showing erratic behaviour also treated as URE.
- **BRAM (FIFO ECC)**
  - Utilises Hamming code to check parity – one bit error can be corrected otherwise MBE recorded.
  - FIFO data also sent by SiTCP connection for offline checking
  - Errors observed offline same order, but some behaviour unclear whether occurs in BRAM or SiTCP



Region	SEU Rate $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$	URE Rate $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$
CRAM	$(5.0 \pm 1.6) \times 10^{-8}$	$(7.9 \pm 2.6) \times 10^{-10}$
Region	**SEU Rate** $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$	**MBE Rate** $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$
BRAM	$(1.8 \pm 0.6) \times 10^{-9}$	$(5.3 \pm 1.7) \times 10^{-10}$

$$\textbf{Error Rate} = \frac{\textbf{Errors}}{\textbf{Neutron Fluence}}$$

Results consistent with previous measurements (accounting for different FPGA size) [7].

[7] Y.Nakazawa et al. "Radiation study of FPGAs with neutronbeam for COMET Phase-I". In:Nucl. Instrum. Method A936(2019), pp. 351–352, DOI:https://doi.org/10.1016/j.nima.2018.10.130.

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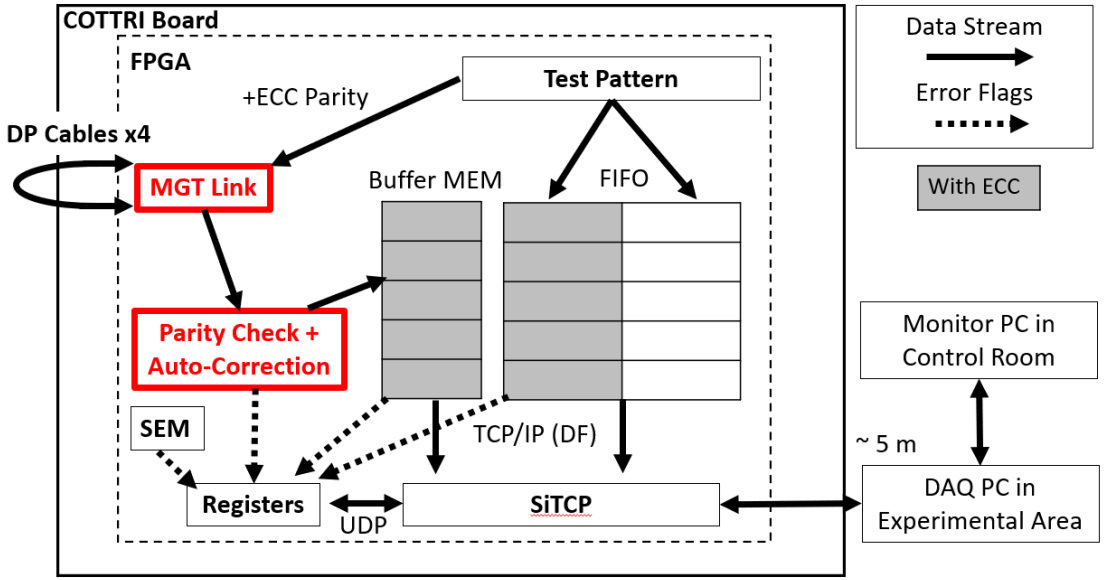
Multi-Gigabit Link

- Parity check/correction ECC used upon 100 ns internal trigger as data sent to ring buffer
- Observed smaller number of SEU/MBE in MGT link compared with the CRAM/BRAM error
  - ➢ Resolved in 1 s so treat as 1 s deadtime
  - ➢ In future, tagging could be used



SEC (s)	LCC (s)	Total Time (s)
44	43	87

- Time period affected by soft error counts (**SEC**) and lost connection counts (**LCC**) also recorded.
  - ➢ Manageable considering total data collection (**150 days**)

SEU Rate $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$	MBE Rate $[\mathrm{n}\cdot\mathrm{cm}^{-2}]^{-1}$
$(7.1 \pm 2.3) \times 10^{-10}$	$(2.1 \pm 0.9) \times 10^{-12}$

- Error rates observed **per 4.8 Gbps MGT link** section (total of 8 links).
- Observed 10 additional erratic counter errors
  - ➢ Should be treated same as URE.
- Rest of SEU resolved by parity check module.

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URE Impact

Observed that **most significant impact** will come from **CRAM URE rate**.

Expected CRAM URE	MGT Link URE	Total Expected URE Rate	Total expected dead time (60 s per URE)	Total expected dead time (30 s per URE)
7900	100	$(2.2 \pm 0.7)\ \mathrm{hr}^{-1}$	$(3.7 \pm 1.2)\%$	$(1.9 \pm 0.6)\%$

Estimated the effect for the **150 day** COMET Phase-I data collection by to obtaining total percentage dead time using:

- CRAM URE Rate per COTTRI Front-End (**FE**) board (**10 in total**)
- Observed MGT Link URE behaviour
- Expected dead time per URE (**60 s conservative** estimate although optimistically closer to **30 s observed**)

MGT Link Impact

Observed that **comparatively small impact** will come from **MGT Link**. Most SEU resolved by parity check module and other non-URE type errors lasted no more than 1 s each in impact

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BRAM MBE Impact

Observed that **BRAM MBE rate** not insignificant.

Trigger Window Size (bits per trigger)	MBE Rate $[\mathrm{n} \cdot \mathrm{cm}^{-2}]^{-1}$	Expected Errors
2 bit ADC × 480 RECBE Channels × 10 CLK cycles = 9600	$(5.3 \pm 1.7) \times 10^{-10}$	2.4 ± 0.8

Estimated effect on trigger data over **150 day** COMET Phase-I data collection by looking at total MBE expected using:

- Trigger window size
- BRAM MBE rate

It can be estimated that we expect 24 ± 8 errors in trigger data for **10 FE boards** over the course of the Phase-I experiment.

Already have proposed solutions for decreasing BRAM MBE:

- **Tagging System** – tag all MBE affected data
- **BRAM Block Allocation** – allocate smaller BRAM block memory (128×32767 bit blocks used for these measurements)
- **BRAM Triple Modular Redundancy** – allocate $3 \times$ all memory blocks

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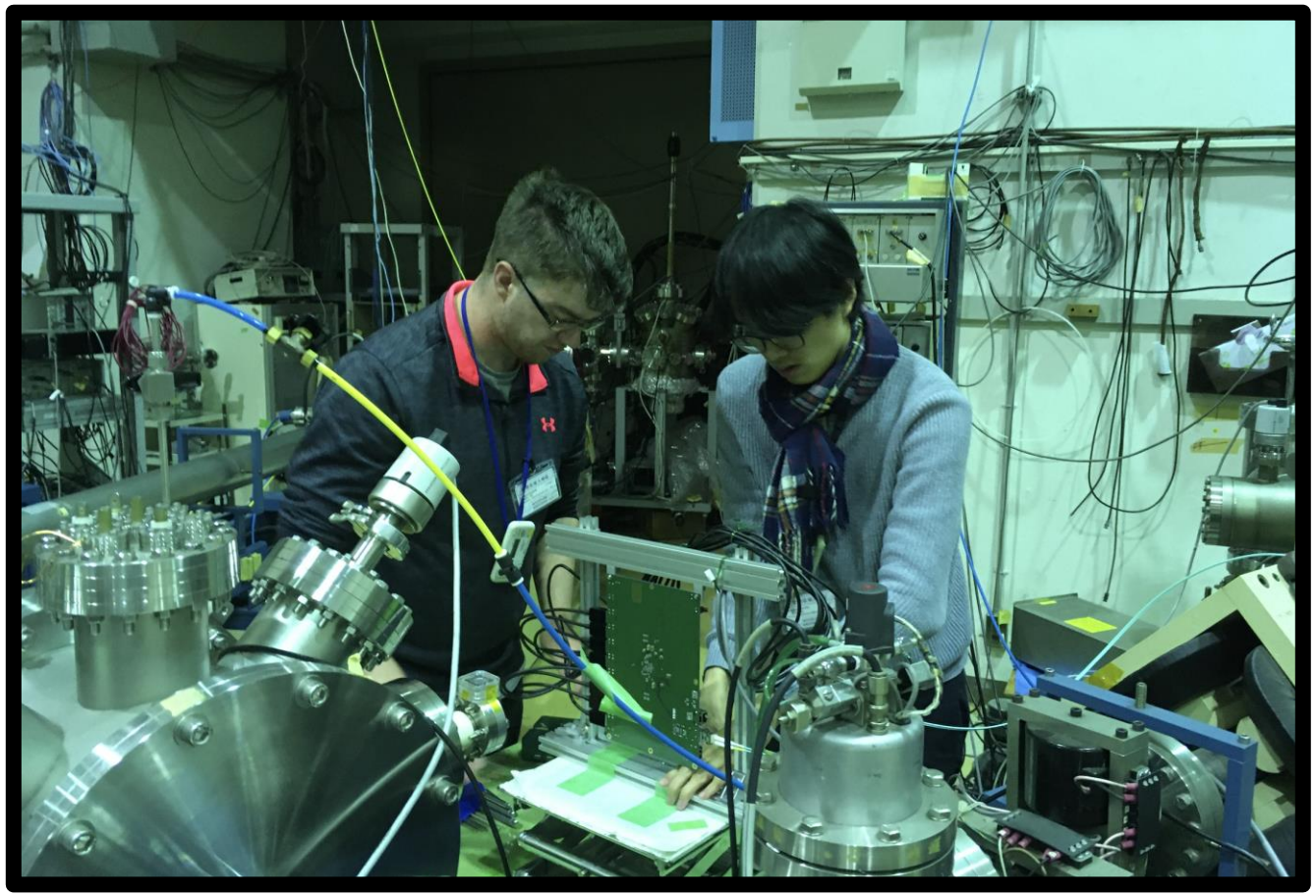
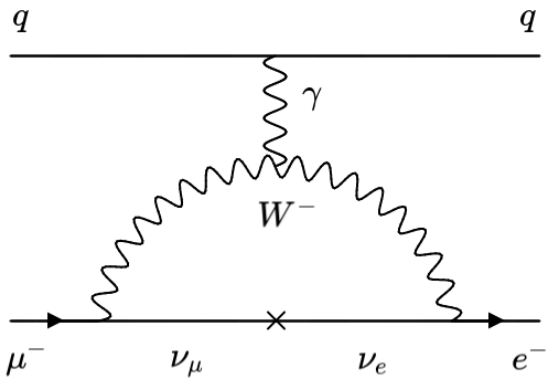


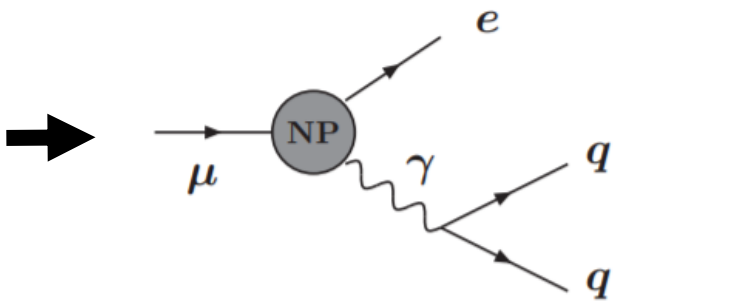
Charged Lepton Flavour Violation



Standard Model + Neutrino Oscillations

$\sim\mathcal{O}(10^{-56})$

Undetectable!



New Physics (e.g. supersymmetry?)

Up to $\sim\mathcal{O}(10^{-15})$

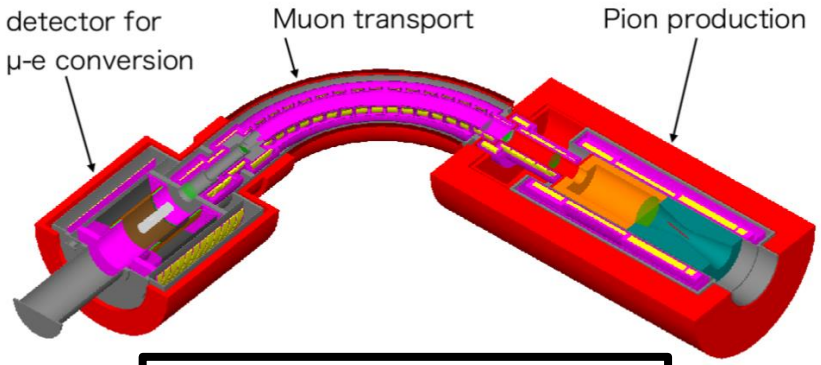
Detectable!

Backup

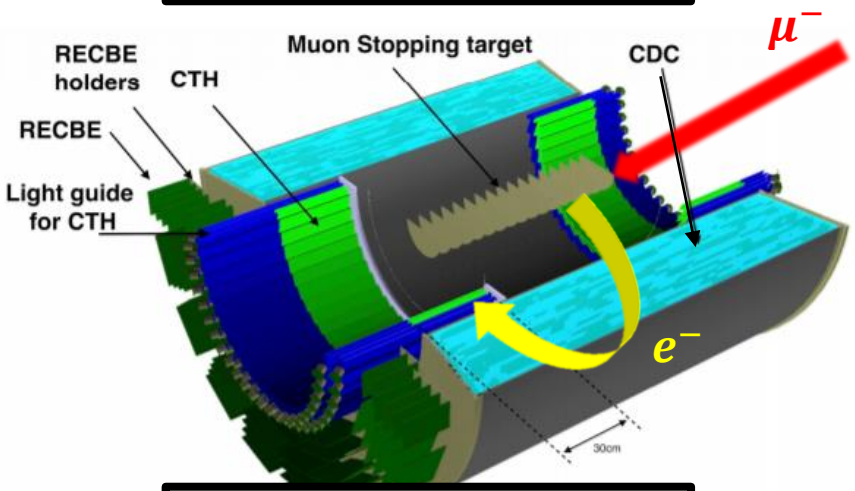
[1] G.Adamov, *et.al*, "COMET Phase-I Technical Design Report", 2020(3)

COMET

(**CO**herent **M**uon to **E**lectron **T**ransition)



COMET Phase-I Layout



CyDet Cross-section

[1] Images from G.Adamov, *et.al*, "COMET Phase-I Technical Design Report", 2020(3)

Searching for charged lepton flavour violation process:

$$\mu^- N \rightarrow e^- N$$

Observation signals **new physics**: COMET will measure at new sensitivity levels ($\approx 3 \times 10^{-15}$ in Phase-I)

Overview of CyDet Detector

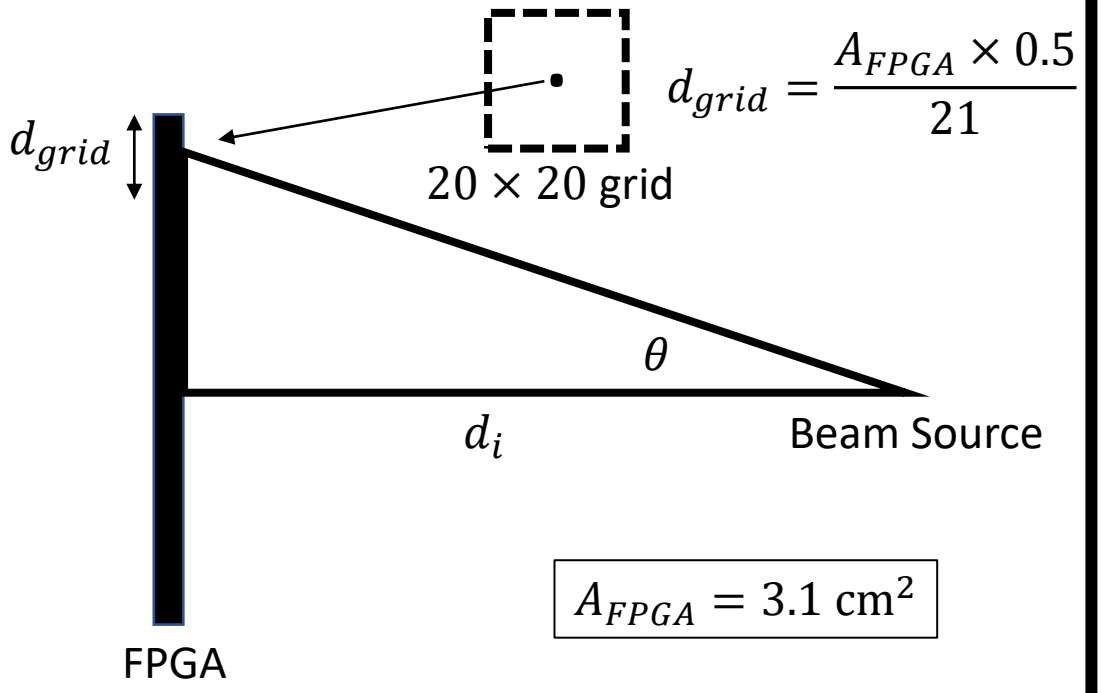
- Inside 1 T detector solenoid
- CDC (**C**ylindrical **D**rift **C**hamber)
  - Electron momentum measurements
  - Trigger: Charge/timing information, looking for 'signal' like hits
- CTH (**C**yDet **T**rigger **H**odoscope)
  - Each end of CDC, consist of two overlapping layers of tilted counters
  - Electron timing measurements (time of flight in CDC)
  - Trigger: 4-fold hit coincidence in scintillating layers (to suppress backgrounds)

Backup

Neutron Fluence

Total Neutron Fluence (1 MeV Equivalent)

$(1.0 \pm 0.3) \times 10^{12}$ n $\cdot$ cm^{-2}



A grid is imposed on the surface area of the FPGA chip in order to account for angular effects when determining neutron fluence.

Conversion between beam current and neutron fluence based on absolute conversion factor measured previously at 10 cm:

$$CF_{10} = (4.9 \pm 1.5)\ \text{MHz} \cdot\ \text{n} \cdot \text{cm}^{-2} \cdot \mu\text{A}^{-1}$$

$C_\theta = 0.0068$ (Angular conversion factor)

Total Conversion Factor:

$$CF_i = CF_{10}(0.96 - C_\theta\theta)\frac{10.0^2}{d_i^2}$$

where d_i is the distance between beam source and COTTRI board

Total Neutron Fluence:

$$NF = \sum_i (CF_i \times IC_i)$$

where IC_i is the integrated beam current for distance d_i.

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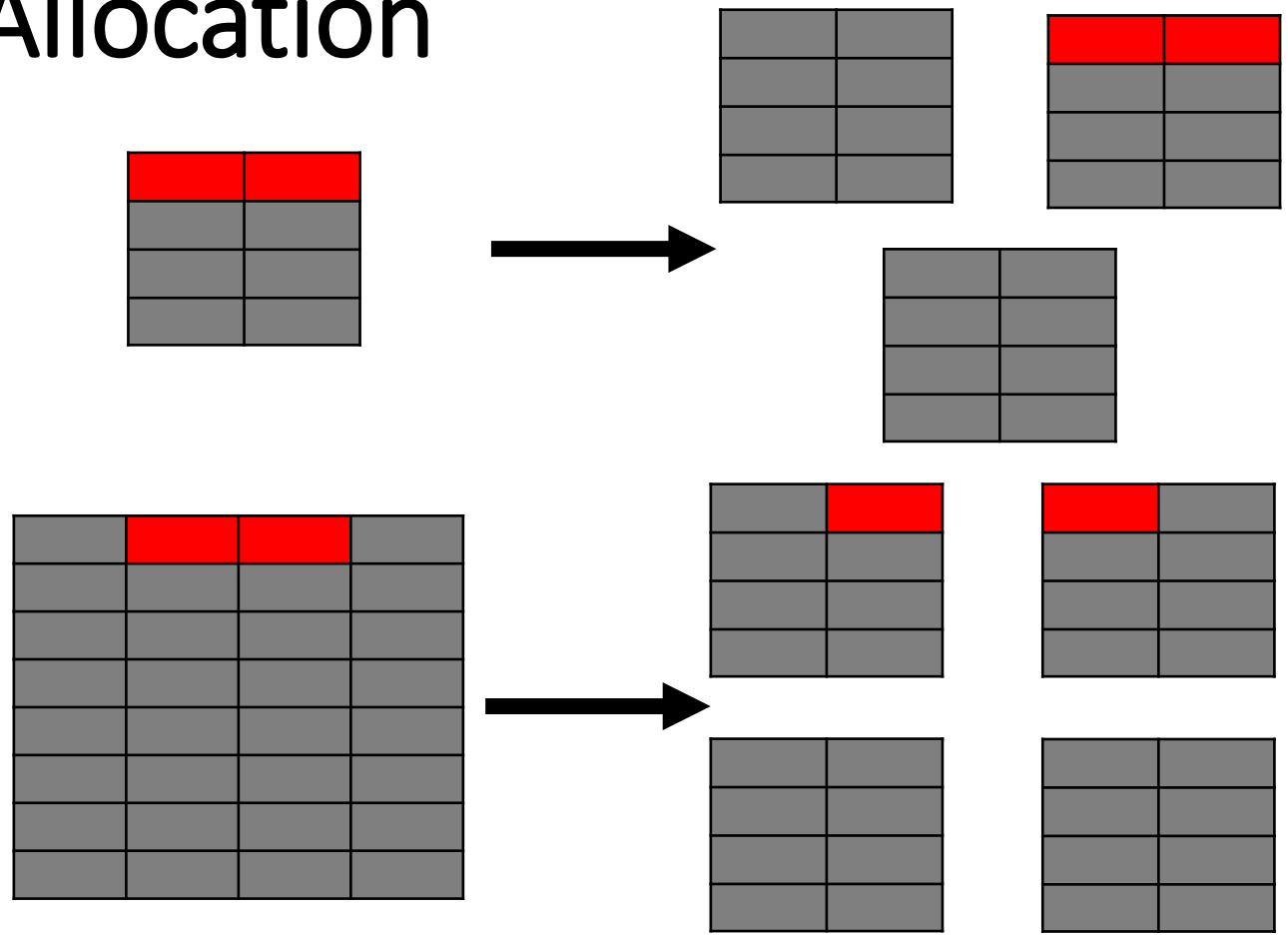
Memory Allocation



Examples for memory allocation in BRAM to improve MBE rate

Top: Triple modular redundancy – repeat same memory block three times. If there is an MBE in data in one block, choose the data pattern stored in two of the blocks.

Bottom: Allocate smaller blocks in memory. By using smaller block sizes (at the cost of more resources), the chance of an MBE can be lowered and thus a lower MBE rate is possible.

Backup