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The threshold voltage generation for CMS ETL readout ASIC

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We present the threshold voltage generation for CMS Endcap-Timing-Layer (ELT) readout ASIC called ETROC. ETROC together with the chosen sensor, low gain avalanche diode (LGAD), aim to achieve time resolution of 30˜40 ps per track. In the analog front-end of ETROC, a pre-amplifier amplifies the signal from LGAD sensor, and then a discriminator converts the pre-amplifier signal into digital pulses for succeeding time-to-digital conversion and readout. The discriminator requires a programmable precision threshold voltage to cover the possible pre-amplifier signal range from 0.6 V to 1.0 V with a fine step size. The proposed threshold voltage generation network includes a reference generation network and a threshold voltage generator.
The threshold voltage generator has been implemented in ETROC0, the first prototype of ETROC, in a 65 nm CMOS technology. It includes a 10-bit digital-to-analog converter (DAC) and a noise filter. A two-stage resistor string structure is used in the DAC to achieve a monotonic adjustment curve. The first stage implements the 5-bit most significant bits (MSB) and the second stage determines the 5-bit least significant bits (LSB). The noise filter is used to filter out high-frequency noise and limit the noise well below the pre-amplifier noise. The threshold voltage generator measures differential nonlinearity (DNL) and integral nonlinearity (INL) of ±0.15 LSB and ±1.2LSB, respectively. The power consumption is 80 uA.
The reference generation network has been implemented in a separate prototype recently. Test results are expected to be presented at the conference.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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