The threshold voltage generation for CMS ETL readout ASIC

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Abstract

We present the threshold voltage generation for CMS Endcap-Timing-Layer (ELT) readout ASIC called ETROC. ETROC together with the chosen sensor, low gain avalanche diode (LGAD), aim to achieve time resolution of 30~40 ps per track. In the analog front-end of ETROC, a pre-amplifier amplifies the signal from LGAD sensor, and then a discriminator converts the pre-amplifier signal into digital pulses for succeeding time-to-digital conversion and readout. The discriminator requires a programmable precision threshold voltage to cover the possible pre-amplifier signal range from 0.6 V to 1.0 V with a fine step size. The proposed threshold voltage generation network includes a reference generation network and a threshold voltage generator.

The threshold voltage generator has been implemented in ETROC0, the first prototype of ETROC, in a 65 nm CMOS technology. It includes a 10-bit digital-to-analog converter (DAC) and a noise filter. The reference generation network has been implemented in a separate prototype recently. Test results are expected to be presented at the conference.

Introduction

Endcap timing readout chips (ETROC) have been under development as the front-end electronics of the ETL since second half of 2018 and aim to have production run in 2023. ETROC is a pixelated readout ASIC with a 16 by 16 pixel-array and supporting circuits on the bottom of the chip. The analog part of the readout chain which includes the pre-amplifier and the discriminator is critical for LGAD-based precision time measurement. The baseline of the pre-amplifier in different pixels spread a significant range because of the mismatch and varies over time due to the variation of temperature and radiation accumulated, which mean each pixel will have its own threshold and calibration should be performed from time to time if not regularly to find out an optimum threshold.

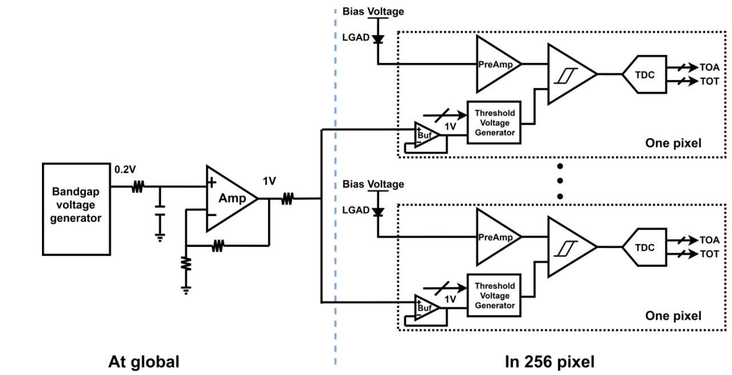


Figure 1. The block diagram of threshold voltage generation network in ETROC .

Design

Figure 1 shows the block diagram of the threshold voltage generation in ETROC. The threshold generation network includes the threshold voltage generator in each pixel and the associate voltage reference generation network. At the global, a 200 mV bandgap voltage is provided by a bandgap voltage generator. A low-pass RC filter is used to filter out high frequency noise of the bandgap voltage. The bandgap voltage is amplified to the target value of 1 V before being distributed to the pixel array. In each pixel, the threshold voltage generator uses the 1 V voltage reference to generate the threshold voltage for the discriminator.

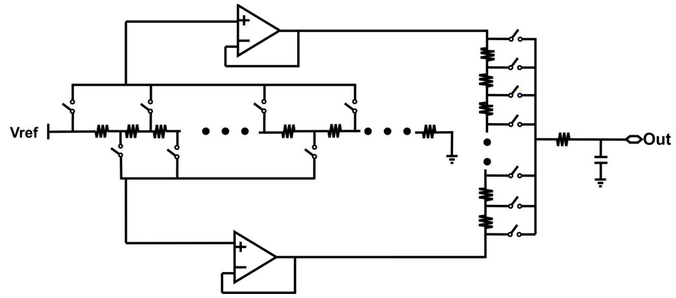
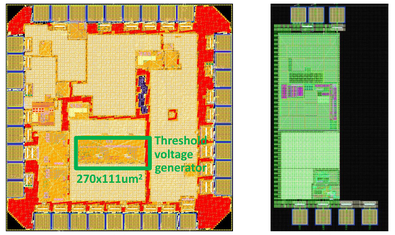


Figure 2. Simplified schematic of the threshold voltage generator .

Figure 2 shows the block diagram of the threshold voltage generator. It includes a 10-bit resistor string DAC and a RC filter. Two unity-gain buffers are used to remove the loading effect of the second stage. Biased with a 1 V voltage reference, the DAC is designed to cover the range from 0.6 V to 1 V, with the LSB of about 0.4 mV. A first-order RC filter is designed such that the noise of the generated threshold output is well below the pre-amplifier noise.

The threshold voltage generator has been implemented in ETROC0, the first prototype of ETROC.The voltage reference generation network was implemented in a different chip recently. Figure 3 include the layout of ETROC0 and the voltage reference generation network.



(a) (b)

Figure3. (a) The layout of ETROC0, in which the threshold voltage generator is highlighted. (b) The reference generation network layout.

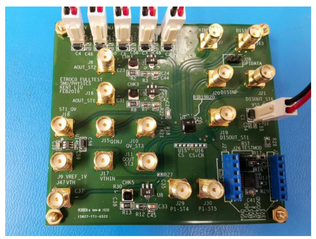


Figure4. ETROC0 test board .

Test Results

Figure 4 and Figure 5 (a) shows the test board and the test setup of the threshold voltage generator with ETROC0 chip. In the test the code of the DAC was sent into the chip through SPI, and the generated threshold voltage was measured with a voltage meter. The 1 V reference voltage was generated with an off-chip voltage reference chip in the test.

Measurement results are shown in figure 5. The generated threshold voltage covers range from 0.6064V to 0.9986V. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) is better than ±0.15 LSB and ±1.2 LSB, respectively. All these parameters meet the requirement of ETROC.

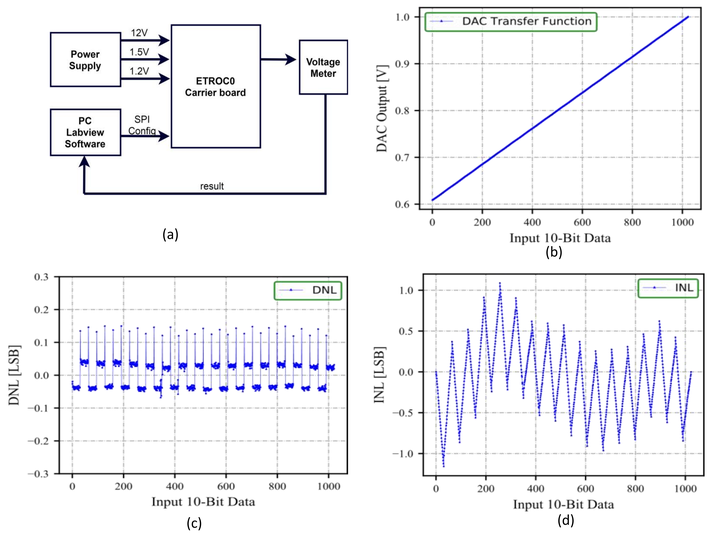


Figure 5. (a) The diagram of the threshold generation circuits test setup. (b) measured threshold voltage, (c) DNL, and (d) INL.

Conclusions

We have presents an threshold generation design and tested for CMS ETL readout chip (ETROC). The threshold voltage generator achieves the DNL and INL of ±0.15 LSB and ±1.2LSB, and the consumption is 96 uW. Meet the requirement of use. For the reference generation network , the test work is on the going , and result will be presneted in the paper.

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