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The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL

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The analog front-end for the Low Gain Avalanche Detector (LGAD) based precision timing application in the CMS Endcap Timing Layer (ETL) has been prototyped in a 65 nm CMOS mini-ASIC named ETROC0. Serving as the very first prototype of ETL readout chip (ETROC), ETROC0 aims to study and demonstrate the performance of the analog front-end, with the goal to achieve 40 to 50 ps time resolution per hit with LGAD (therefore reach about 30ps per track with two detector-layer hits per track). ETROC0 consists of preamplifier and discriminator stages, which amplifies the LGAD signal and generates digital pulses containing time of arrival (TOA) and time over threshold (TOT) information. The actual TOA and TOT measurements will be done with a time-to-digital converter (TDC) downstream and is not part of the ETROC0. ETROC0 chips have been tested extensively using charge injection, laser, cosmic rays as well as beam, and the measured performance agrees well with simulation. The initial beam test at Fermilab has demonstrated time resolution of around 33 ps from the preamplifier waveform analysis and around 42 ps from the discriminator pulses analysis. A subset of ETROC0 chips have also been tested to a total ionizing dose (TID) of 100 MRad using X-ray machine at CERN and no performance degradation been observed. The ETROC0 design is successful and is directly used without modification for the next prototype chip, ETROC1, which has 5x5 pixel arrays and includes a new TDC stage and H-tree style clock distribution.

Minioral

Yes

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No

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No

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