The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL

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Introduction

MIP timing detector(MTD) is a new detector on CMS approved for HL-LHC to measure precisely production time of minimum ionizing particles (MIP), which includes the Barrel Timing Layer (BTL) and Endcap Timing Layer (ETL).

ETL aims for 30-40 ps time resolution at the beginning of the operation and 50-60 ps by the end of the operation. There will be two detector layers on each endcap, relaxing time resolution to 40-50 ps per hit. Low Gain Avalanche Detector (LGAD) with Most Probable Value (MPV) charge of around 15 fC will be used as the sensor.

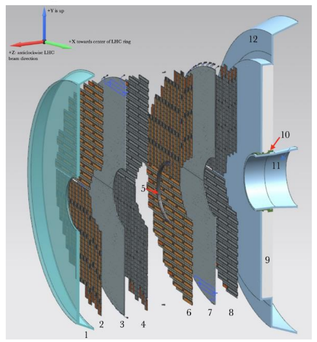

Figure 1. CMS Endcap Timing Layer

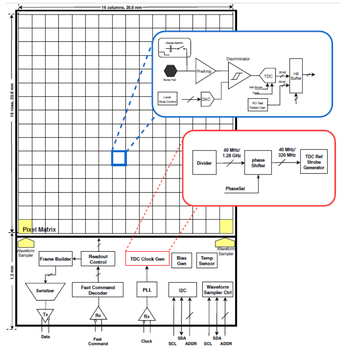

Figure 2. Block Diagram of ETROC

ETL Readout Chip (ETROC) will be designed to include a 16 x 16 pixel matrix, each pixel cell being 1.3 x 1.3 mm^2 to match with the LGAD sensor pixel size. The design goal for the time resolution is 50 ps per hit, in order to achieve a 35 ps arrival time measurement for a MIP track with an ETL hit in each of the two layers. A major challenge of ETROC is precision time measurement at tight power budget (1 W/chip) and small signal (15 fC). ETROC will tolerate a total ionizing dose(TID) of 100 Mrad.

The analog front-end design

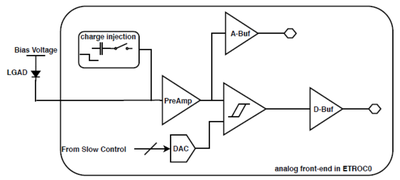

Figure 3. Block diagram of the analog front-end implemented in ETROC0

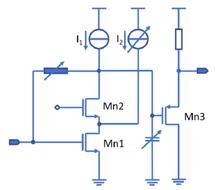

Figure 4. Simplified schematic of the pre-amplifier

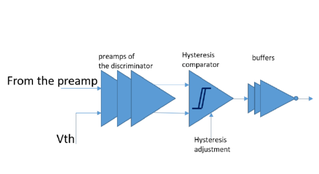

Figure 5. Architecture of the discriminator

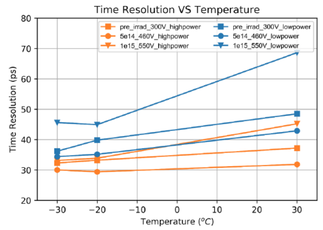

Figure 6. Analog front-end simulation with LGAD data from WeightField2.

The first prototype chip for CMS ETL, ETROC0, has been developed, aiming for exploring the performance of the analog part of the front-end readout circuits (analog front-end). A preamplifier, a discriminator and a DAC for threshold generation were implemented in ETROC0 to form the analog frontend. A charge injector was included to facilitate the test. Signal at the output of the pre-amplifier and the discriminator are accessible through an analog buffer and a digital buffer, respectively.

In order to evaluate the overall performance of the analog front-end in ETROC0 and the LGAD sensor in the simulation stage, LGAD data from WeightField2 simulation was applied to the circuits SPICE simulations at post-layout level. LGAD with different irradiated levels were used in the simulations. Different bias settings and temperature conditions were applied to the analog front-end in the simulation. Results show that even the worst case expected time resolution per hit is still below the required 50 ps at the operation temperature of -20 ºC, with best case (beginning of operation) down to around 30 ps.

ETROC0 Test

ETROC0 is a 1 x 1 mm^2 chip in 65 nm CMOS process. ETROC0 bare dies were glued onto the PCBs and directly wire-bonded to the pads on the boards. Two sets of PCB were developed to carry out the tests. One set is used for the charge injection and the TID test and the other set for the tests involving LGAD sensors.

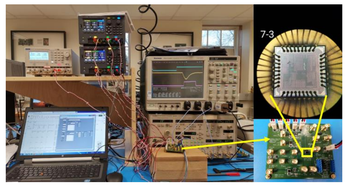

Figure 7. Setup of the charge injection test.

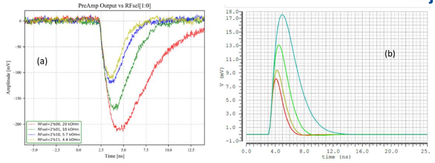

Figure 8. Waveform of the pre-amplifier with 6 fC charge input at gain settings, (a) measured, (b) simulated.

The pre-amplifier was tested by injecting charge. A commercial amplifier with gain of -10 was used to amplify the signal on the PCB. The on-chip buffer has a typical gain of 0.7.

The jitter of leading edge was measured with charge injection. The threshold was placed 9 DAC LSBs, about 3.6 mV about the pre-amplifier baseline. Since the charge injection pulse from the signal generator is faster (about 25 ps), the signal seen by the pre-amplifier is faster than an actual LGAD signal.

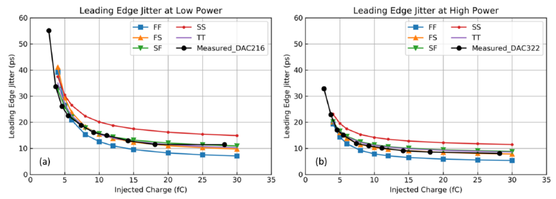

Figure 9. Leading edge jitter from measurement and simulation, (a) low power, (b) high power.

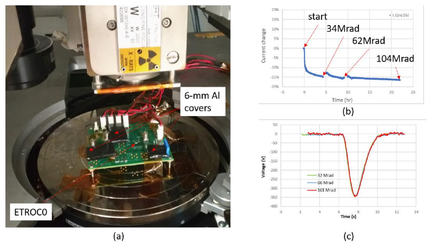

Figure 10. TID test, (a) x-ray test setup at CERN, (b) the current of the preamp, (c) the waveforms of the preamp.

A few ETROC0 chips were irradiated to 100 Mrad (ETROC spec.) with x-ray for TID test at CERN. The current of the preamp was monitored during the test and was found to drop by 15% during irradiation, no difference was observed from the preamp output waveform. The chips were then extensively tested after the irradiation over a few weeks and no performance degradation was observed when compared with the performance before the TID testing.

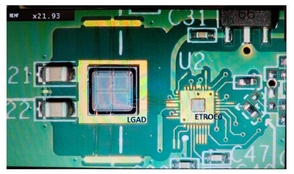

Figure 11. ETROC0-LGAD sensor connection.

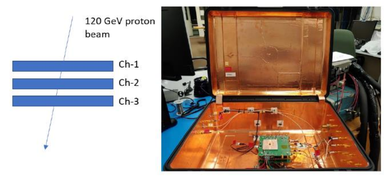

Figure 12. A simple telescope with 3 ETROC0 boards for ETROC0 beam test

$$\begin{cases} \sigma_{21}^2 = \sigma_2^2 + \sigma_1^2, \\ \sigma_{31}^2 = \sigma_3^2 + \sigma_1^2, \\ \sigma_{32}^2 = \sigma_3^2 + \sigma_2^2. \end{cases}$$

$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{32}^2 + \sigma_{21}^2 - \sigma_{31}^2)}$$

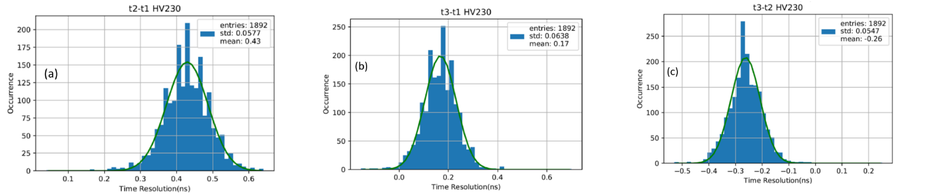

Figure 13. Inter-channel TOA of the preamp waveform with constant fractional discrimination applied at 230 V. 33 ps time resolution is derived.

ETROC0 was tested in FermiLab test beam facility at room temperature with a 2 x 2 LGAD sensor and 120 GeV proton. A 3-layer telescope was tested in the beam, with layer 1 and layer 3 the reference and layer 2 the board under test (BUT).

Time resolution of 33 ps can be derived from the pre-amplifier output with constant fraction discrimination applied. And the time resolution of 42 ps is derived from the discriminator output with TOT based time walk correction applied.

Summary and Acknowledgement

ETROC analog front-end has been prototyped and tested extensively with good performance. The analog front-end has been used in the next prototype chip, ETROC1, without modification.

We would like to thank Syzmon Kulis and Paulo Moreira for the support of common circuitry.

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