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A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

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We present the design and test results of a Time-to-Digital-Converter (TDC) functional block. The TDC will be a part of the readout ASIC, called ETROC, of the Low-Gain Avalanche Detectors (LGADs) for the CMS Endcap Timing Layer (ETL) of High-Luminosity LHC upgrade. One of the challenges of the ETROC design is that the TDC is required to consume less than 200 mW for each pixel at the nominal hit occupancy of 1%. The TDC is based on a simple delay-line approach originally developed in FPGA implementation. In order to meet the low power requirement, we use a single delay line for both the Time of Arrival (TOA) and the Time over Threshold (TOT) measurements without delay control. A double-strobe self-calibration scheme is used to achieve high performance. The TDC is fabricated in a 65 nm CMOS technology mini-ASIC. The TOA has a bin size of 17.8 ps and a precision of around 5.4 ps. Within its effective dynamic range of 11.4 ns, the Differential Non-Linearity (DNL) is better than ±0.5 LSB and the Integral Non-Linearity (INL) is less than ±1.0 LSB. The TOT has a bin size of 35.4 ps, twice the TOA bin size, and a precision of about 10 ps. The DNL and INL of the TOT are ±0.8 LSB and ±1.3 LSB, respectively. The calibration process functions as expected. The actual TDC block consumes about 100 mW at the hit occupancy of 1%. The overall measured performance of the TDC meets the CMS ETL upgrade requirements.

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