A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) upgrade

Wei Zhang[1,2], Hanhan Sun[1,2], Christopher Edwards[3], Datao Gong[*,1], Xing Huang[1,2], Chonghan Liu[1], Tiankuan Liu[1], Tiehui Liu[3], Jamieson Olsen[3], Quan Sun[3], Xiangming Sun[2], Jinyuan Wu[*,3], Jingbo Ye[1], and Li Zhang[1,2]

[1] Southern Methodist University, Dallas, TX 75275 USA [2] Central China Normal University, Wuhan, Hubei 430079, China [3] Fermi National Accelerator Laboratory, Batavia, IL 60510 USA

(22nd Virtual IEEE Real Time Conference) *dgong@smu.edu *jywu168@fnal.gov

Abstract

We present the design and test results of a Time-to-Digital-Converter (TDC) functional block. One of the challenges of the TDC is required to consume less than 200 uW at the nominal hit occupancy of 1%. The TDC is based on a simple delay-line approach for both the Time of Arrival (TOA) and the Time over Threshold (TOT) measurements without delay control. A double-strobe self-calibration scheme is used to achieve high performance. The TOA has a bin size of 17.8 ps and a precision of around 5.4 ps. The Differential Non-Linearity (DNL) is better than ±0.9 LSB and the Integral Non-Linearity (INL) is less than ±1.0 LSB. The TOT has a bin size of 35.4 ps. The calibration process functions as expected. The TDC block consumes about 100 uW at the hit occupancy of 1%.

Design of the TDC

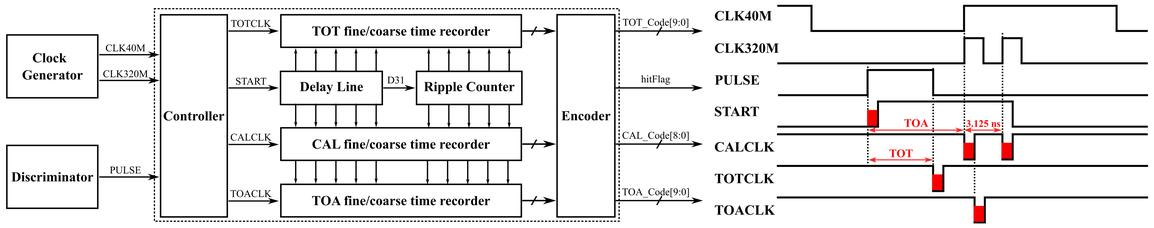


Figure 1: Block diagram of the TDC and timing diagram of the major signals

Our TDC design is based on a simple untuned delay-line approach for both the Time of Arrival (TOA) and Time over Threshold (TOT) measurements.

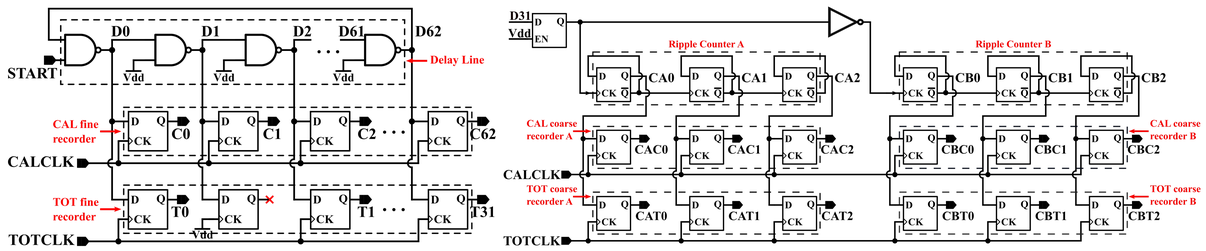


Figure 2: Schematic of the fine and coarse time measurement circuit

The CALCLK signal has two consecutive pulses in every 25 ns with a fixed offset of 3.125 ns. The first pulse represents the TOA information and the second one is for in-situ time calibration.The falling edge of the TOTCLK is aligned with the falling edge of the signal PULSE. The TOTCLK is used to record TOT time information.

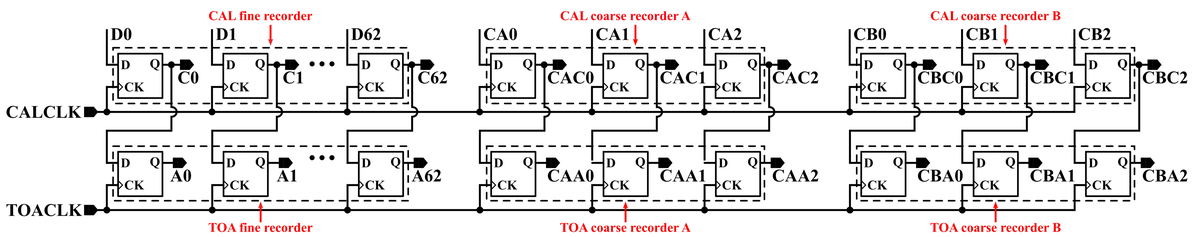
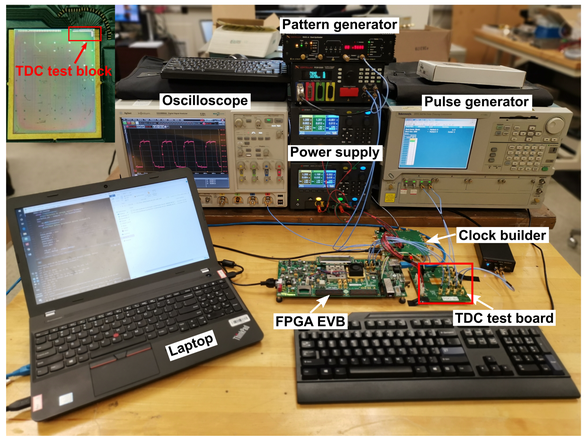


Figure 3: Schematic of the calibration and the TOA recorder

The TOA time information is carried by the CALCLK and TOACLK signals.

Test results of the TDC



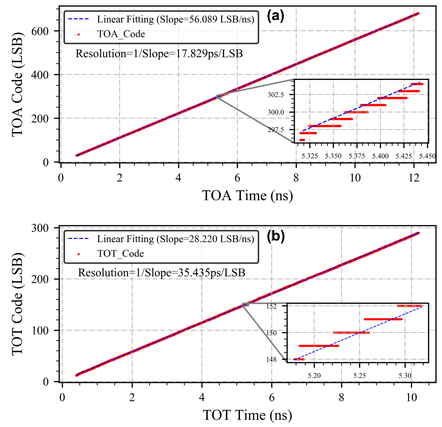
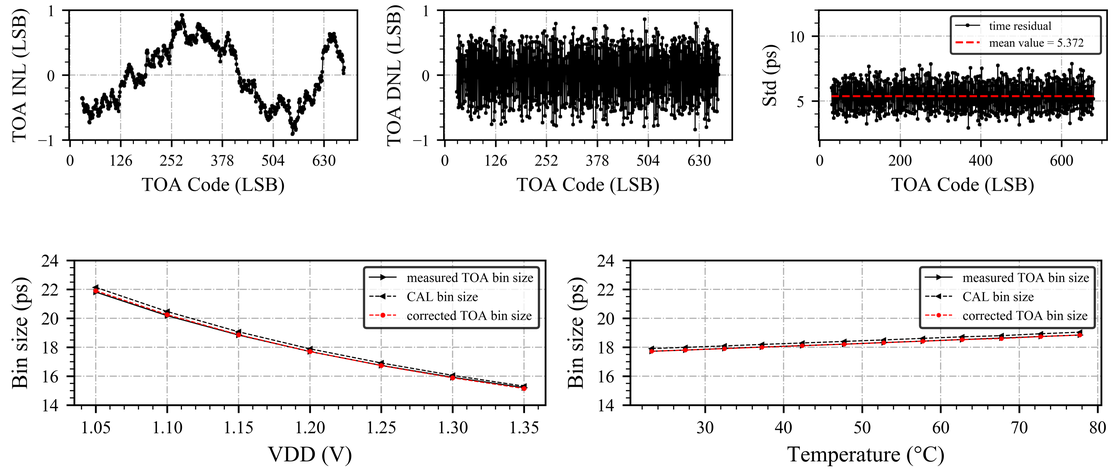


Figure 4: TDC test setup and TOA/TOT transfer function

The bin size of the TOA and TOT are estimated to be 17.83 ps and 35.43 ps, respectively.



The INL and DNL of TOA are better than ± 1.0 LSB and ± 0.9 LSB, respectively and the precision is about 5.4 ps. The calibration process functions are as expected at different voltage and temperature.

Conclusion

We have successfully designed and tested a delay-line based TDC in a commercial 65 nm CMOS technology. The TDC achieves the consumption of 97 uW per pixel at the hit occupancy of 1%. The measured performance of the TDC meets the requirement for the ETROC for the CMS ETL project.

Acknowledgments

Thanks Szymon Kulis for providing us with I2C slow contoller.

References

Jinyuan Wu, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay,"