A 10 Gbps Driver/Receiver ASIC and Optical Modules for Particle Physics Experiments

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INTRODUCTION

We present the design and test results of a Drivers and Limiting AmplifierS operating at 10 Gbps (DLAS10) and Miniature Optical Transmitter /Receiver/Transceiver modules (MTx+, MRx+, and MTRx+) based on DLAS10.

CHIP DESIGN

DLAS10 has two channels. Each channel of DLAS10 consists of an input buffer, a four-stage Limiting Amplifier (LA), and an output driver.

The conventional Continuous-Time Linear Equalization (CTLE) are used in the input buffer.

An active feedback is adopted in the LA to accommodate the Processes, Voltages and Temperatures (PVTs) variations.

The output driver is based on Current-Mode Logic (CML) structure.

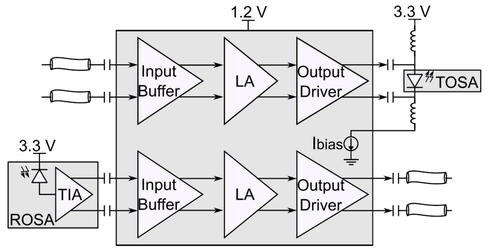


Fig. 1. Block diagrams of DLAS10 in the use case of MTRx+.

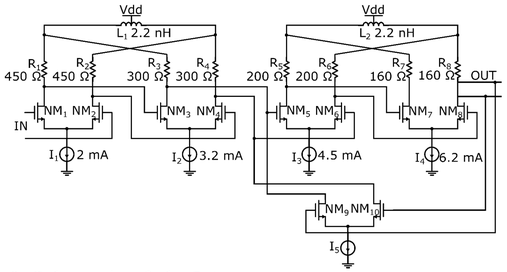


Fig. 2. Schematic of the LA.

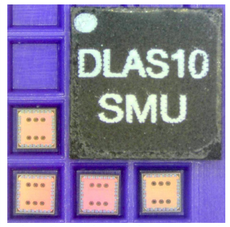
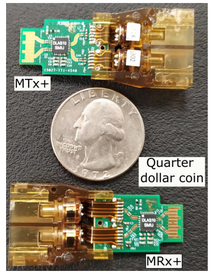


Fig. 3. Microphotograph of the die.

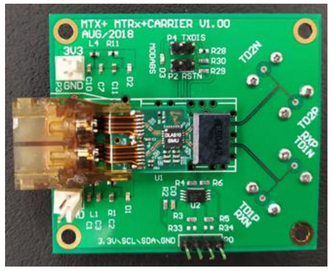
DLAS10 is fabricated in a 65 nm CMOS technology. The die is 1 mm × 1 mm. DLAS10 is packaged in a 4 mm × 4 mm 24-pin quad-flat no-leads (QFN) package.

MODULE DESIGN

Matching DLAS10 with a Transmitter Optical Sub-Assembly (TOSA) and a Receiver Optical Sub-Assembly (ROSA) with only Trans-Impedance Amplifier (TIA), and with a custom optical coupler, MTx+/MRx+/MTRx+ offers an economical option with a robust electrical connector and receives fibers with the LC connectors. The modules stay below 6 mm in height and are both board and panel mountable.



(a)

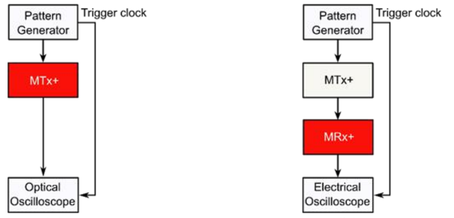


(b)

Fig. 4. (a) picture of MTx+ and MRx+; (b) MRx+ mounted on carrier board.

TEST SETUP

DLAS10 has been tested in MTx+, MRx+, and MTRx+ modules. A pattern generator (CENTELLAX TG1C1-A with a clock module CENTELLAX PCB12500) provides 10 Gbps Pseudo-Random Binary Sequence (PRBS) signals. An optical oscilloscope (Tektronix TDS8000B) captures the optical eye diagrams of MTx+. An electrical oscilloscope (Tektronix DSA72004) measures the electrical eye diagrams of MRx+. For the MRx+ test, MTx+ is the optical source.

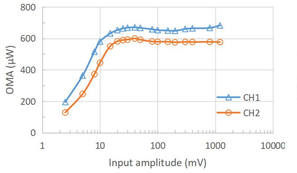


(a) (b)

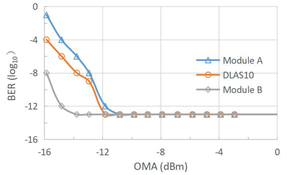
Fig. 5. (a) and (b) Test block diagrams of MTx+ and MRx+.

RESULTS

The input electrical sensitivity is 40 mVp-p, while the input optical sensitivity is -12 dBm.



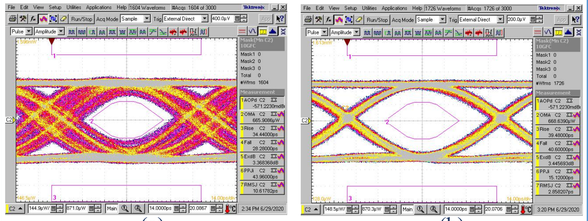
(a)



(b)

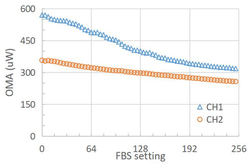
Fig. 6. (a) and (b) Sensitivities of MTx+ and MRx+.

Two 2 m long coaxial cables with SMA connectors are used to test input CTLE. When the input equalization is 62, the RMS jitter achieves 2.8 ps.



(a) (b)

Fig. 7. (a) and (b) Eye diagrams before and after equalization.

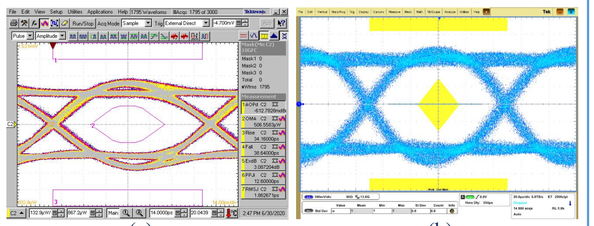


OMA decreases when the feedback strength (FBS) increases because of the gain of LA decreases.

Fig. 8. Dependence of the OMA on the feedback strength.

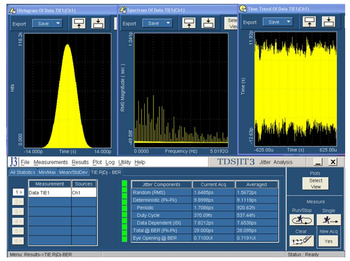
RESULTS (CONT.)

Both measured optical and electrical eye diagrams pass the 10 Gbps eye mask test.



(a) (b)

Fig. 9. (a) and (b) Eye diagrams of MTx+ and MRx+.



Total jitter 29 ps (P-P);
Random jitter 1.6 ps (RMS);
Deterministic jitter 9.9 ps.

Fig. 10. Jitter measurement of MRx+.

Each MTx+/MTRx+ module consumes 82 mW/ch and 174 mW/ch, respectively.

The radiation tolerance of DLAS10 and the ROSAs used in the MRx+/MTRx+ modules will be tested in the future. The previous prototype of DLAS10 and the TOSAs that are used in MTx+/MTRx+ have been verified to be radiation tolerant before.

CONCLUSION

DLAS10 has two channels each works up to 10.24 Gbps and can be configured to be two VCSEL drivers, or two receiver limiting amplifiers, or one driver and one receiver. The three variants, MTRx+, MTx+, and MRx+, cover the needs of optical transceiver, dual optical transmitter and receiver, for on-detector readout electronics outside the inner trackers.