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## A System-on-a-Chip based Front-end electronics control system for the HL-LHC ATLAS Level 0 muon trigger

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Exploiting commodity FPGAs in the front-end electronics is a standard solution for readout and trigger electronics for the HL-LHC. It requires the system to be capable of configuring, debugging and testing the firmware from a remote host. Furthermore, the control system is also responsible for monitoring and recovery in case of the SEU errors on the configuration memory of the FPGAs. Realizing such control capability is a unique challenge for the HL-LHC experiments. We have developed a control system to achieve such requirements with a new module exploiting System-on-a-Chip device as the solution for the Level-0 endcap muon trigger system of the LHC-ATLAS experiment. The new module named JATHub module will provide functionalities of flexible control of the system: configuration, testing, monitoring, and debugging the FPGAs on the front-end electronics. In addition, realization of the robust operation scheme for the possible radiation damage on the JATHub module is another essential item of development. We have invented a scheme to mitigate SEU errors on the SoC device and a redundant boot mechanism that will guarantee robust operations even in case of the radiation damages in the flash memory devices during the physics data taking with beam collisions. We have fabricated two prototype boards of the JATHub module. Demonstration study with the proto-modules will verify the concept of the use of SoC for the management of the front-end FPGAs in the experimental cavern of the collider experiments for HL-LHC.

### Minioral

Yes

### IEEE Member

No

### Are you a student?

Yes

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