Digital Trigger Module for Cherenkov Time of Flight Detector

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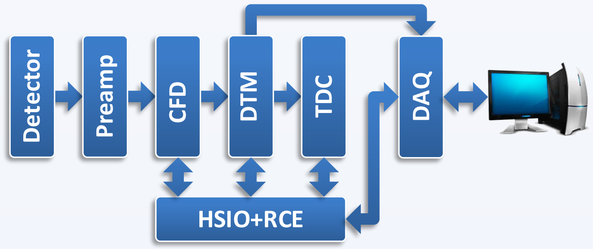
INTRODUCTION

The AFP Time-of-Flight (ToF) detector is located at LHC in CERN. Its main purpose is to measure the time delay of the detected high-energy protons during the multiple proton-proton collisions. Due to the high luminosity at LHC the number of events detected by ToF is enormous as well as the amount of data produced. The main purpose of the digital trigger module is to select the events relevant to the ongoing physical experiment.



The depicted ToF detector consists of following blocks:

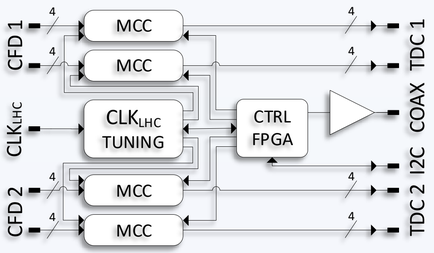
- Cherenkov particle detector - 4×4 quartz & photomultiplier
- 2 stages of preamplifiers
- Constant Fraction Discriminator (CFD)
- Digital Trigger Module (DTM)
- Time-to-Digital Converter (TDC)
- Data Acquisition System (DAQ)
- High-Speed I/Os & Reconfigurable Cluster Element (HSIO, RCE)

OBJECTIVES

The objective is to design a flexible DTM for processing of the CFD signals (i.e. selecting the relevant events). The required features are following:

- Passing/blocking of the individual columns (so-called trains) within the 4×4 matrix detector. The minimum Nr. of concurrent active signals is settable.
- Qualification of the CFD output signals within the 25 ns LHC bunch clock time window (400 ps – 8000 ps range).
- Sending of the DAQ commands via 265 m long cable.
- Processing the CFD signals up to 40 MHz rate.
- Remotely controlled via I2C, rad-hard design

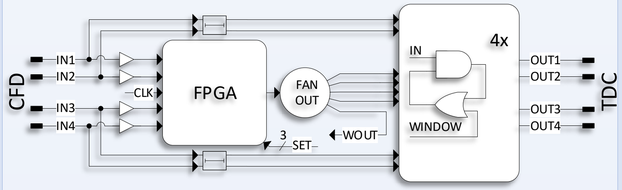
DEVICE ARCHITECTURE



The overall DTM architecture depicted above is based on the multichannel coincidence circuits. These circuits select the events related to the set conditions and subsequently pass/block the train signals on their way to the TDC.

The CLK_{LHC} tuning block prepares the CFD qualification signal synchronously to the LHC operating clock.

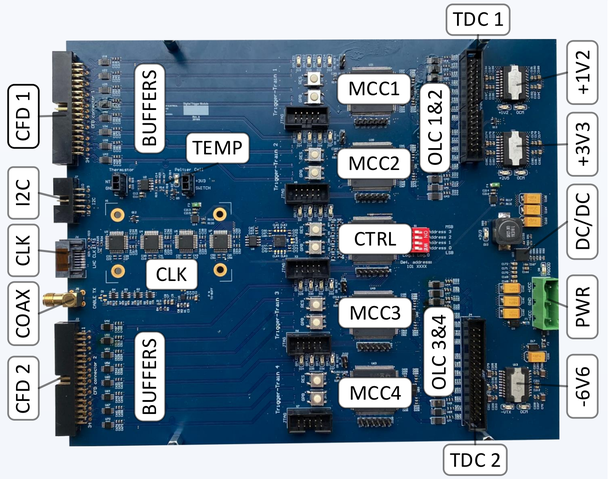
The CTRL FPGA controls the whole DTM (train conditions, qualification signal tuning, temperature measurement etc.) and communicates with the TDC (master) via I2C bus. This FPGA also sends the commands containing the activity of the individual trains to the DAQ via long coax cable.



This block diagram illustrates the MCC architecture. The CFD signals are processed in two parallel branches:

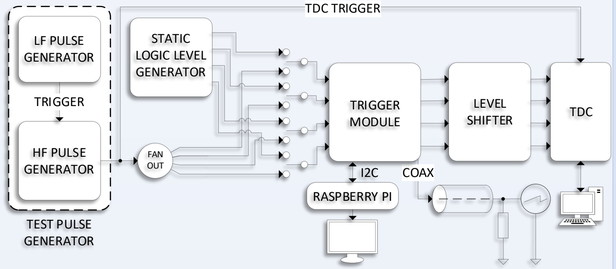
- The delay branch delays the signals on their way to the output latch circuits (OLCs) composed of AND&OR gates.
- The FPGA branch generates the short “window” pulse if the logical condition is set (the minimal number of active signals is reached). This pulse opens the OLCs for the incoming delayed CFD signals. In this case the CFD outputs are passed to the TDC (and otherwise blocked).

The WOUT signals go to the CTRL FPGA collecting the train activity and sending the commands to the DAQ.



The DTM circuitry is based on the rad-hard (or at least properly tested commercial off-the-shelf) components. The 2-slot NIM box is used as a form factor.

MEASUREMENT & RESULTS



The DTM efficiency is defined as the ratio between the correctly processed events and all events. Burst generator was used during the efficiency test. The number of dynamically generated signals within the individual tracks was changed accordingly to the set logical conditions. The time delay between the DTM input signals was changed in four steps (200/400/600/800 ps) in order to simulate the real CFD signals as they can be slightly shifted in a time domain.

The table below shows efficiency results for MCC3 tested by 40,000 test pulses per each input combination (i.e. 0 to 15 as the train is 4-bit wide). The errors occurred for signal delays higher the 400 ps. The expected maximum delay within the CFD signals is 300 ps and therefore the DTM timing is designed properly.

	CFD signal combination [-]															
INPUT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ER_{200ps} [%]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ER_{400ps} [%]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ER_{600ps} [%]	0	0	0	0	0	97	5	0	0	0	0	0	0	0	0	0
ER_{800ps} [%]	0	0	0	0	0	96	99	1	0	0	0	99	34	20	0	

The sending of the DAQ commands was tested at LHC in CERN. 265 m cable was used and no problems occurred.

Other features like I2C control, CLK tuning circuitry, temperature monitoring, MCC control etc. were successfully tested.

As the high-speed circuits are used (LVDS, LVPECL, CML IOs) the overall power consumptions reaches 18 W.

CONCLUSIONS

The performed tests proved the DTM proper function. The device will be soon tested in DESY in the full ToF chain and then installed at LHC in CERN for Run3.

REFERENCES

[1] Zich J., Georgiev V., Holík M., Pavlíček V., Vavroch O. Multichannel Coincidence Circuit with Settable Threshold Level for ToF AFP Detector. I*n: TELFOR. 2019.*

ACKNOWLEDGEMENT

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