



Contribution ID: 238

Type: Mini Oral and Poster

A reconfigurable neural network ASIC for detector front-end data compression

Tuesday 13 October 2020 16:05 (1 minute)

The next generation of particle detectors will feature unprecedented readout rates and require optimizing lossy data compression and transmission from front-end application-specific integrated circuits (ASICs) to off-detector trigger processing logic. Typically, channel aggregation and thresholding are applied, removing information useful for particle reconstruction in the process. A new approach to this challenge is directly embedding machine learning (ML) algorithms in ASICs on the detector front-end to allow for intelligent data compression before transmission. We present the design and implementation of an algorithm optimized for the High-Granularity Endcap Calorimeter (HGCAL) to be installed in the CMS Experiment for the high-luminosity upgrade to the Large Hadron Collider which requires 16x data compression at inference rates of 40 MHz. A neural-network (NN) autoencoder algorithm is trained to achieve optimal compression fidelity for physics reconstruction while respecting hardware constraints on internal parameter precisions, computational (circuit) complexity, and area footprint. The autoencoder improves over non-ML algorithms in reconstructing low-energy signals in high-occupancy environments. Quantization-aware training is performed using qKeras and the implementation demonstrates the effectiveness of a high-level synthesis-based design automation flow, using the `hls4ml` tool, for building design IP for ASICs. The objective encoding can be adapted based on detector conditions and geometry by updating the trained weights. The design has been implemented in an LP CMOS 65 nm process. It occupies a total area of 2.5 mm², consumes 280 mW of power and is optimized to withstand approximately 200 MRad ionizing radiation. The simulated energy consumption per inference is 7 nJ.

Minioral

IEEE Member

Are you a student?

Authors: TRAN, Nhan Viet (Fermi National Accelerator Lab. (US)); DI GUGLIELMO, Giuseppe (Columbia University); BLANCO VALENTIN, Manuel; FAHIM, Farah (Fermilab); GINGU, Cristian (Fermilab); HERWIG, Theodor Christian (Fermi National Accelerator Lab. (US)); HIRSCHAUER, Jim (Fermi National Accelerator Lab. (US)); LLOVIZNA, Miranda; LUO, Yingyi; OGRENCI-MEMIK, Seda

Presenter: TRAN, Nhan Viet (Fermi National Accelerator Lab. (US))

Session Classification: Poster session B-01

Track Classification: Front End Electronics and Fast Digitizers