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Remote Configuration of the ProASIC3 on the ALICE Inner Tracking System Readout Unit

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A Large Ion Collider Experiment (ALICE) is one of the four major experiments conducted by CERN at the Large Hadron Collider (LHC). The ALICE detector is currently undergoing an upgrade for the upcoming Run 3 at the LHC. The new Inner Tracking System (ITS) sub-detector is part of this upgrade. The front-end electronics of ITS is deployed in a radiation environment, and Single Event Upsets (SEUs) in the SRAM-based Xilinx Kintex Ultrascale FPGA of the ITS Readout Unit (RU) is therefore a real concern. To clear SEUs in the configuration memory of this device, a secondary Flash-based Microsemi ProASIC3E (PA3) FPGA is included on the RU. This device configures and continuously scrubs the Xilinx FPGA while data-taking is ongoing, which avoids accumulation of SEUs. There are altogether 192 RUs located in the experimental cavern with limited access. The communication path to the RUs is via the radiation hard Gigabit Transceiver (GBT) system on 100 m long optical links. The PA3 is reachable via the GBT Slow Control Adapter (GBT-SCA) ASIC using a dedicated JTAG bus driving channel.

During the course of Run 3, it is foreseeable that the FPGA design of the PA3 requires upgrades to correct possible issues and add new functionality. It is therefore mandatory that the PA3 itself can be configured remotely, for which a dedicated software tool is needed. This paper presents the design and implementation of the distributed tools to re-configure remotely the PA3 FPGAs.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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