High Throughput Optical Module for Large Size Experiment

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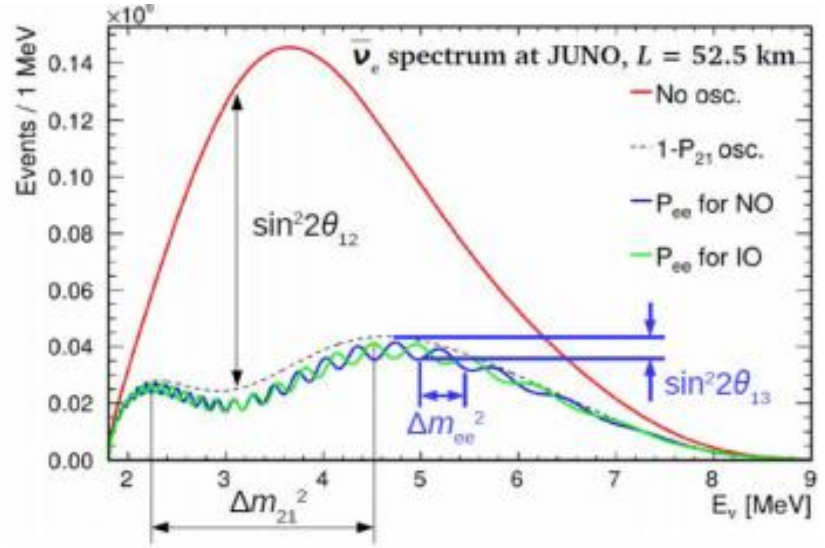
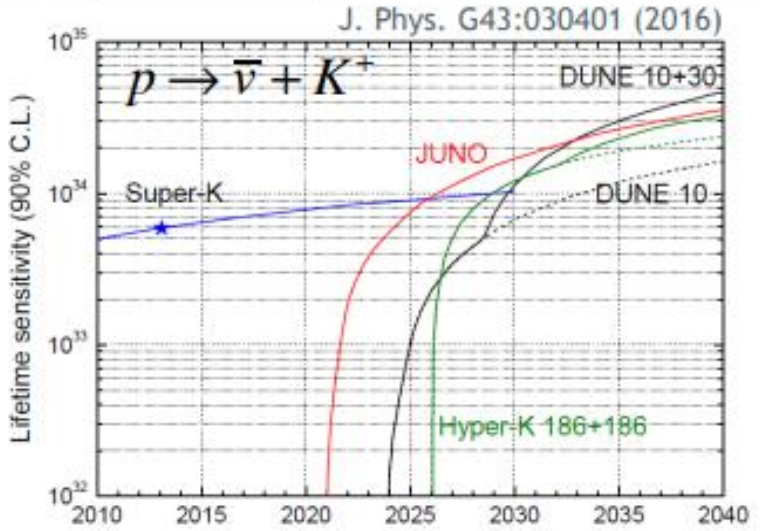
JUNO

The JUNO Experiment

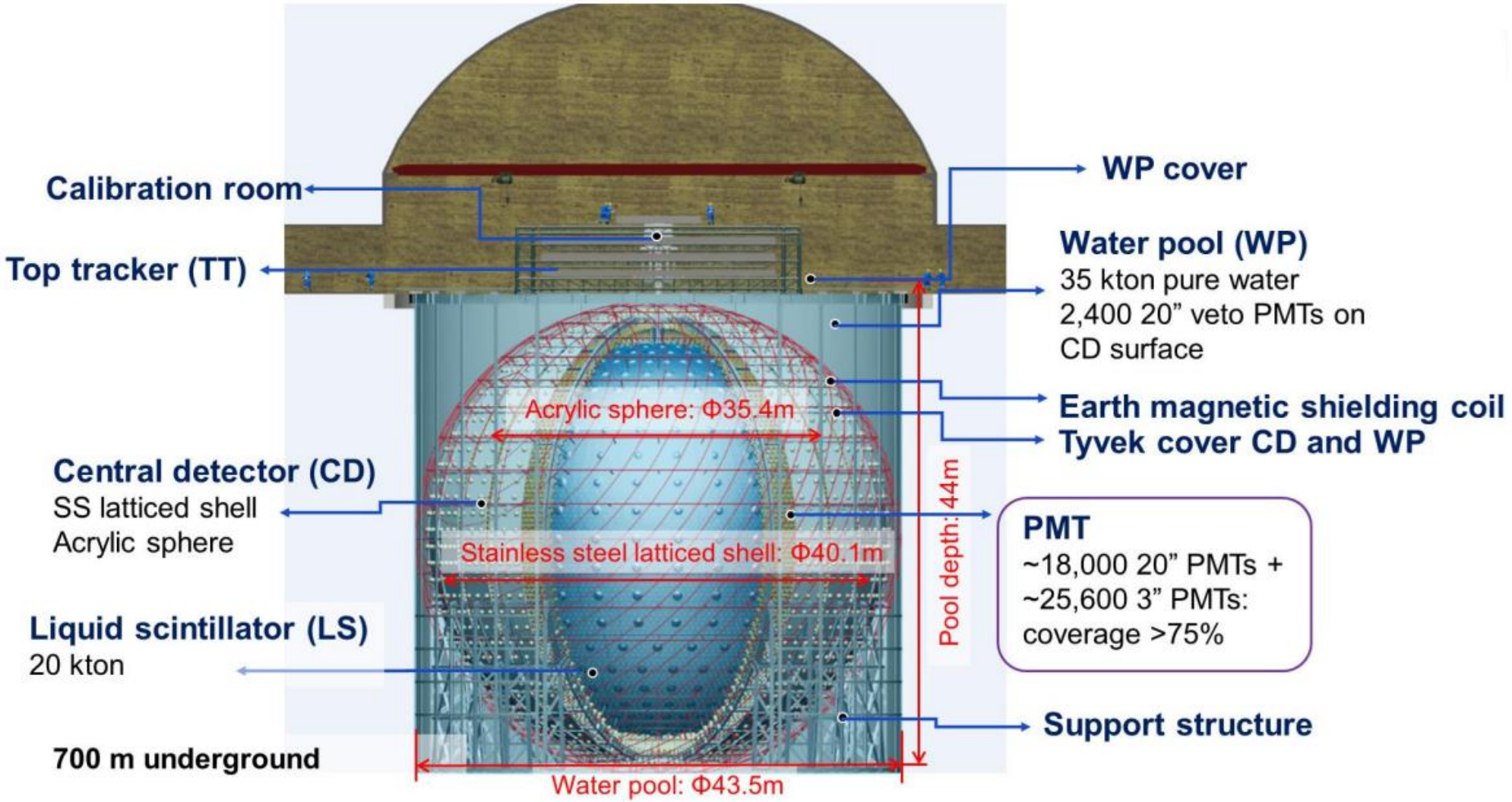
- Determination of the neutrino mass ordering (NMO)
- Measurement of $\sin^2 2\theta_{12}$, Δm^2_{21} and Δm^2_{31} to better than 0.7%
- Supernova neutrinos:
  - 10^4 detected events (5000 IBDs) for SN@10kpc
  - Leading sensitivity to Diffuse Supernova Neutrino Background
- Measurement of geoneutrino flux to ~5% in 10 years
- Search for proton decay and other new physics
- Atmospheric and solar neutrinos



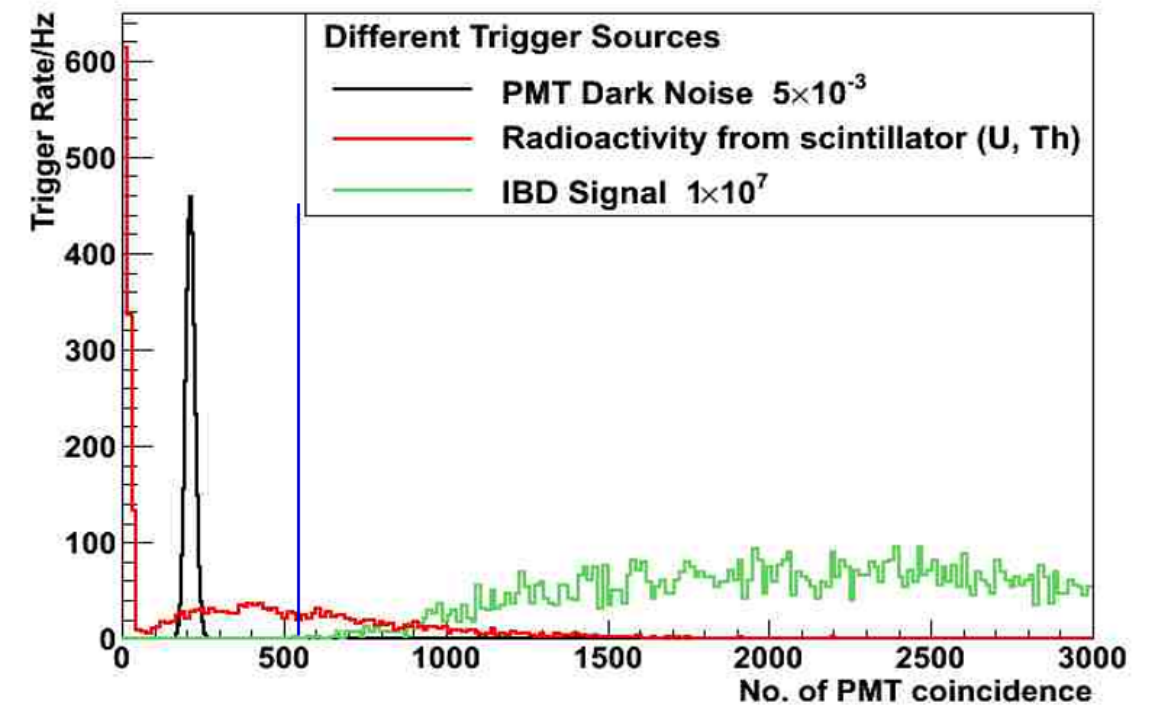


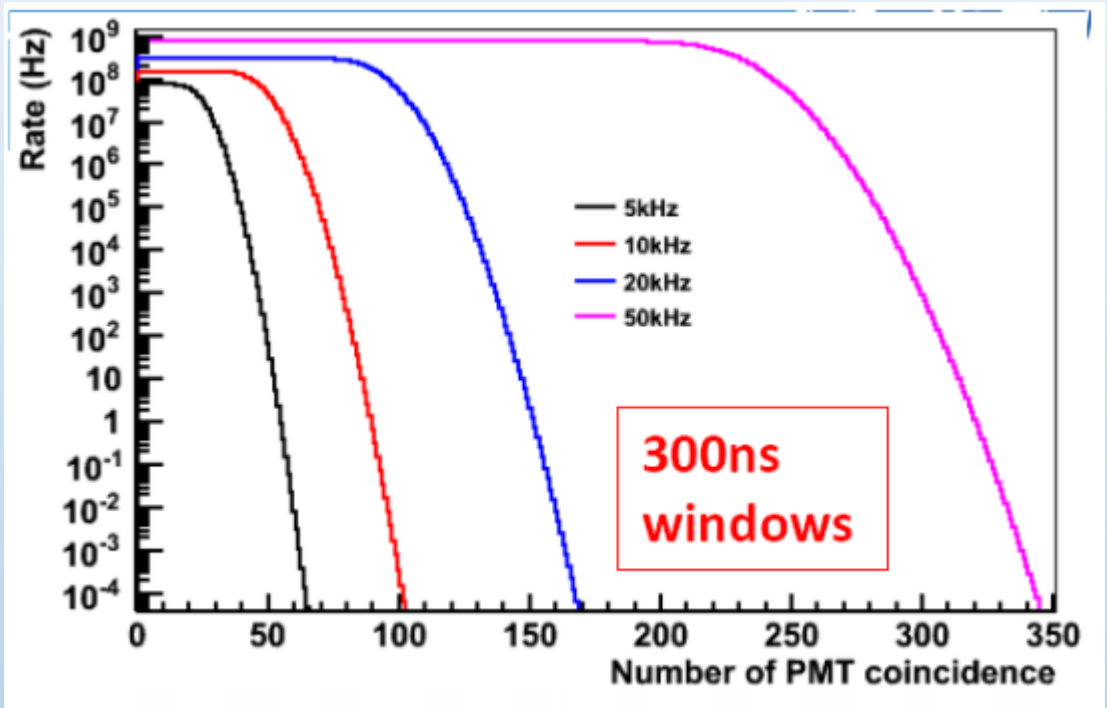
From J. Pedro Ochoa-Ricoux's Nufact 2019

The JUNO Experiment



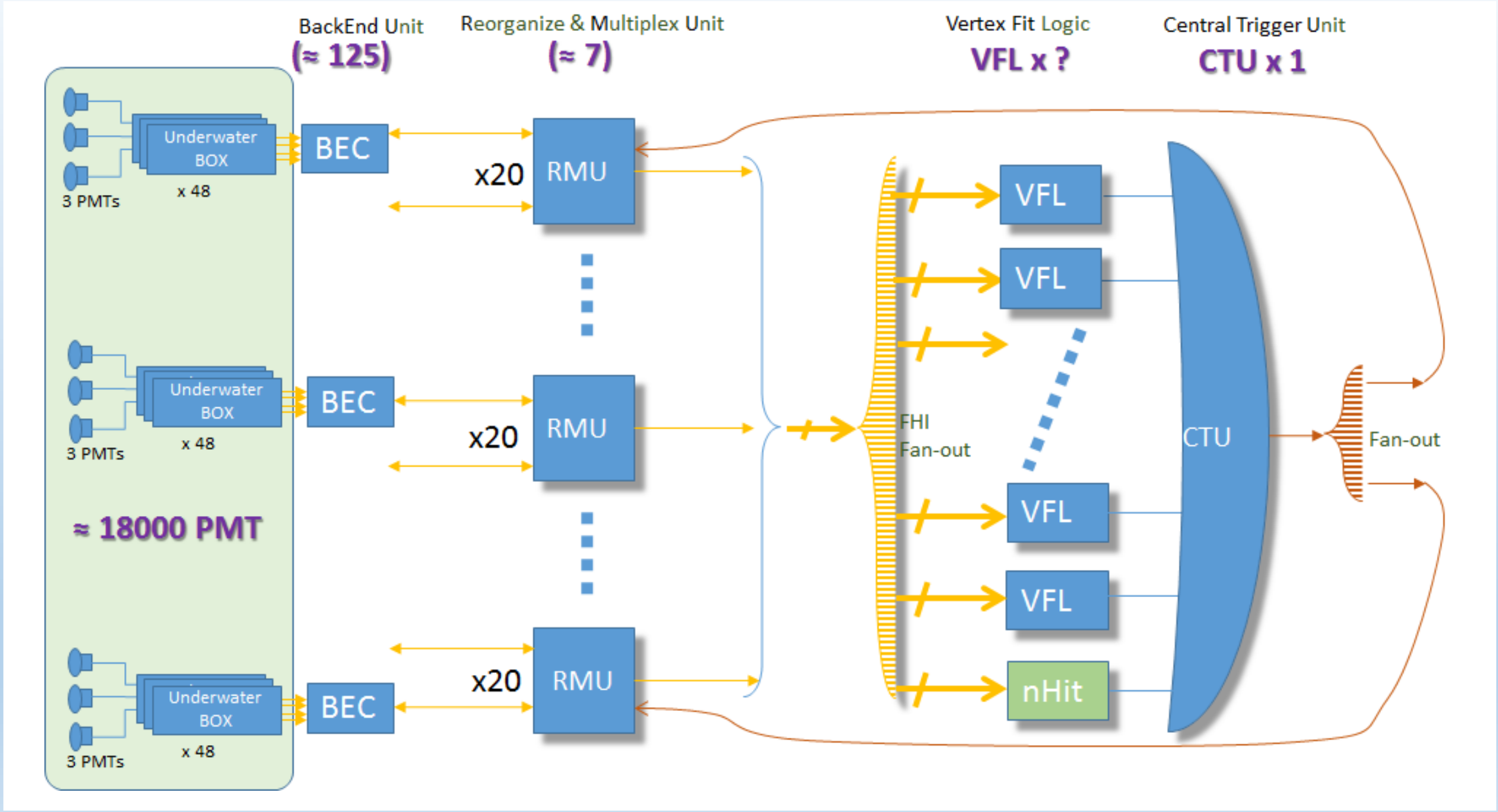
Why we need a trigger?



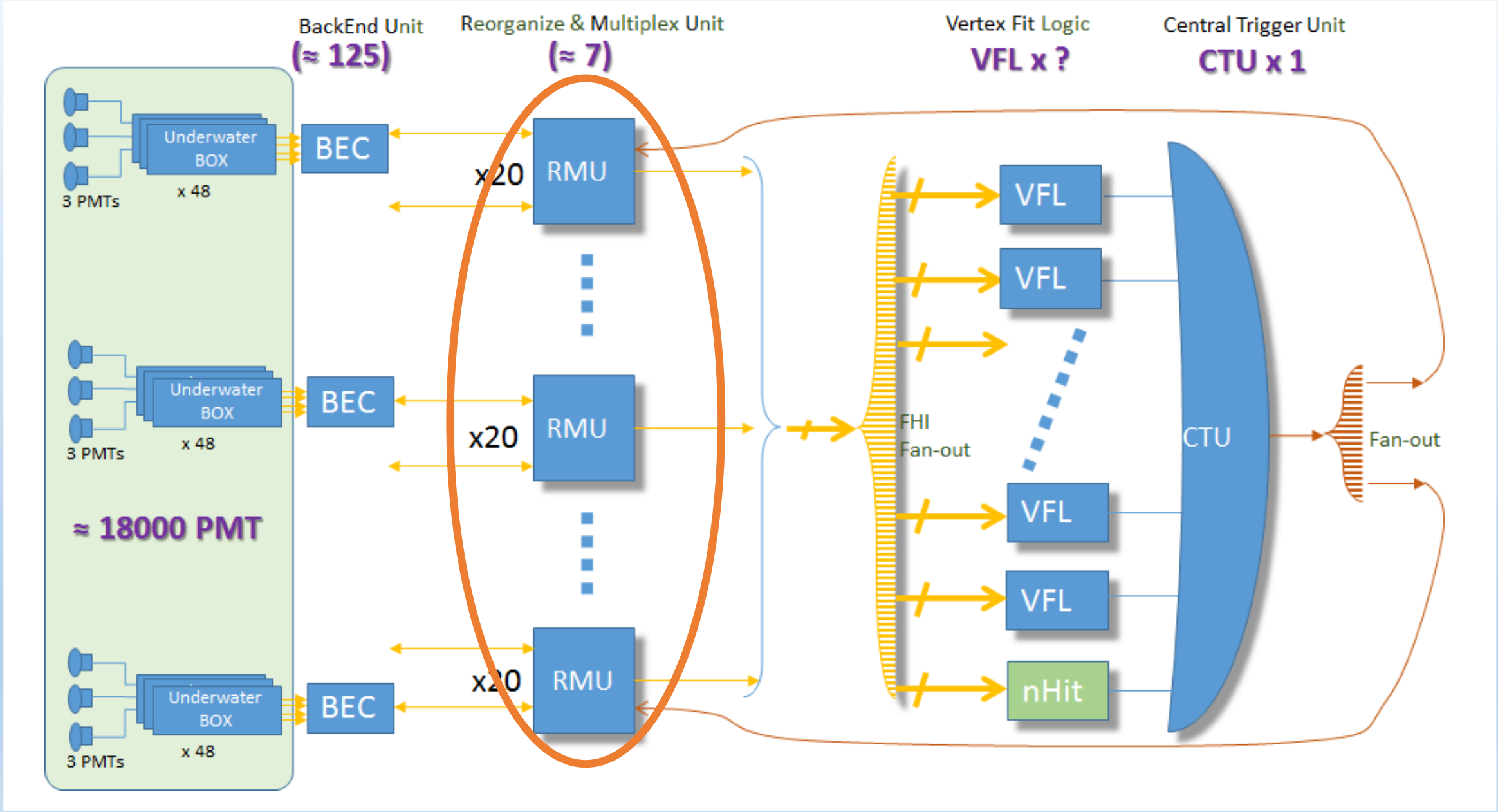


- PMT dark noise is not distinguishable from single p.e. hit
- Dark noise rate can reach 50 kHz from a single PMT
- Number of hits (nHit) can be collected for a multiplicity trigger
- More complex trigger can be deployed with all information collected togheter on a single board

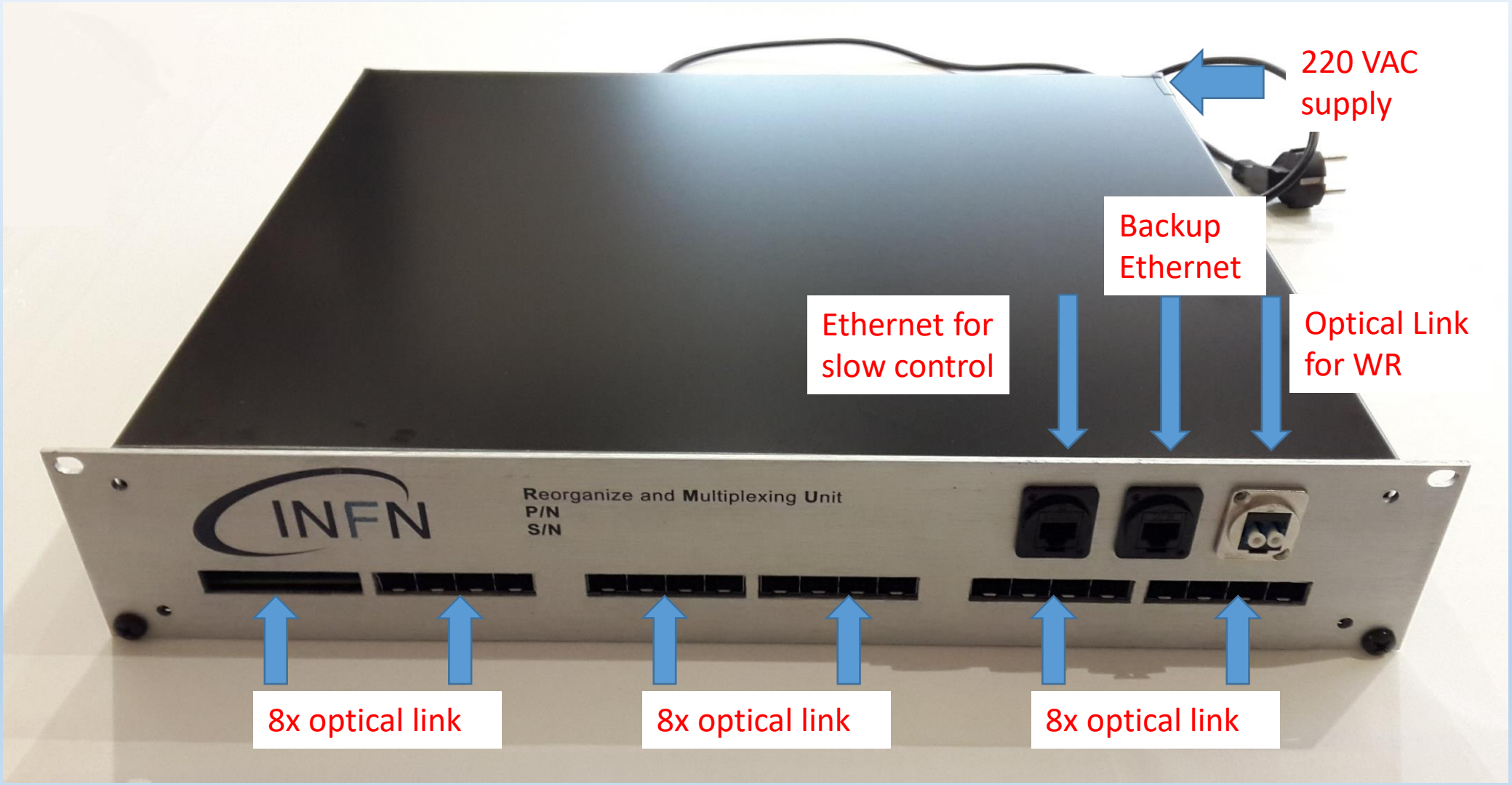
CD trigger block schematic



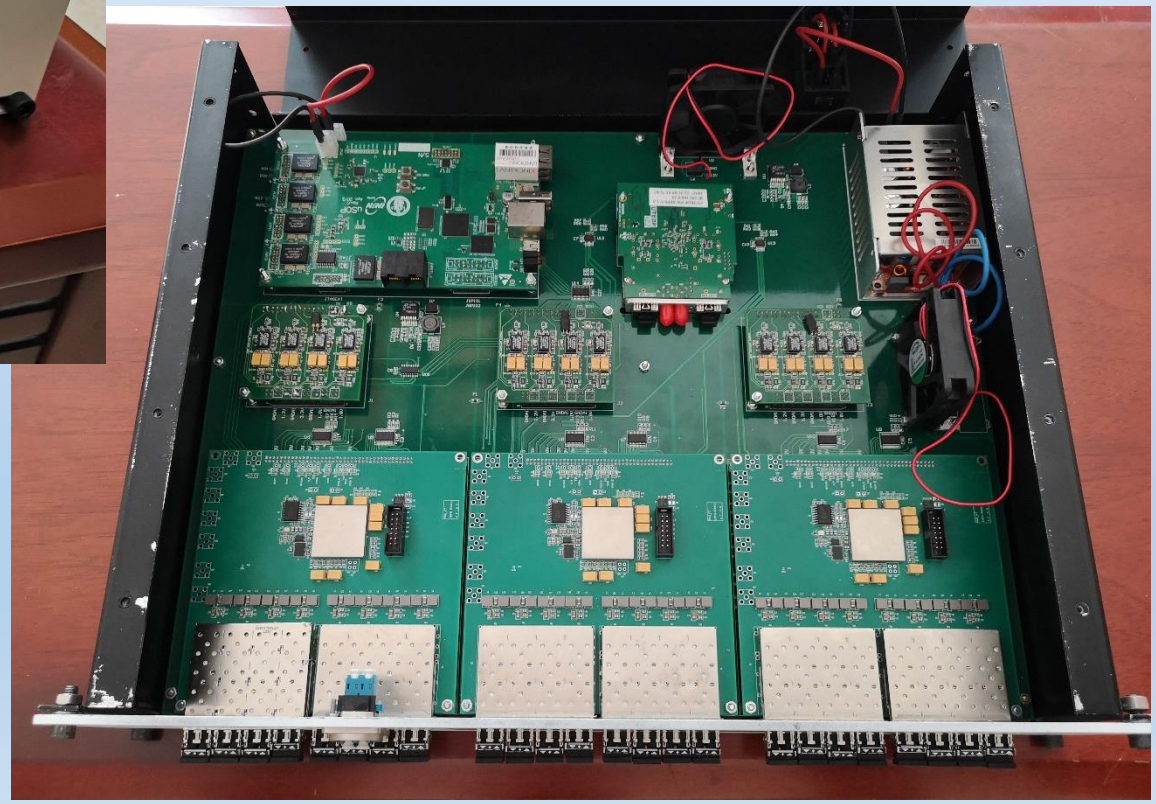
CD trigger block schematic



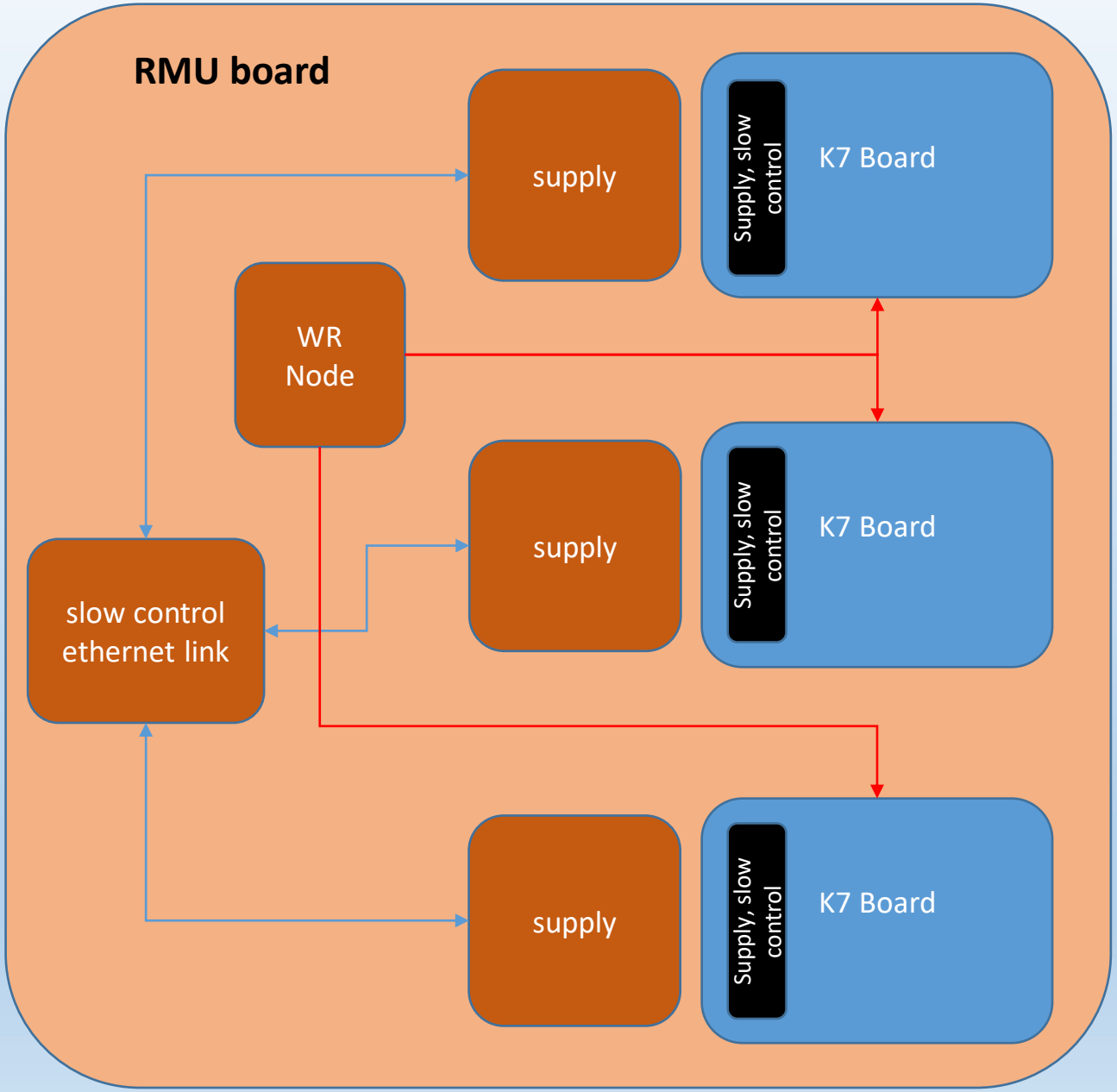
RMU External connection



RMU New Assembly



RMU Reorganize & Multiplexing Unit



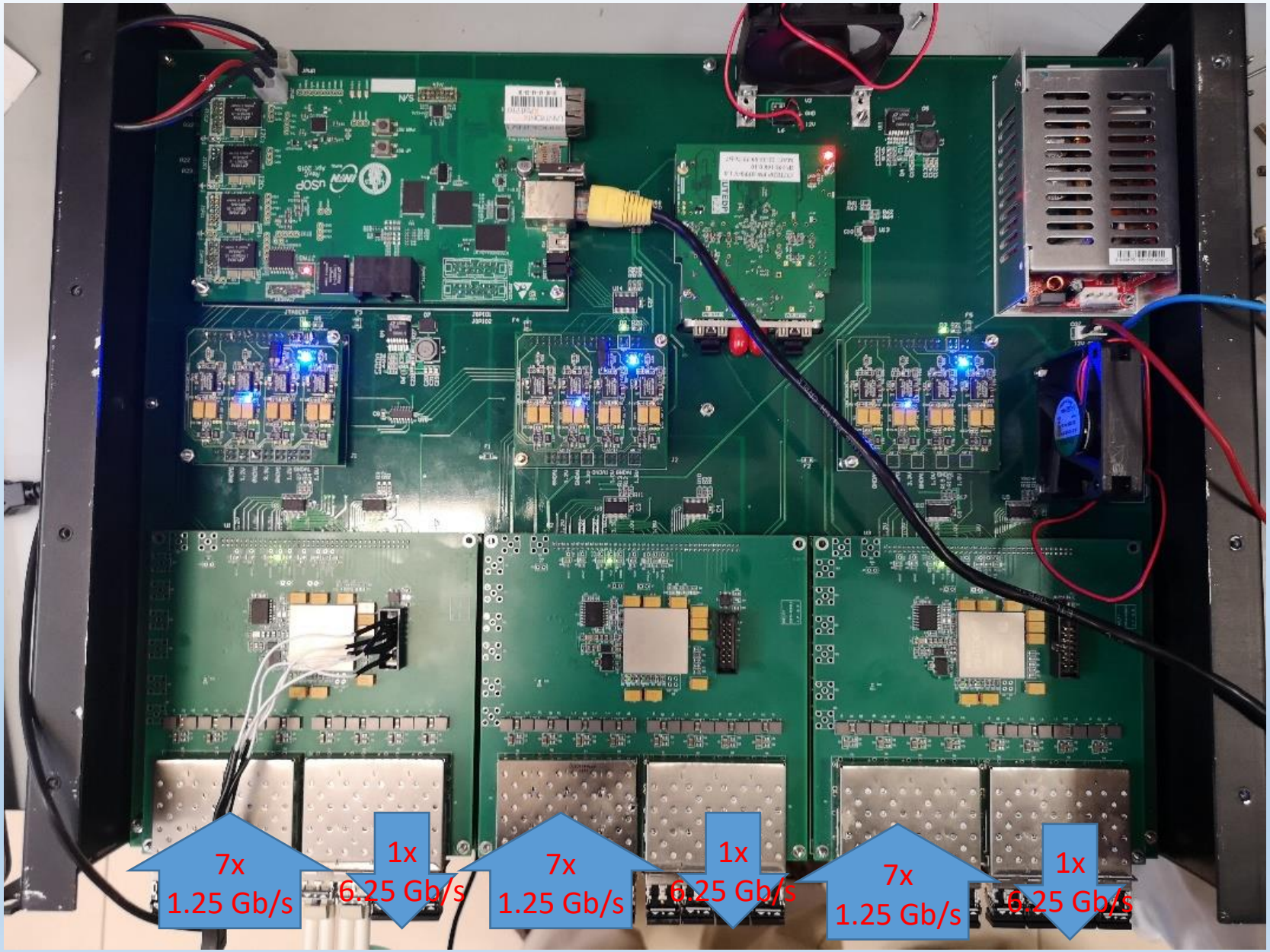
Specification:

125 input link from BEC organized in 7 RM Unit:
21x 1 Gb/s input link each
3x 6.25 Gb/s output link each

Each RMU has 3 separate FPGA board with 7x input link and 1x output link

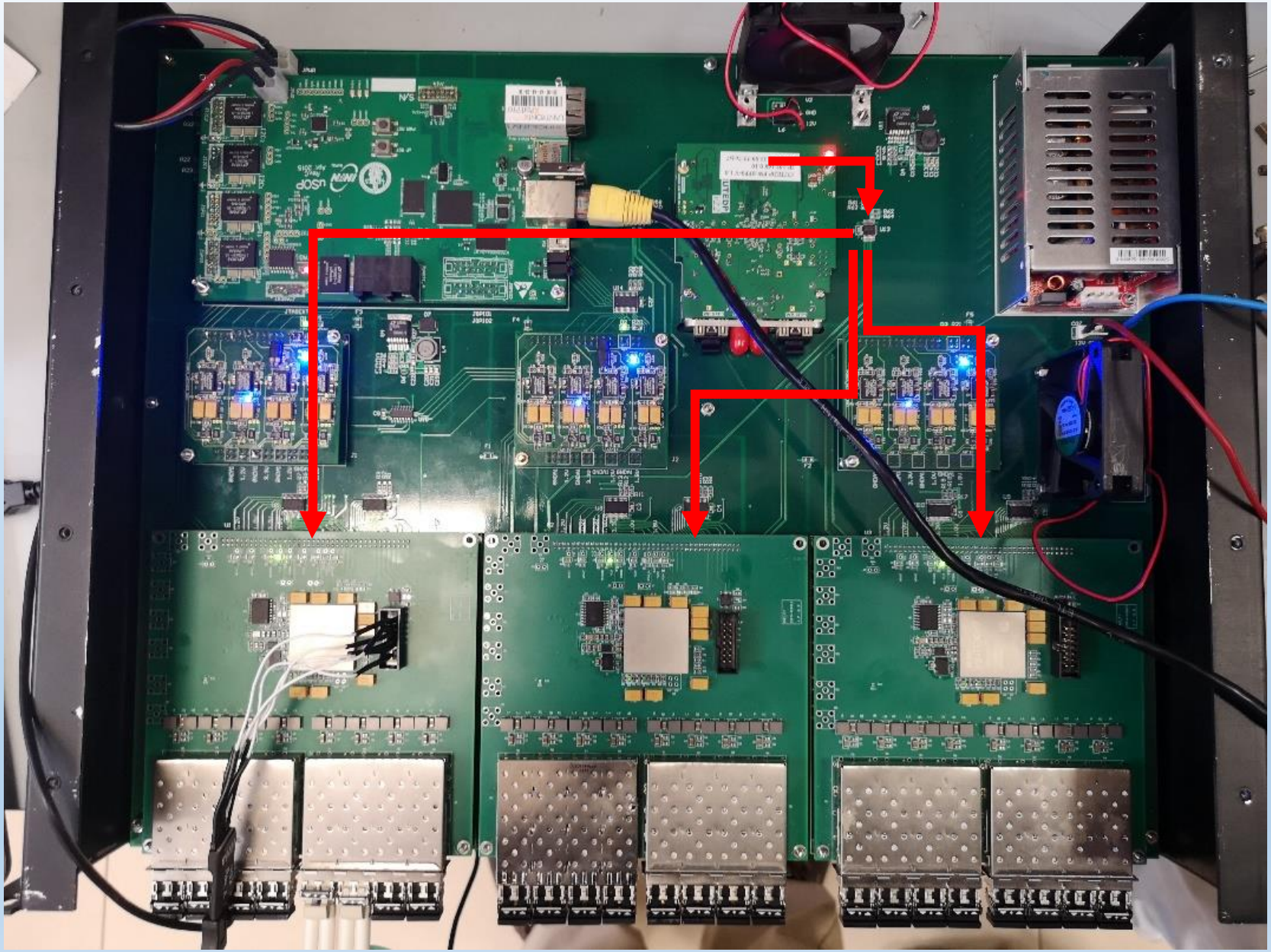
Room for up to 21168 large PMTs.
(taking into account Underwater box (x3) and BEC (x48))

RMU Data Flow



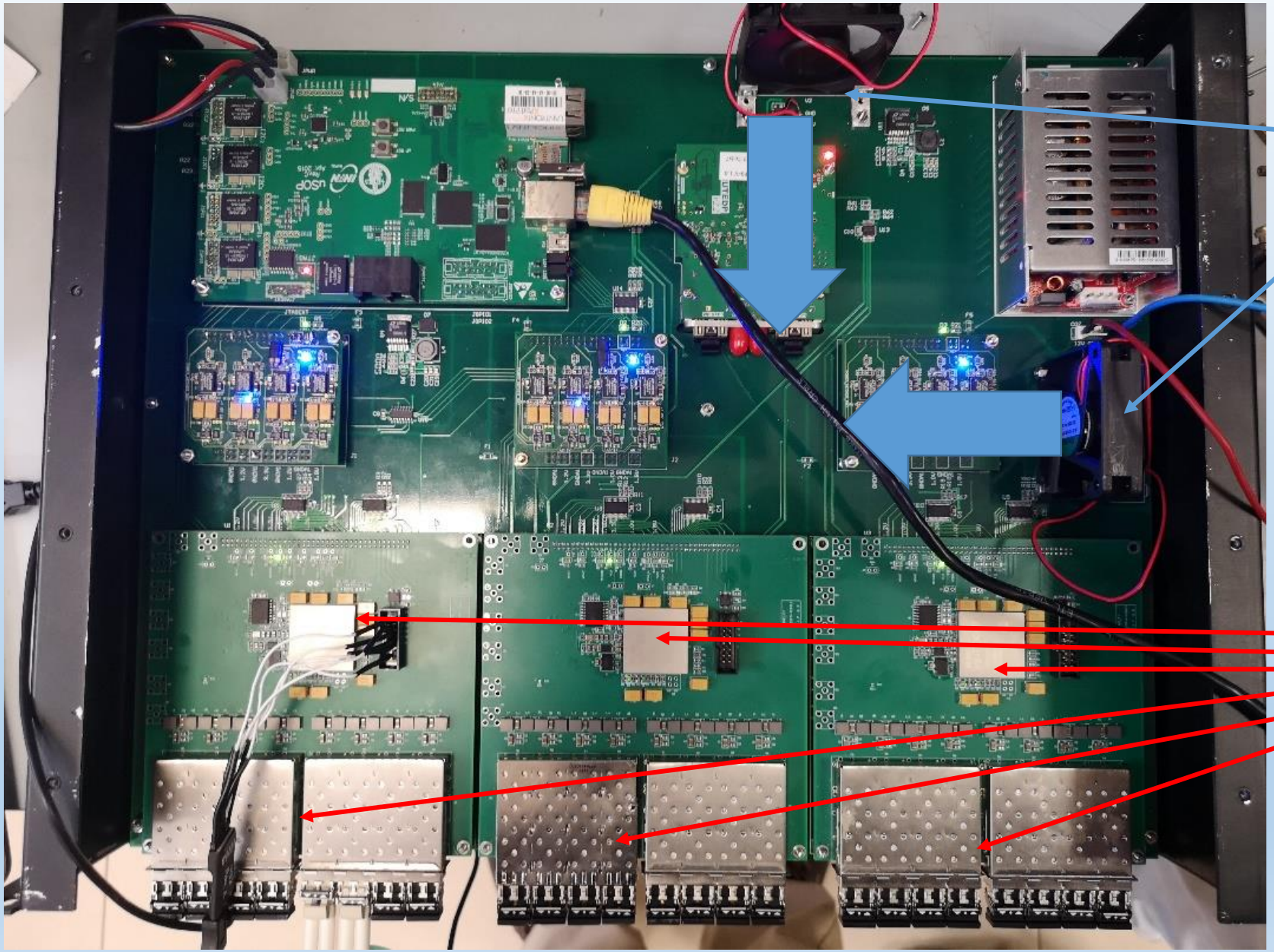
- Each K7 board has 8 in/out optical link tested at 8 Gb/s.
- Production board (V2.0) will be equipped with -2 (instead of current -1) speed grade FPGA (= 10 Gb/s link) => It is possible to avoid data compression.

White Rabbit Clock distribution



- WR clock comes from Cute WR board.
- LVDS clock from WR is distributed by clock fanout IC.

Air Flow

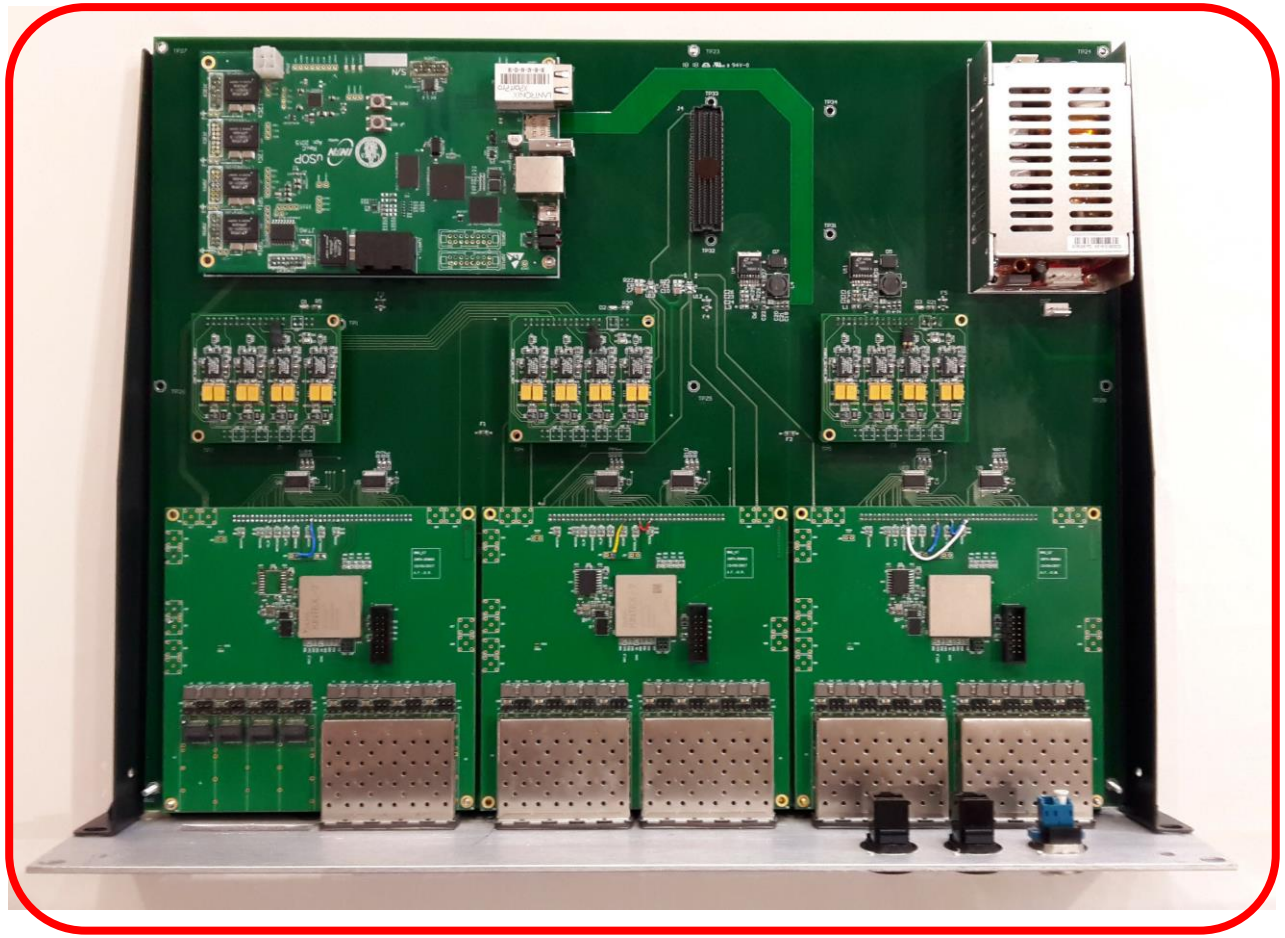


Two fans position

Measured temperature on the FPGAs (open frame) = ***35°***

Hot Spots (FPGAs and transcievers)

RMU Motherboard



Mother Board v2.1

Mainly works as docking for K7, Power and USOP boards.

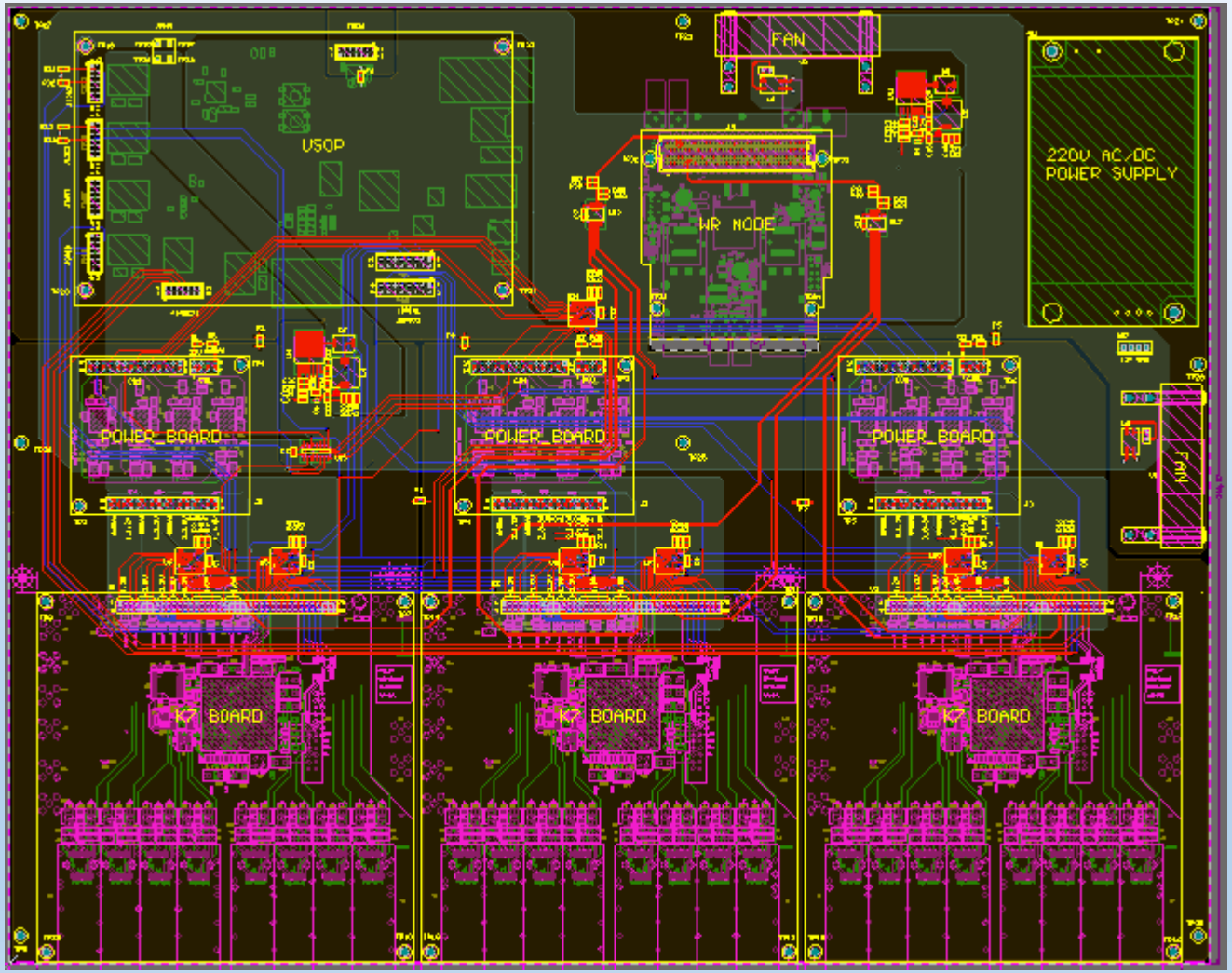
Fit commercial 2U case for 19’’ racks.

Supplies and control signals routing between different boards.

I2C bus allows USOP slow control of the system

V2.1 is equipped with clock fan-out from USOP to allow clock distribution test.

RMU Motherboard

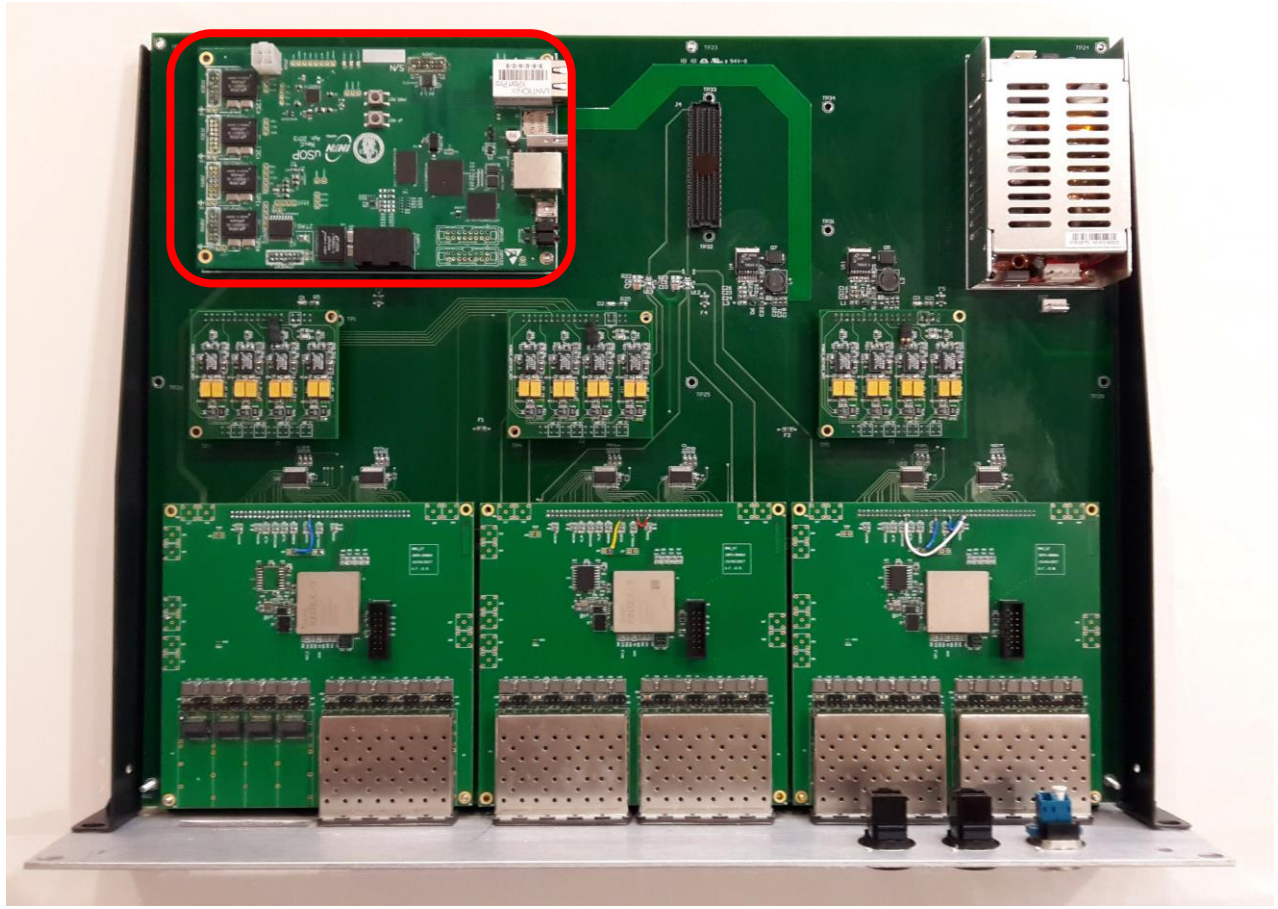


Four layer PCB:

- L1: Top Layer
- L2: Ground Plane
- L3: Power Plane
- L4: Bottom Layer

Host RECOM RAC150-12 PSU for 220V AC / 12V DC conversion (150W output).

RMU status



USOP v2.0

Developed by INFN Roma Tre and INFN Napoli for Belle II experiment.

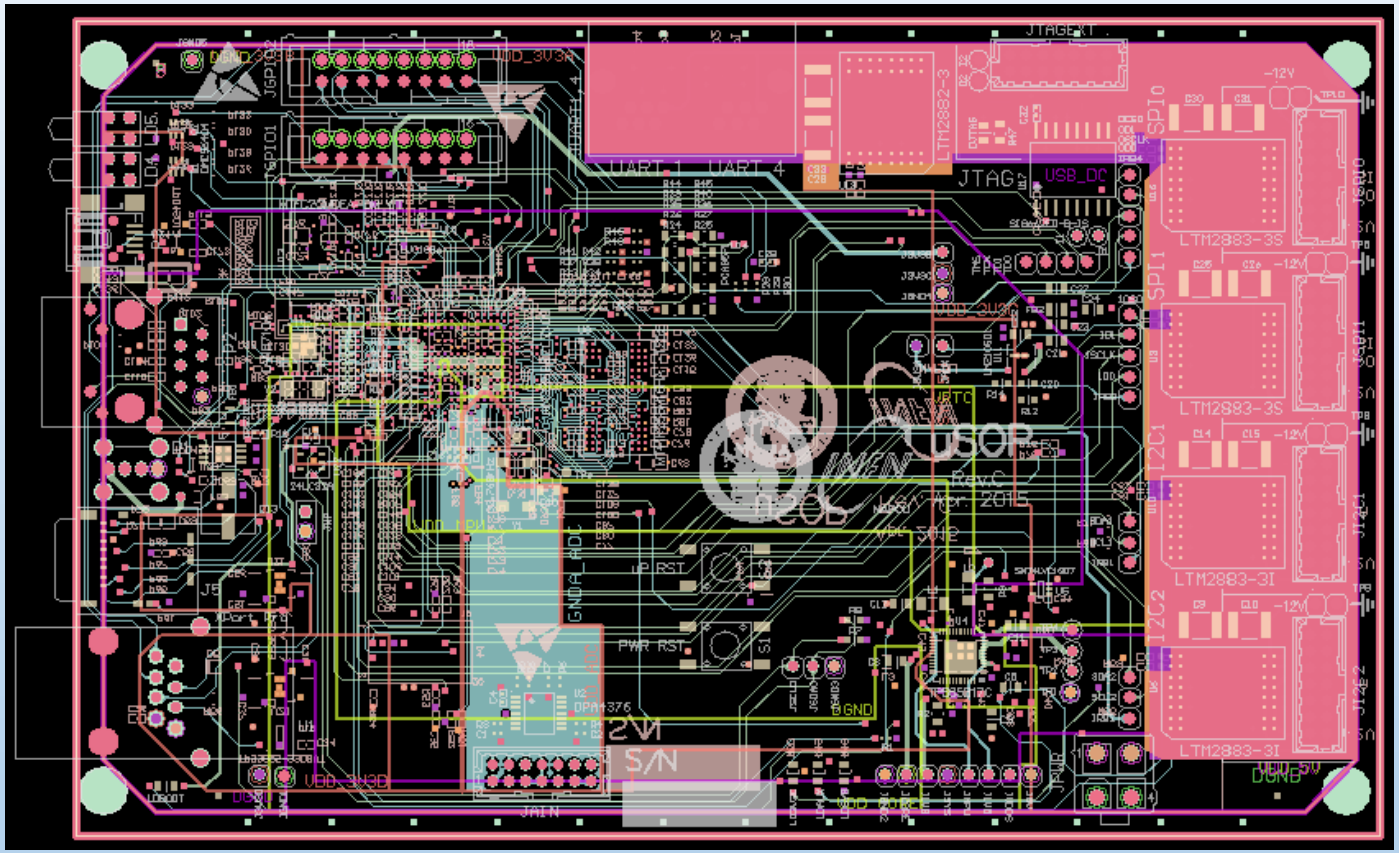
Ten boards on-line at KEKB since 2016 without any failures.

Standard ethernet link for slow control (TCP/IP).

- Power supply monitor (I/V)
- Transciever monitor (RX Sync loss, TX Failure, data average…)
- Temperature monitor

Redundant ethernet link for recovery operation

RMU K7 Board



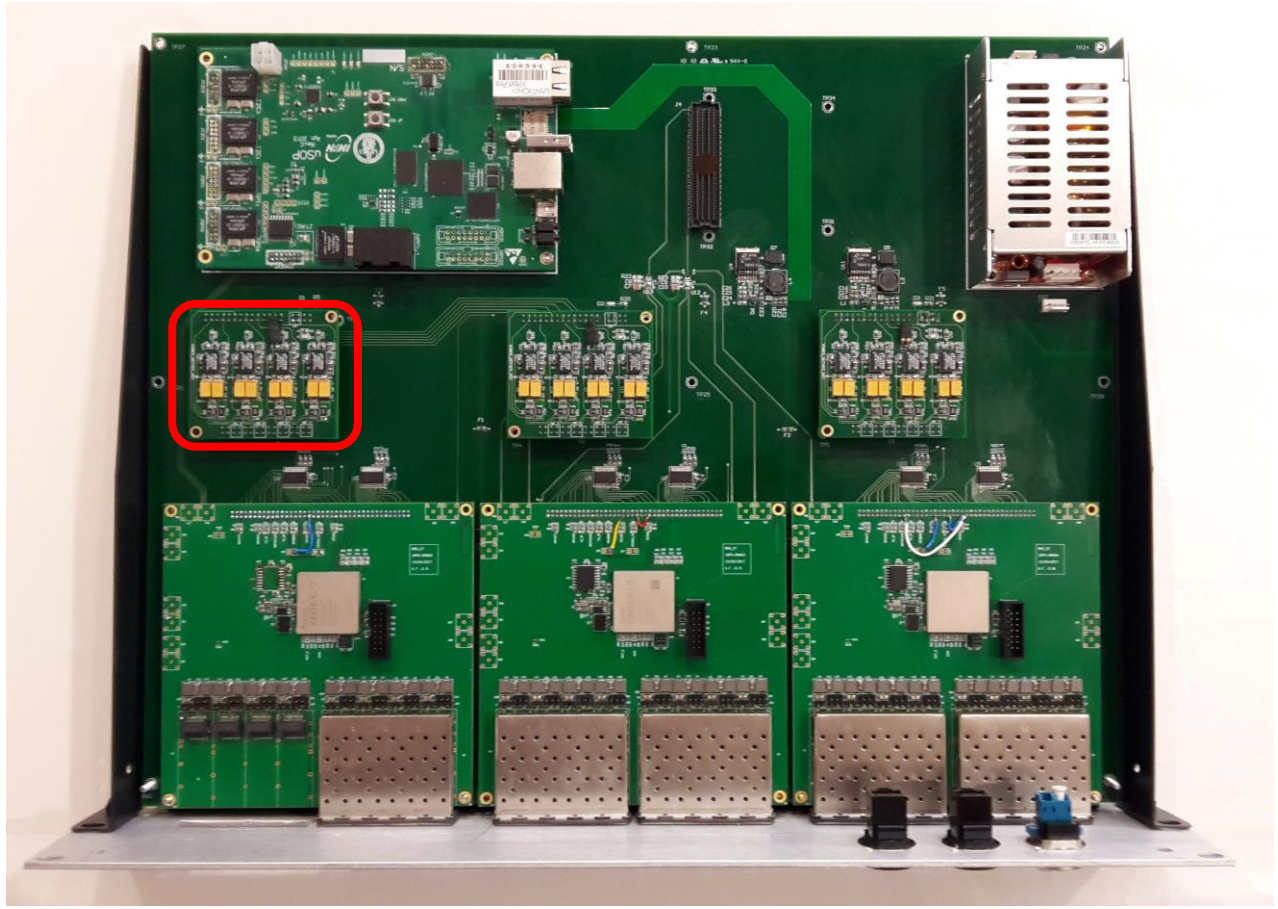
Ten layer PCB:

- L1: Top Layer
- L2: Power Plane
- L3: Signal Layer
- L4: Ground Plane
- L5: Signal Layer
- L6: Power Plane
- L7: Signal Layer
- L8: Ground Plane
- L9: Power Plane
- L10: Bottom Layer

AM3358 Sitara processor (embedded Linux distribution) with two SPI and two I2C interfaces.

JTAG connection to FPGA boards for on-site firmware update *(USOP firmware must be developed to perform this task)*

RMU status

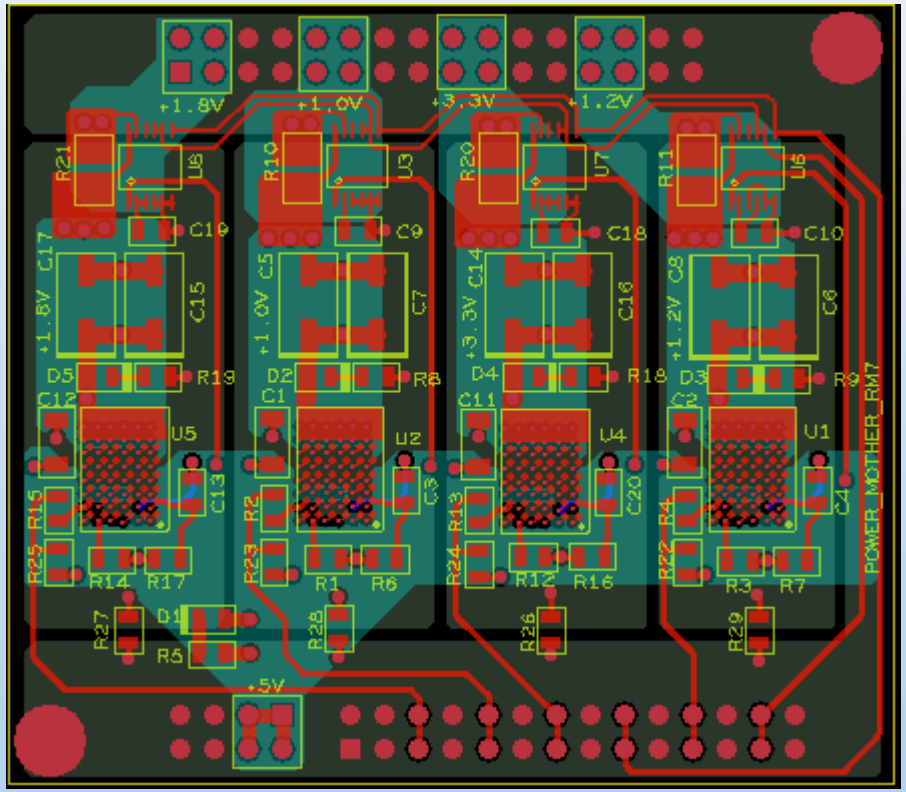


Power Board v2.1

Four DC/DC modules for FPGA supplies: 1.0V, 1.2V, 1.8V, 3.3V.

Each one is followed by a power monitor (I/V measurement).

RMU Power Board



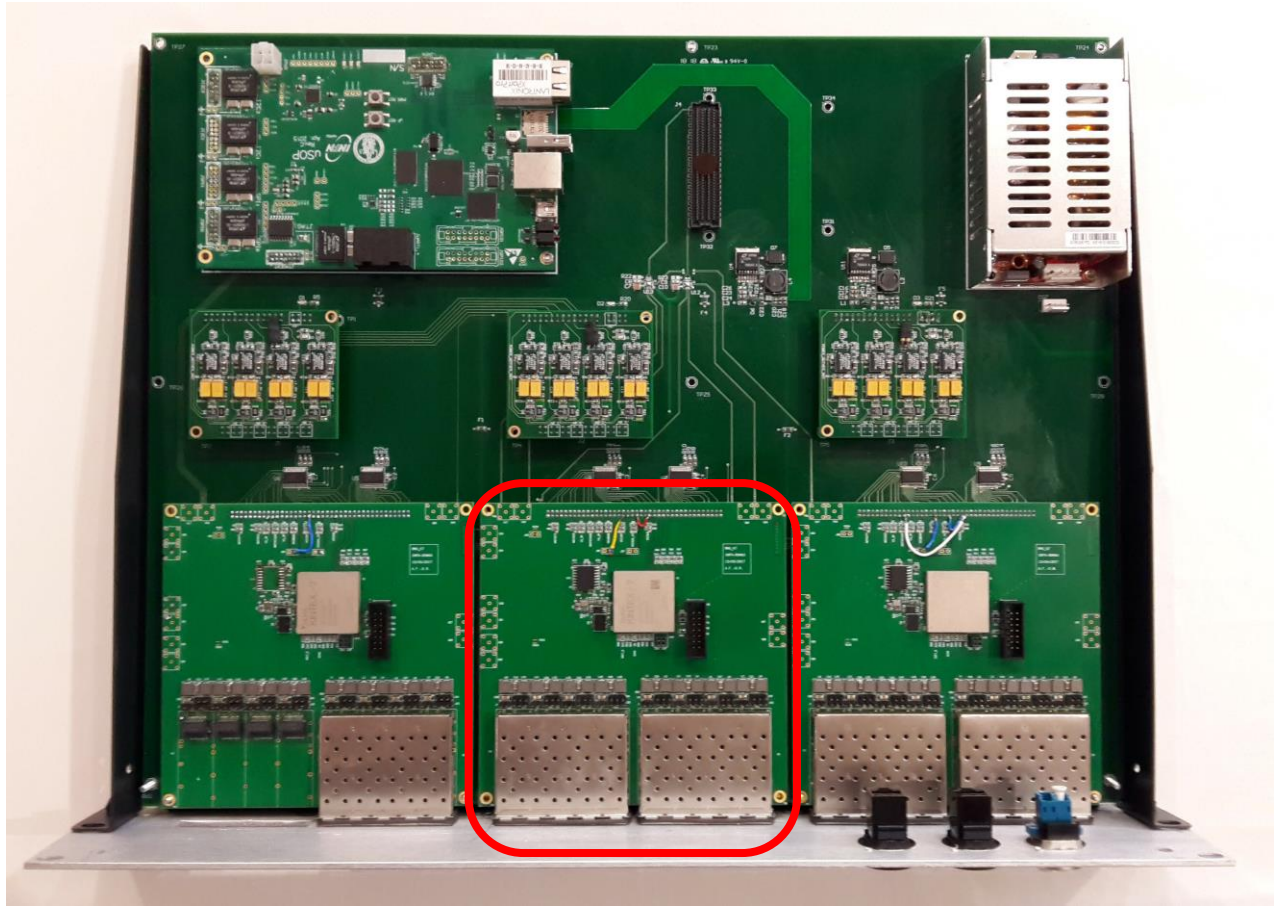
Four layer PCB:

- L1: Top Layer
- L2: Ground Plane
- L3: Power Plane
- L4: Bottom Layer

Four LTM 8053 DC/DC converter (3.5 A each)
Four LTC 2945 I^2C Power Monitor

Rail	Nominal (V)	Measured (V)
VCC_INT	1.0	0.985 ± 0.005
MGTA_VTT	1.2	1.173 ± 0.005
AUX	1.8	1.768 ± 0.005
3V3	3.3	3.221 ± 0.005

RMU status

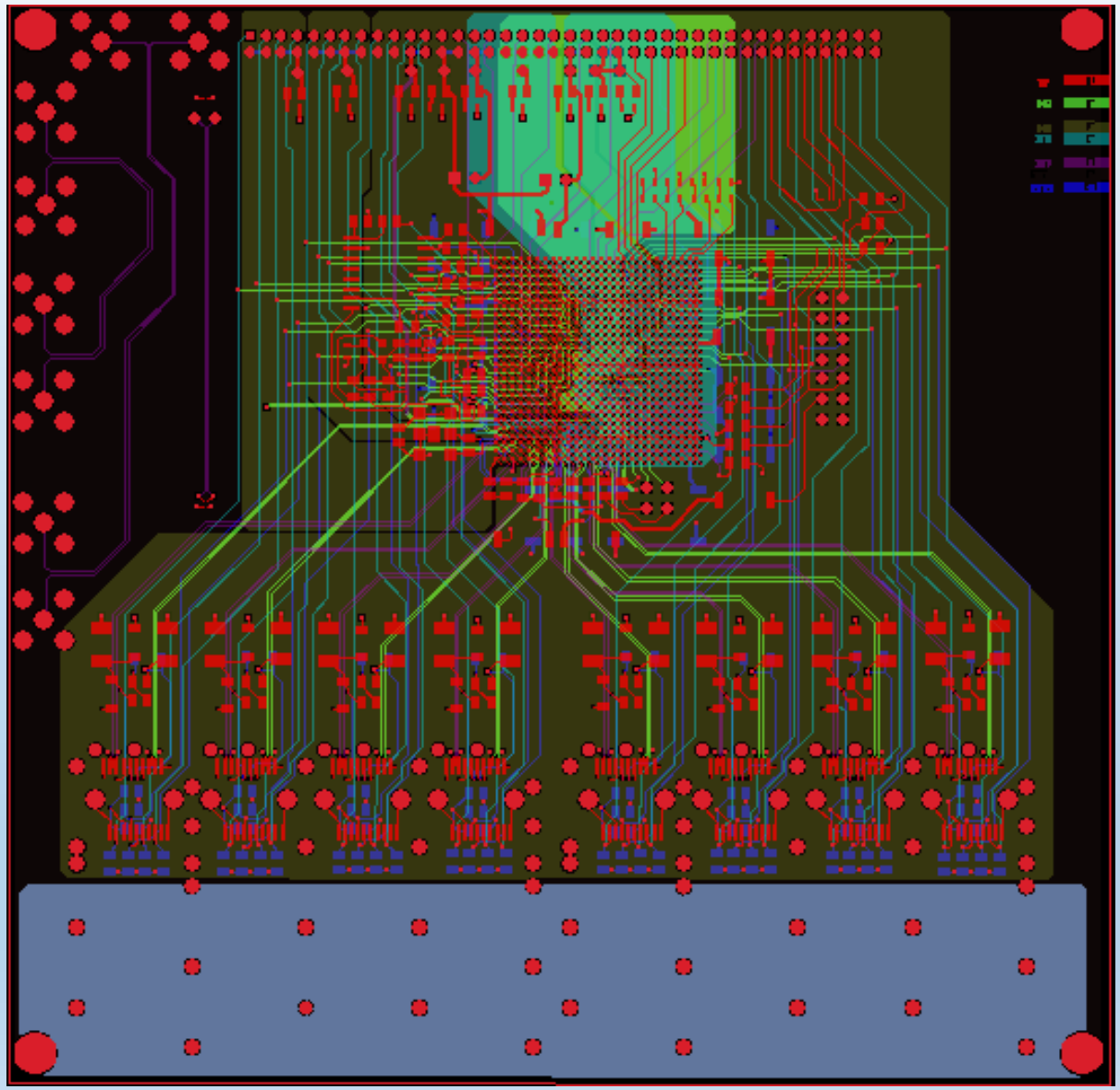


K7 Board v2.0

Based on Kintex 7 FPGA, each board is equipped with 8 optical transceiver.

- No measurable cross talk
- BER test > 10^{16}

RMU K7 Board

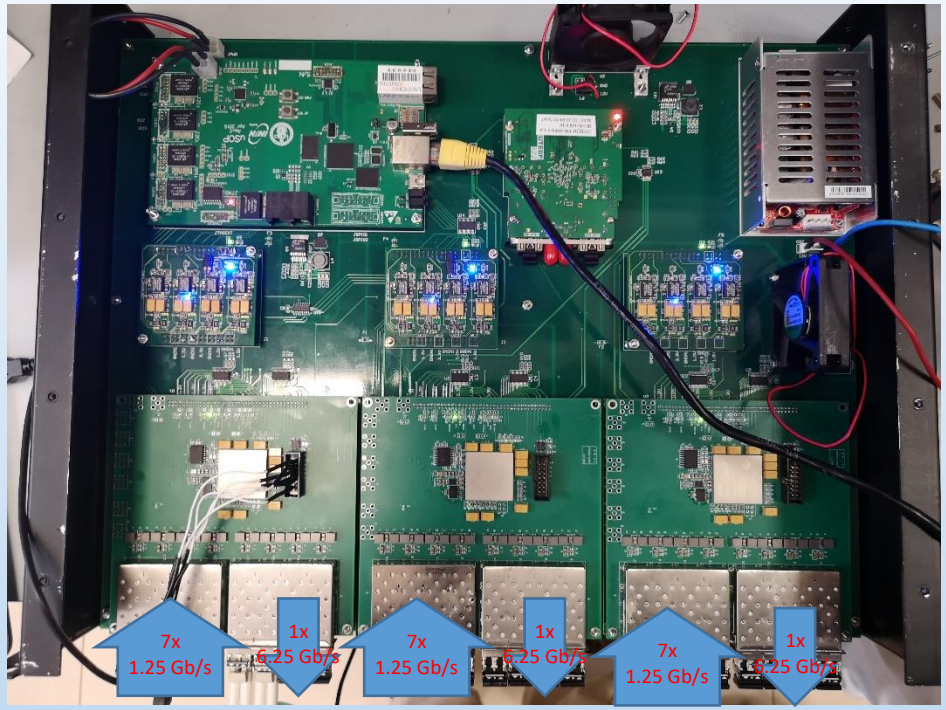


Ten layer PCB:

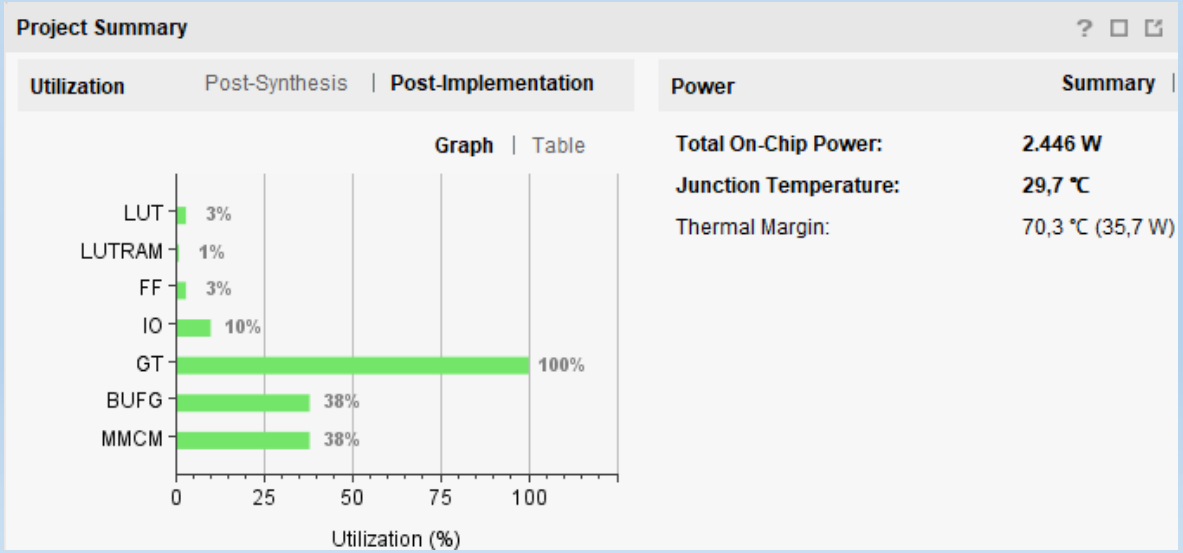
- L1: Top Layer
- L2: Ground Plane
- L3: Signal Layer (TX)
- L4: Ground Layer
- L5: Power Plane
- L6: Powe Plane
- L7: Ground Layer
- L8: Signal Layer (RX)
- L9: Ground Plane
- L10: Bottom Layer

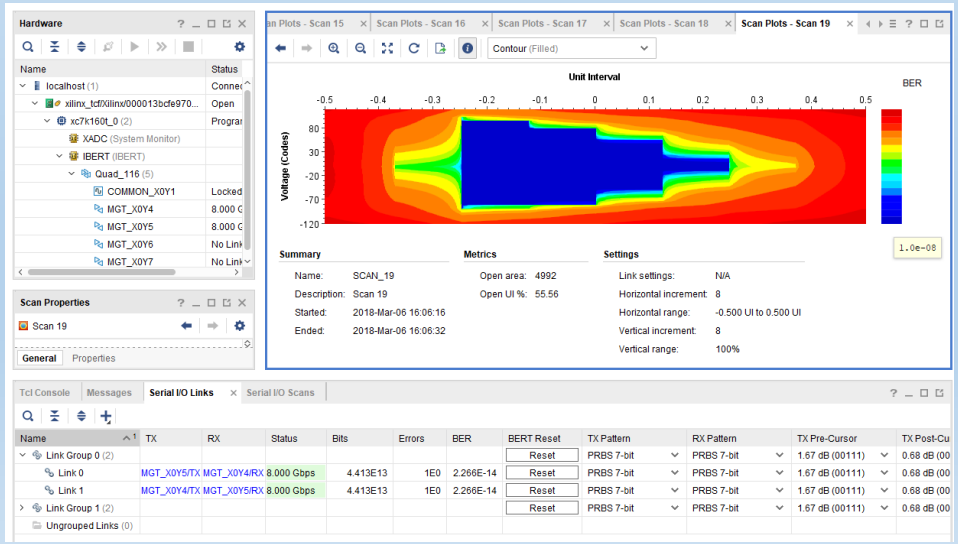
Xilinx K7 XC7K160T-2FFG676 FPGA
Eight Full-duplex SFP+ 10Gb Avago Transceiver

Firmware development

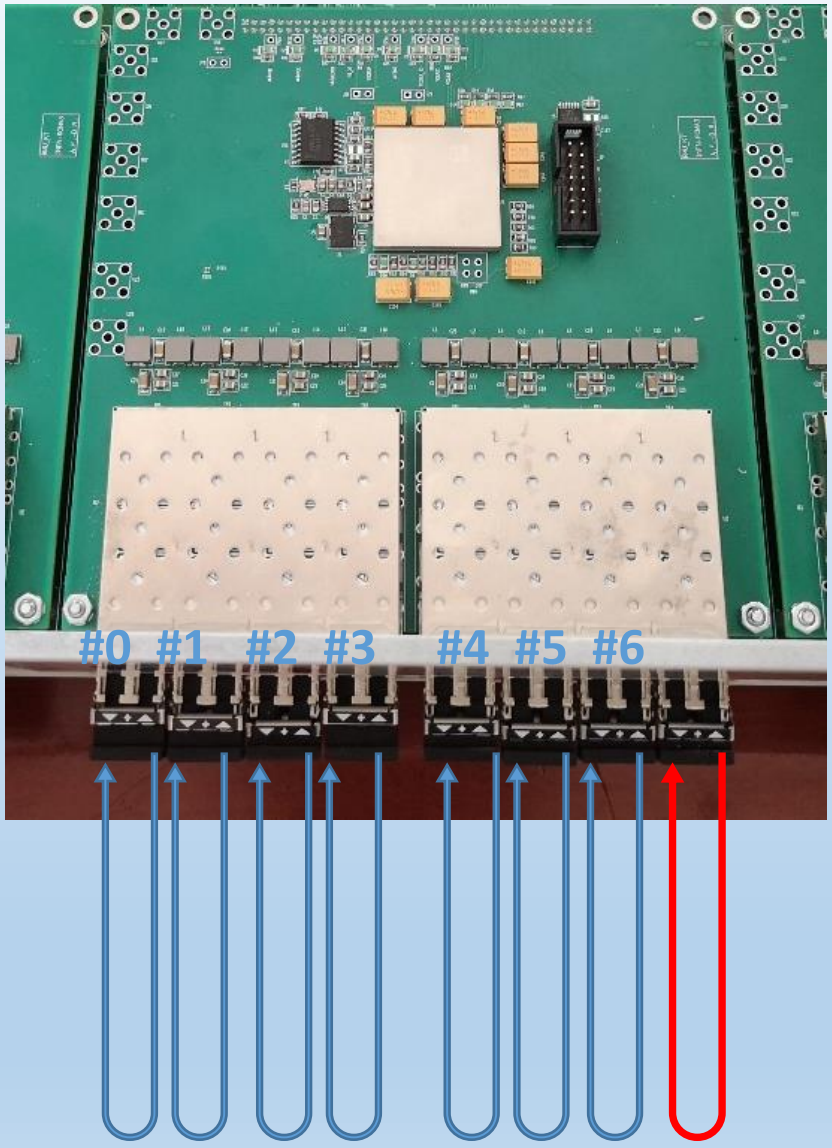


- BER was measure up to 10 Gbit/s with zero errors up to 10^{16} transmitted bit.
- Optical link data transfer is working fine. Data collected from the 7x input link are transmitted by the 1x output without error.
- I^2C interface on FPGA is working fine. Parameters about data trasmitted/received from the transceivers can be read (data average, transceiver status, etc…).
- Data from supply board (voltages, currents) are currently logged by USOP board.





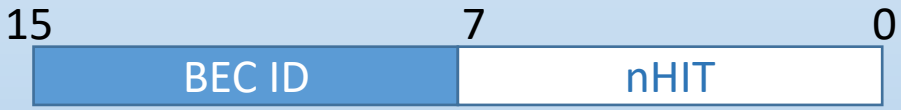
Self-test mode



Loopback configuration

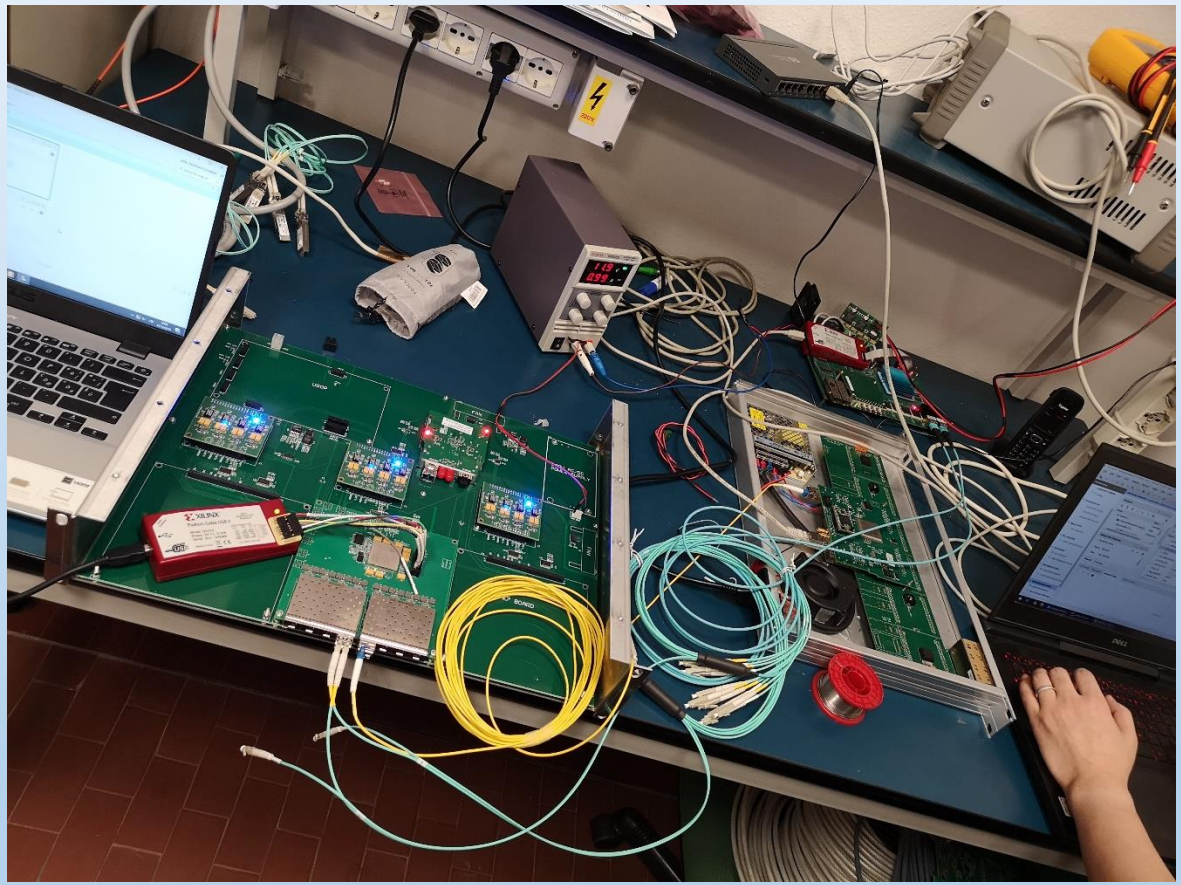
- Self test configuration can be set by I^2C interface on FPGA.
- In self test mode each low speed link transmit a configurable fixed pattern.
- Received data from the high speed link should match with transmitted data from low speed link.

Low speed data frame (1.25 Gbit/s, 8B/10B encoding):



High speed data frame (5 Gbit/s, 8B/10B encoding):

Trigger test



Test setup:

1 BEC

1 RMU 1 CTU

BEC->RMU->CTU link: ok

CTU->RMU->BEC link: ok

RMU link clock from WR Node
(with local oscillator on WR board)

Summary

- RMU module is based on 3 FPGA boards with 8 optical transceiver each. The module is compliant with White Rabbit clock distribution and it is equipped with a dedicated board for slow control on a standard ethernet connection.

- RMU modules were assembled and tested with the full trigger chain, both uplink and downlink are working.

- For the JUNO experiment each FPGA manages 7 link @ 1.25 Gbps and 1 link @ 5 Gbps, several tests were performed with all links at 10 Gbps with BER > 10^{16}.

- Moreover, Kintex7 FPGAs have plenty of computational power to ensure data elaboration.

Thank you!