Firmware and Software Implementation Status of the nBlm and icBlm Systems for ESS Facility

Wojciech JALMUZNA (Lodz University of Technology)
Grzegorz JABLONSKI (Lodz University of Technology)
Rafal KIELBIK (Lodz University of Technology)
Wojciech CICHALEWSKI (Lodz University of Technology)
Andrzej NAPIERALSKI (Lodz University of Technology)
Fabio ALVES (ESS)
Irena DOLENC sKITTELMANN (ESS)

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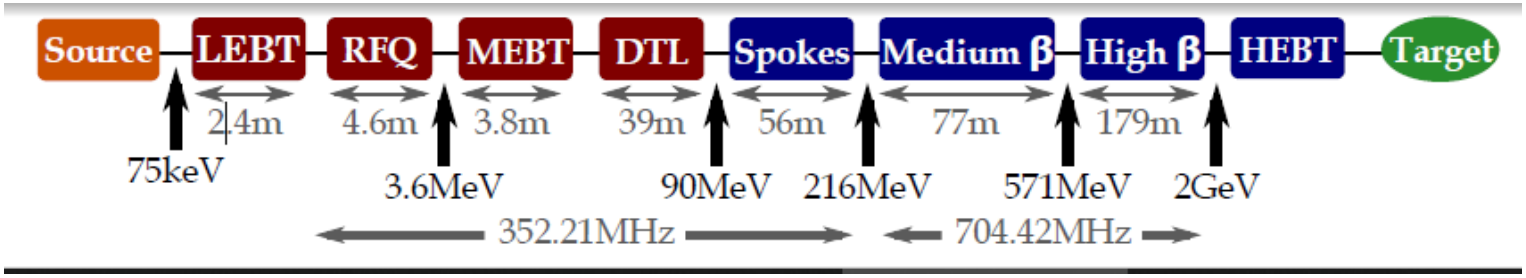
Department of Microelectronics and Computer Science, Lodz University of Technology
http://www.dmcs.p.lodz.pl

BLMs - Introduction

- BLM systems are designed to detect showers of secondary particles produced by lost beam particles interacting with the accelerator equipment.
- BLM systems play an important role in machine protection from beam-induced damage by detecting unacceptably high beam losses and promptly inhibiting beam production. To be effective, they need to react within a few microseconds
- The ESS BLM consist of two types of systems, differing in detector technology.
- The ICBLM system is based on 266 ionisation chambers as detectors, located almost exclusively throughout the SC parts of the linac. They operate in current mode.
- The nBLM system consists of 82 neutron detectors, specially designed to primarily cover the lower energy part of the ESS linac.
- They operate in pulse mode.

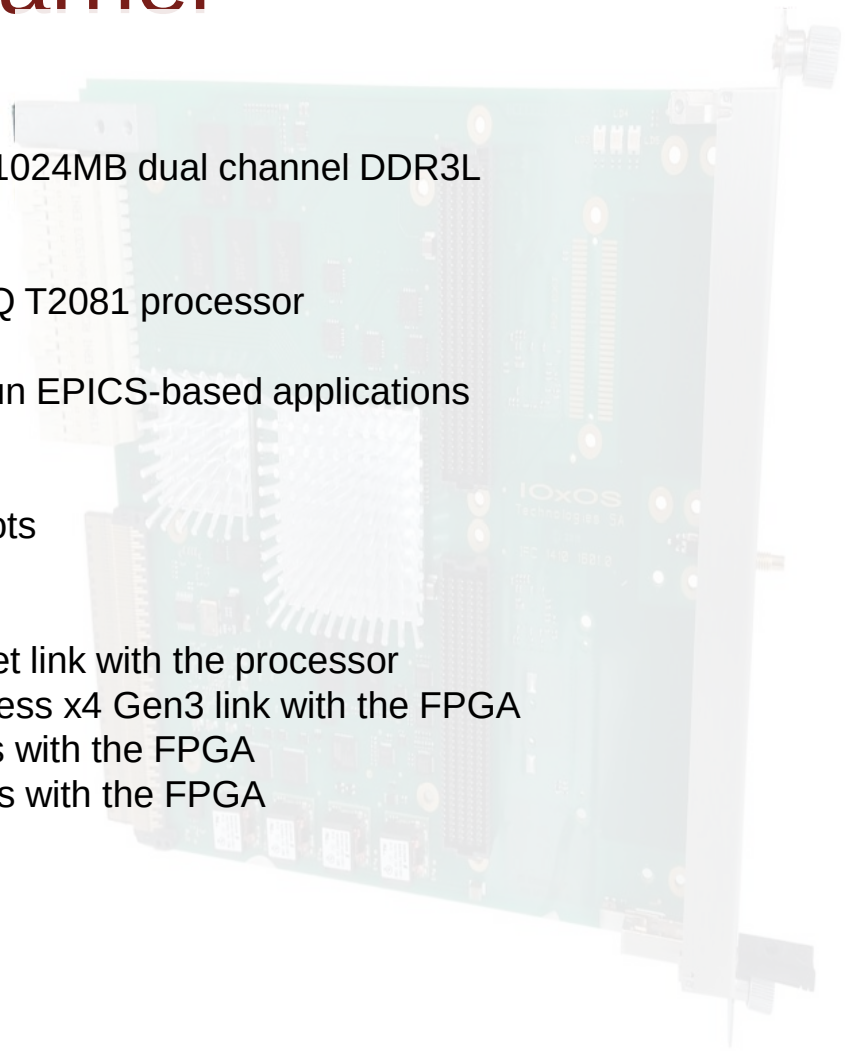


BLM hardware platform uTCA

Infrastructure
- Chassis
- MCH – management unit
- CPU – processing unit
- Power Modules
- Cooling units

AMC cards
- EVR – event receiver
- FMC carriers

BLM hardware platform
IFC 1410 FMC Carrier



FPGA Processing Unit
- Xilinx Kintex UltraScale KU040 FPGA+1024MB dual channel DDR3L

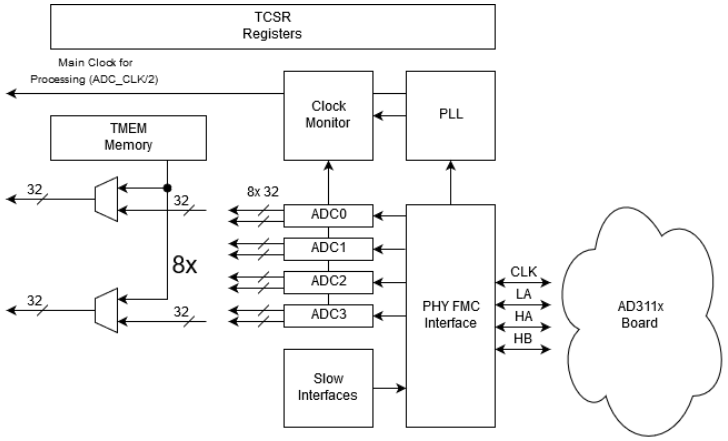
Processor Unit
- High-performance Freescale/NXP QorIQ T2081 processor
- On-board 2GB DDR3L 1866 SDRAM
- Powered by U-Boot/Linux and able to run EPICS-based applications

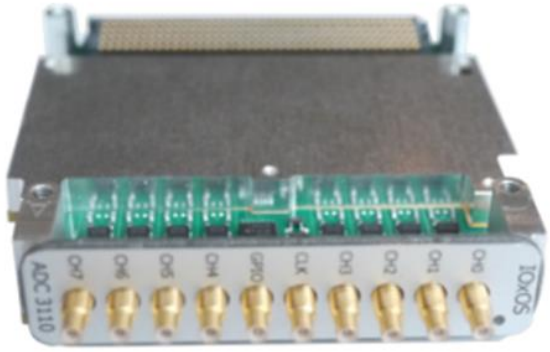
FMC Interfaces
- Dual HPC VITA-57.1-compliant FMC slots

AMC Interface
- Port 0: AMC.2-compliant gigabit Ethernet link with the processor
- Ports 4 to 7: AMC.1-compliant PCI express x4 Gen3 link with the FPGA
- Ports 12 to 15: point-to-point LVDS links with the FPGA
- Ports 17 to 20: shared bus M-LVDS links with the FPGA

nBLM hardware platform AD3111

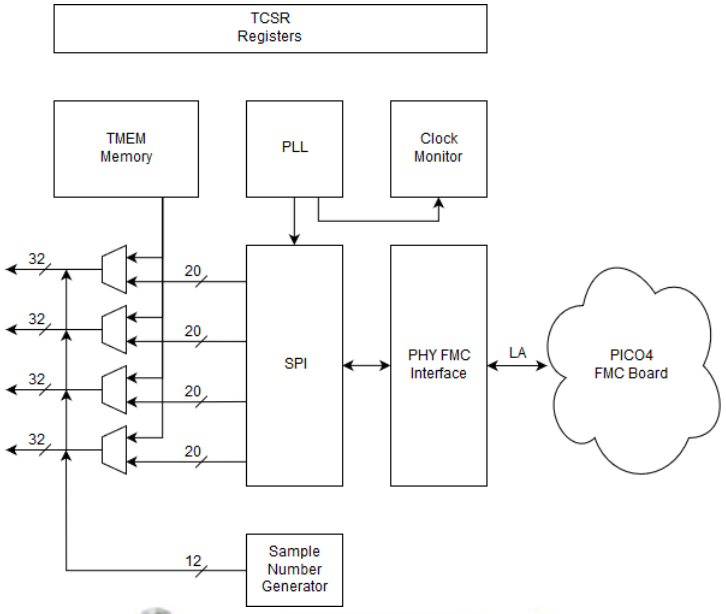
- Eight (8) channels 16-bit 250Msps ADC
- Clock distribution
  - TI LMK4906 (dual PLL)
  - On-board ultra-low noise oscillator
  - External SSMC Clock reference

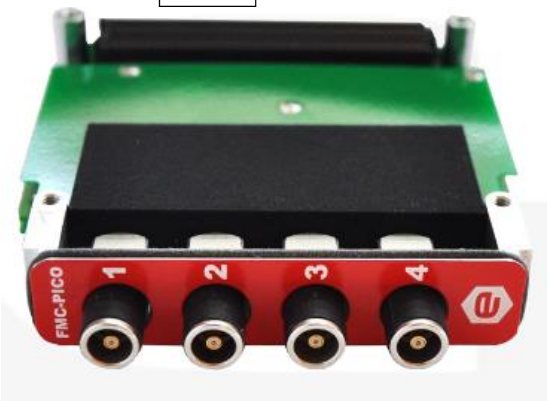




icBLM hardware platform PICO 4

- High Resolution multi-channel current measurements up to ±10 mA (different versions available)
- 4 Current-Input Channels - Bipolar
- 1 MSPS simultaneous and independent sampling
- 20-bit Resolution
- Floating up to 300 V





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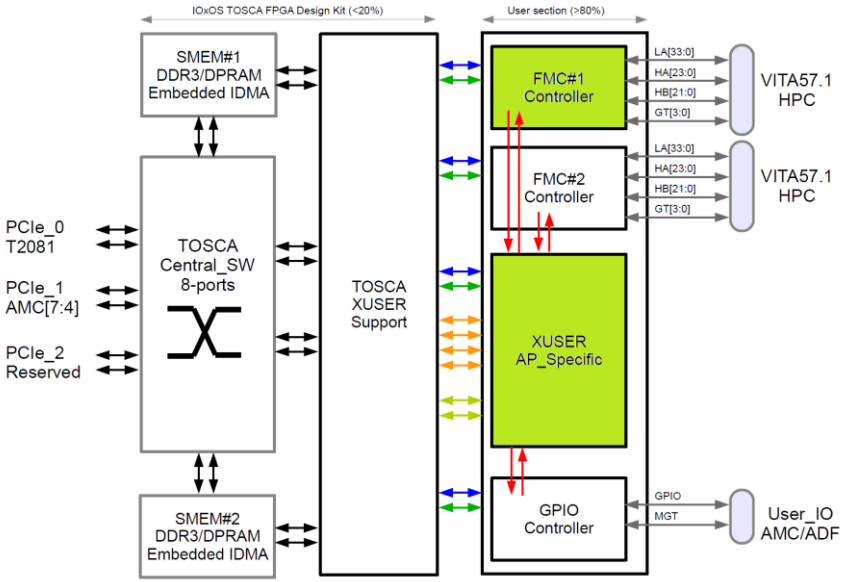
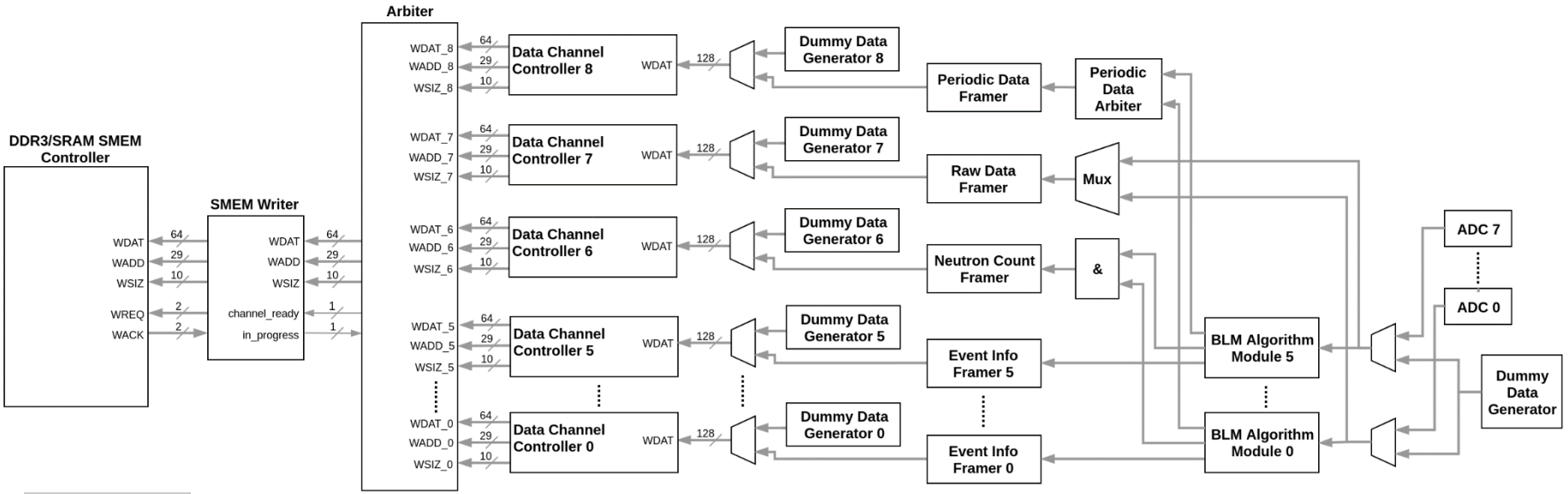
Hardware-software interface

- Using circular buffers in DRAM to stream data to CPU
- Using register interface for control and algorithm parameters
- Both DDR3 banks (currently) via dedicated interface @275MHz, 1900 MB/s bandwidth



Data transmission protocol layers

- Circular buffers – stream of unstructured data
- Data frames – timestamping and integrity check
- Periodic data – content-specific header



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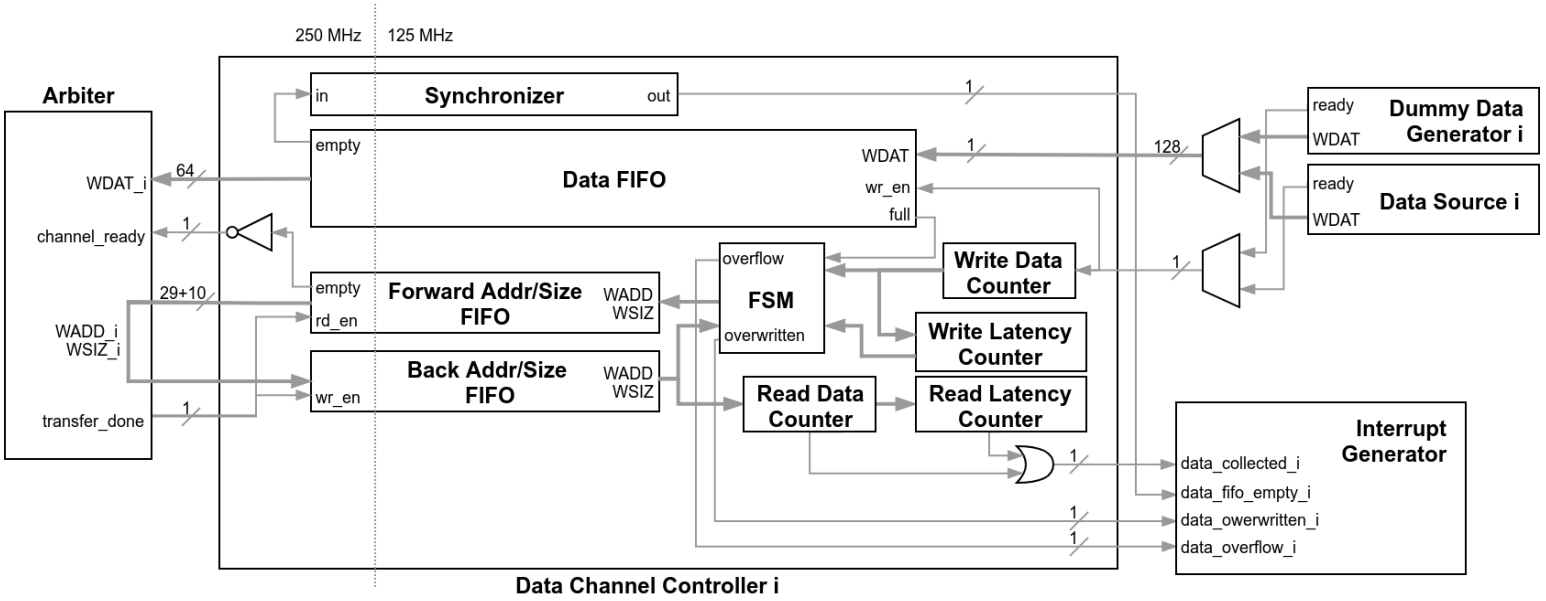
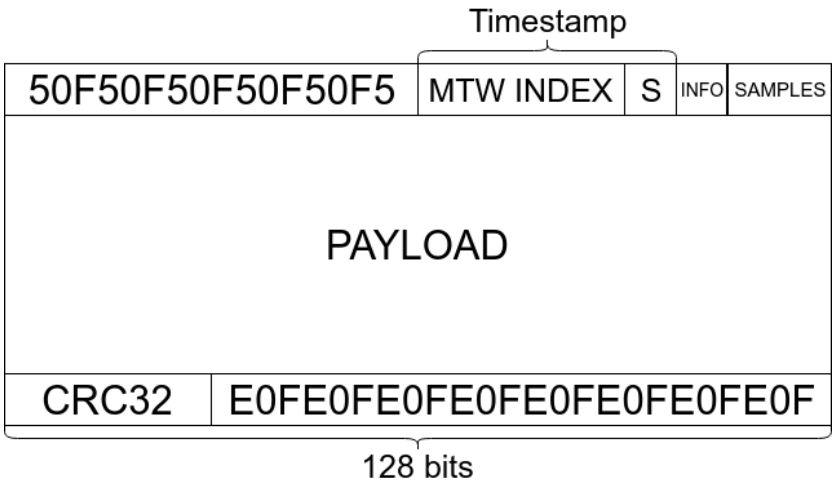
Circular Buffer Implementation



- Read pointer, write pointer for each channel
- Overflow – not able to write data to DDR at given input data rate
- Overwrite – data readout by DMA too slow
  - Read pointer at the moment of overwrite recorded

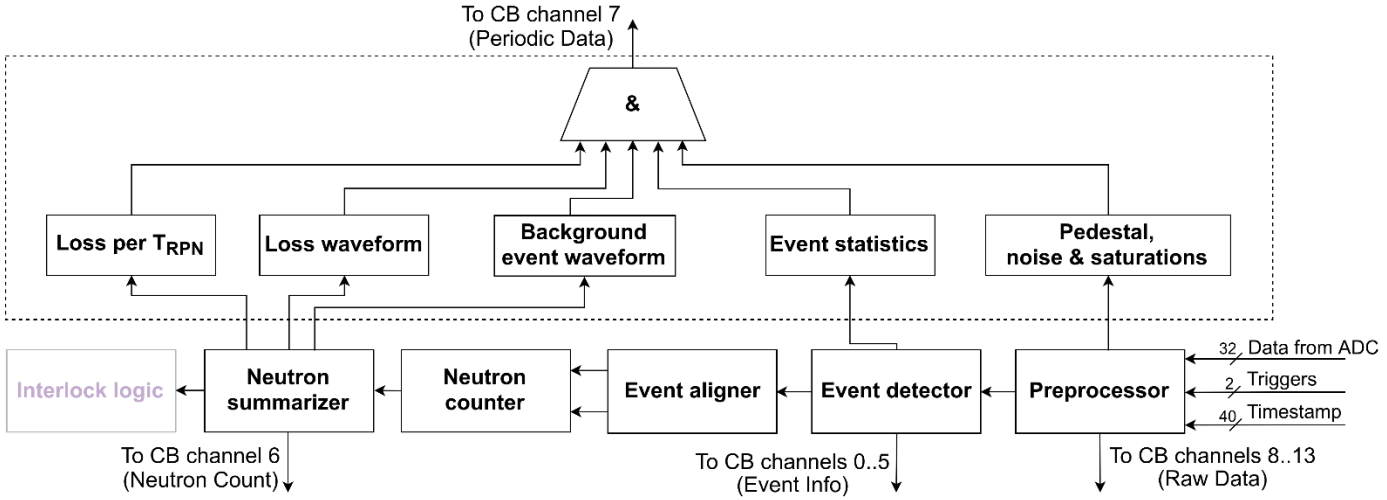
Frame layout

- Start-of-frame pattern
- Timestamp
  - Serial number of the 1-microsecond window
  - Sample index within the window.
- 1 generic information byte
- 16-bit number of samples in the frame
- Payload packed back-to-back on the bit level without any additional padding
- 32-bit CRC of all the previous words in the frame followed by the End-of-frame pattern.



nBLM algorithms block diagram

- Main flow – 5 pipelined processing blocks
- Implemented in C++ with High Level Synthesis
- Data in raw data, neutron summary and raw events channels timestamped by MTW number and sample number within MTW
- Periodic data – timestamped in the same way, but not cycle-accurate

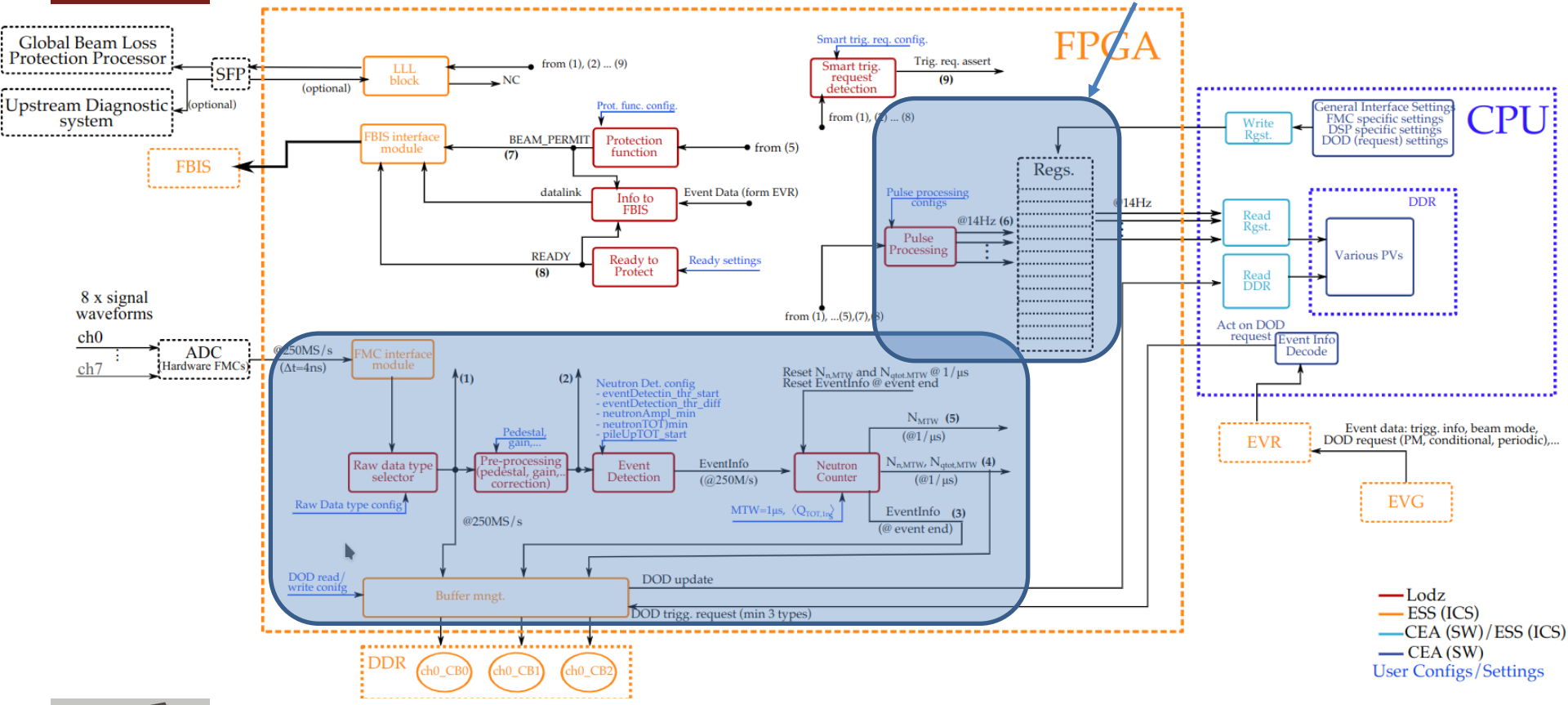


Event detection algorithm

```
void
detect (hls::stream<preprocessedData>& A, hls::stream<eventInfo>& E, hls::stream<eventInfo>& E2,
hls::stream<pedestalComputationData>& PC, hls::stream<eventInfoForArchiving>& event_stream,
uint16_t neutronTOT_min_indx, uint16_t pileUpTOT_start_indx)
{
#pragma HLS LATENCY min=1 max=1
#pragma HLS PIPELINE II=1
#pragma HLS INTERFACE axis off port=A
#pragma HLS DATA_PACK variable=A
// ….
for (int i = 0; i < 2; ++i)
//…
      if (data.belowThr1 || (data.belowThr2 && ended_by_frame))
        {
          //start an event
          if (!bEve)
            {
              MTWindx = data.frame_index;
              bEve = true;
              TOTstartTime = data.sample_index;
              peakValue = data.adjusted_sample;
              peakTime = 0;
              peakValid = false;
              TOTvalid = false;
              pileUp = false;
              TOTlimitReached = false;
              event_isPart2 = ended_by_frame;
              TOT = -1;
              Q_TOT = 0;
              peakCounter = 0;
```

nBlm Implementation status

Periodic data is available via DDR



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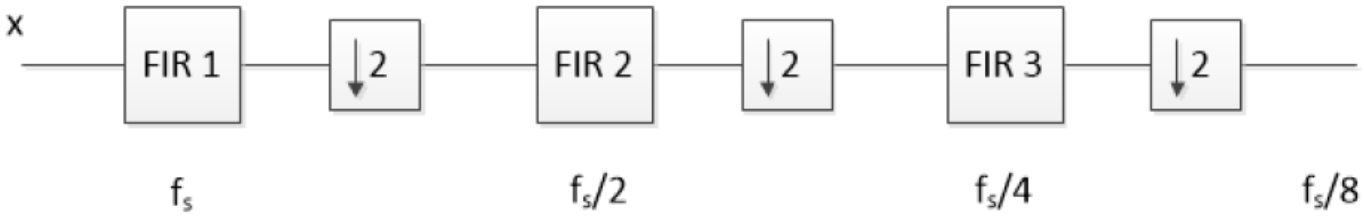
icBLM algorithms

- ICBLM is much less demanding (in terms of data rates and clock frequencies) than nBLM
- So far, the most complex block is HV 0.1 Hz modulation detection
- Two proposals:
  - Do a Fast Fourier Transform of the input signal and have the magnitude of several frequencies
  - Apply Goertzel algorithm to verify a presence of a specific frequency
- We have decided to implement FFT so the operator sees more information on the panel.
- Background correction algorithm

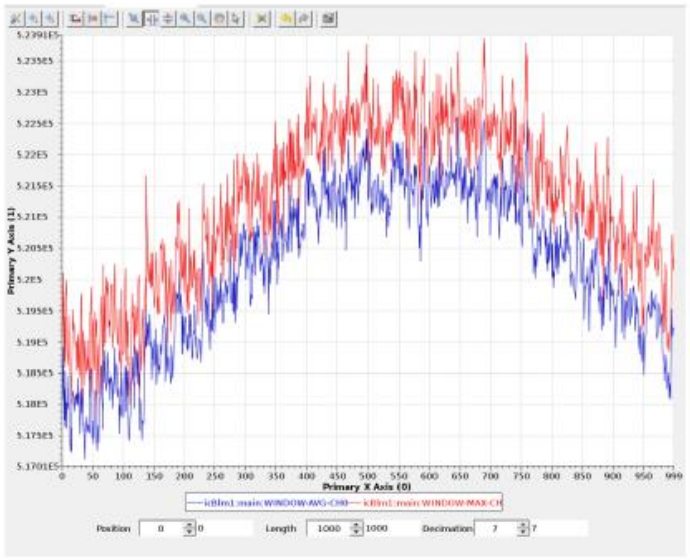
icBLM algorithms – antialiasing

- Reduce the sampling rate to ca. 1 Hz before further processing.
- First filter out higher frequencies
- Then take every n-th sample
- For the bandwidth 0.4 Hz at 1 Ms/s sampling the FIR antialiasing filter would need a few millions coefficients
- At decimation factor > 10 multistage decimation is more efficient.

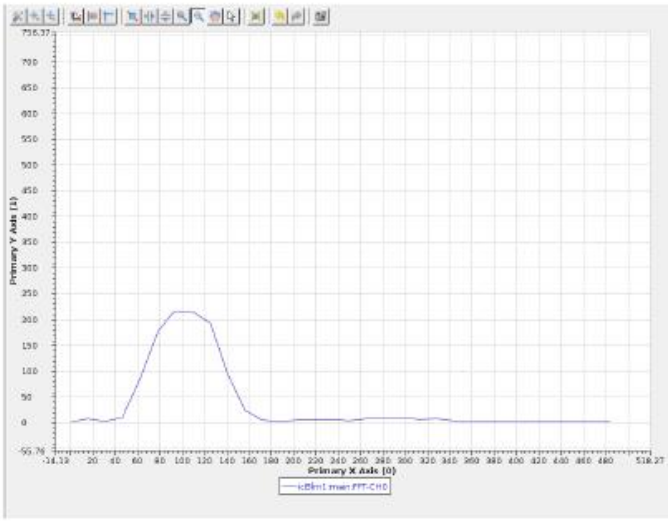


icBLM algorithms

- The results of FFT are transmitted in the periodic data channel.
- One can choose among rectangular, Hamming, Hann, Bartlett, Flattop windows.
- The DC level has been removed by subtracting the average of data in window from each sample.
- Below the results for 1% modulation, with 10 decimation stages, flattop window.



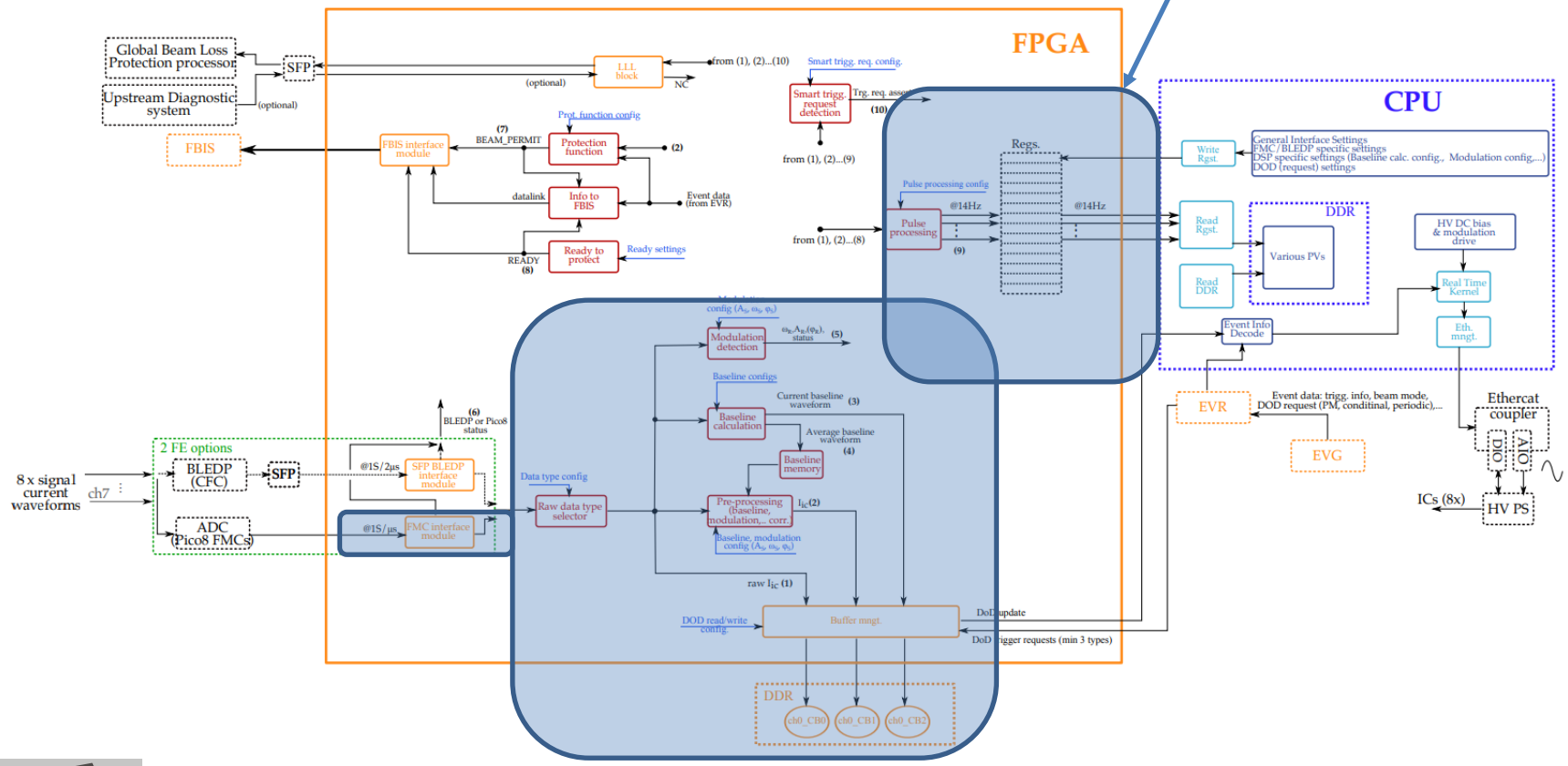
Raw data (100 Hz)



FFT

icBlm Implementation status

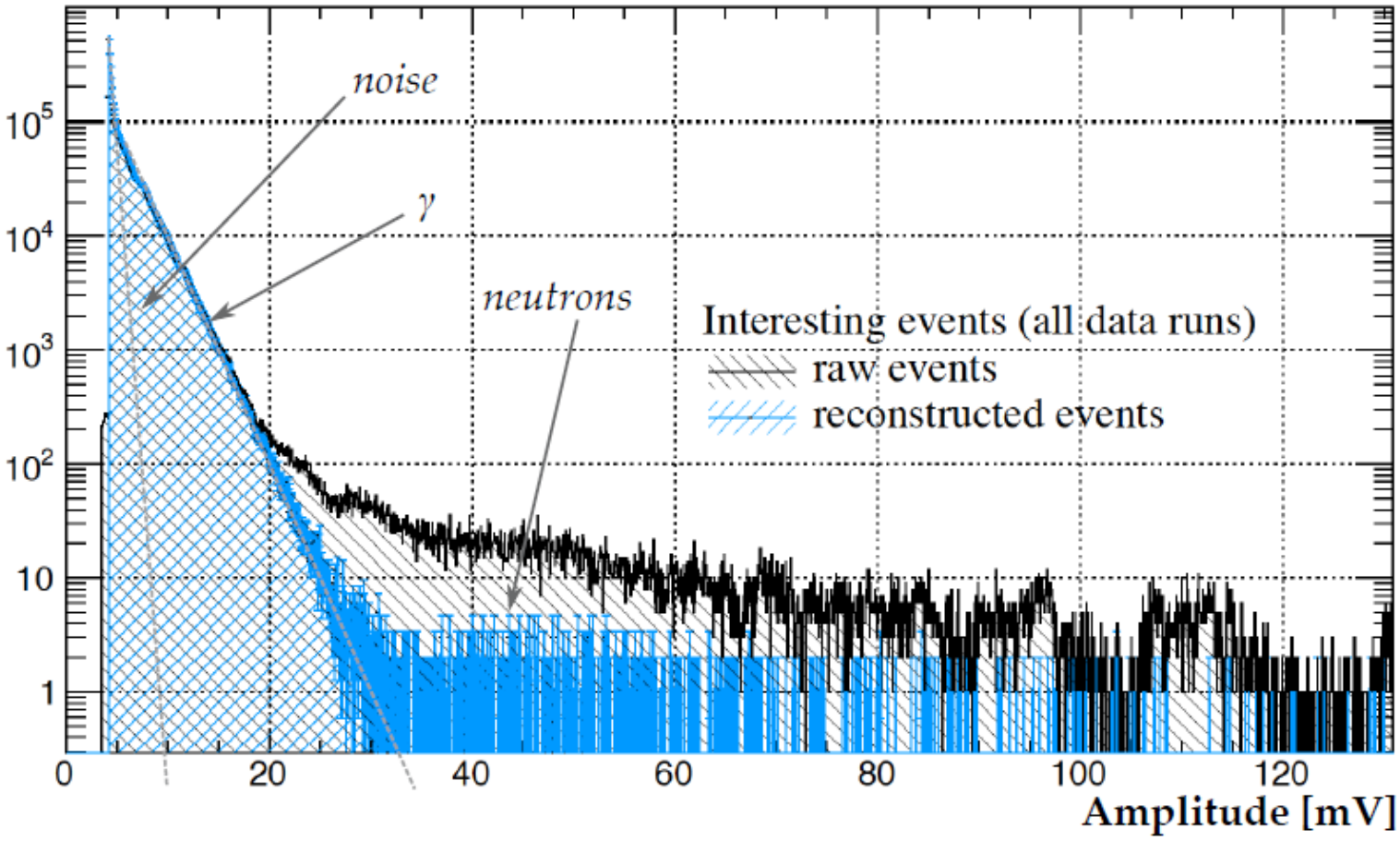
Periodic data is available via DDR



nBLM tests

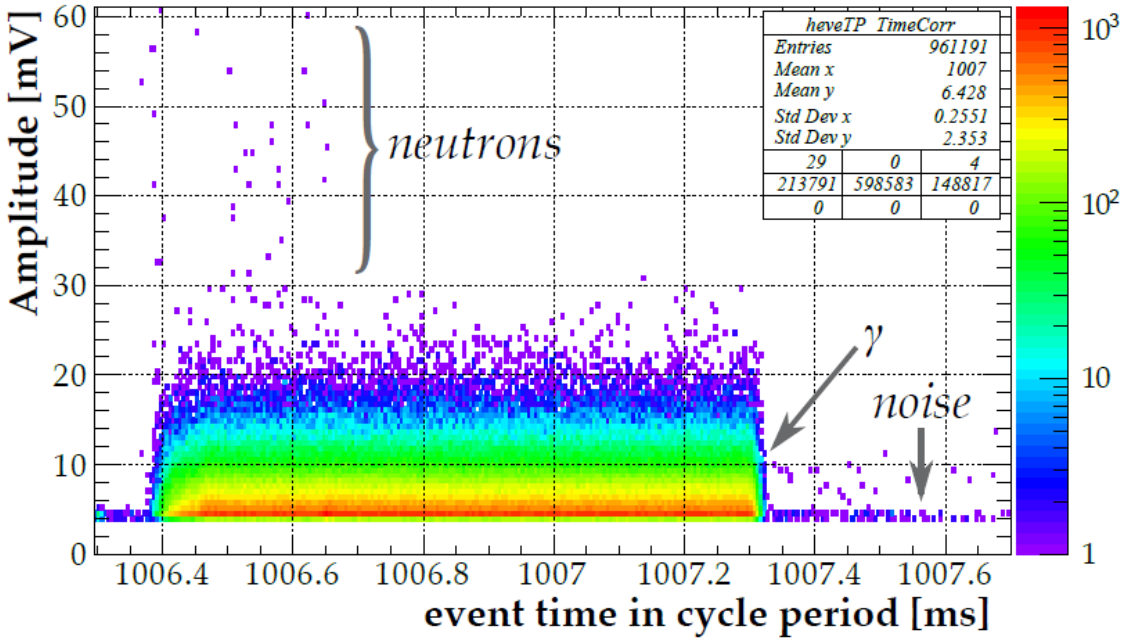
- In December 2018, a nBLM-F pre-series detector module was installed at LINAC4 at CERN, in the section where conditions close to the ones expected in the ESS DTL can be expected.
- The module was placed close to the beam pipe at the inter-tank region between DTL1 and DTL2 tank, where H^- beam energy reaches 12 MeV

nBLM tests


noise
γ
neutrons
Interesting events (all data runs)
raw events
reconstructed events
10^5
10^4
10^3
10^2
10
1
0
20
40
60
80
100
120
Amplitude [mV]

nBLM tests

- There were some problems with interpretation of the data, as the system did not support external timestamp source.
- The exact ADC clock rate has been estimated based on the optimization of the steepness of the falling edge of the event count distribution.



icBLM tests

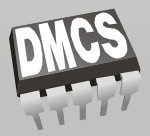
- icBLM implementation tested only in Lab environment
- Testing with real detectors will start in November

Problems

- The accelerator timing is not yet defined
- Background correction specifications in case of ICBLM cannot be finalised - no information about empty pulses
- Trigger sequence per cycle not precisely defined
- No examples or guidelines of how to work with beam data, synchronisation, timestamping
- Problems with standalone operation of EVR - timestamps abruptly jumping at every full second
- Not clear how to set up a test in realistic environment with external cycle trigger
- No power supply with HV modulation yet

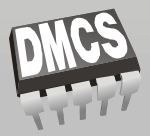
Problems

- Various problems with IOxOS boards and TOSCA framework
  - Limited memory and DMA bandwidth
  - Numerous problems with kernel driver (Tosca vs Tsc vs ESS Tsc, interrupt support, scatter-gather DMA)
  - Problems with timing closure
  - Problems with memory calibration at 275 MHz
  - Random CRC errors (might be also caused by software bugs)



Problems

- Tsc driver prone to resource leaks
- Problems with PCIe Gen3 link to Concurrent CPU



TODOs

- Implement and test protection function
- Interface with MPS using dedicated RTM board
- Prepare operator interfaces for icBlm (Epics + UI panels)
- Test Test Test
  - general reliability
  - system recovery
  - software independence

Thank you for your attention

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