From 40G to 100G and beyond
a new MCH concept

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Agenda

- MOSA at the example of MicroTCA
  - Why and Where
  - How application demands create increasing challenges
  - How actual limitations can be overcome
  - What is coming next

MOSA: *M*odular *O*pen *S*ystem *A*rchitecture

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Open Standards – the habitat of the talk

- Benefits:
  - ***Open*** means access to specification for everyone => standard
  - ***Standard*** means industrial supporters => growing ecosystem
  - ***Growing ecosystem*** means growing user base => increasing install base
  - ***Increasing install base*** means longevity support => safe to use for many years
  - ***Safe to use for many years*** means means long term users => new features
  - ***New features*** means keeping the standard state-of-the-art => future versions
  - **Future versions** means growing ecosystems and growing user base

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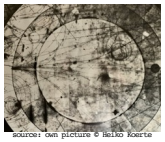
Where MicroTCA is being used today

- Automation
- Communication
- Defense & Aerospace
- Energy
- Industrial Control
- Medical
- Test & Measurement
- Transportation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... and **BIG** Physics
... and **small** Physics

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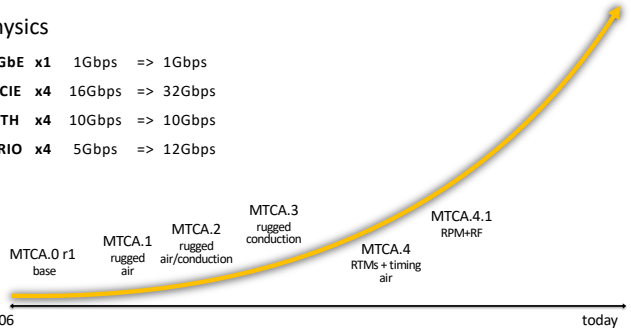
How MicroTCA was used before

- Physics

1GbE	**x1**	1Gbps	=>	1Gbps
PCIE	**x4**	16Gbps	=>	32Gbps
ETH	**x4**	10Gbps	=>	10Gbps
SRIO	**x4**	5Gbps	=>	12Gbps



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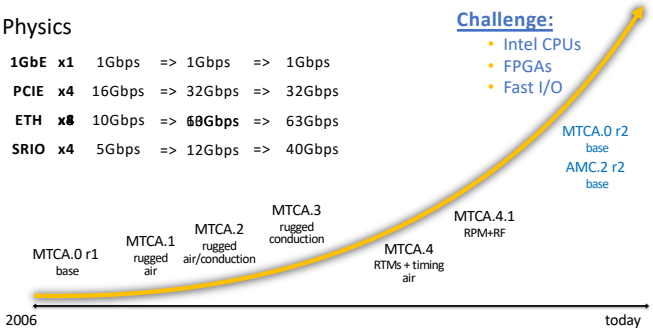
How MicroTCA is used today

- Physics

1GbE	**x1**	1Gbps	=>	1Gbps	=>	1Gbps
PCIE	**x4**	16Gbps	=>	32Gbps	=>	32Gbps
ETH	**x8**	10Gbps	=>	**40Gbps**	=>	63Gbps
SRIO	**x4**	5Gbps	=>	12Gbps	=>	40Gbps

Challenge:
- Intel CPUs
- FPGAs
- Fast I/O



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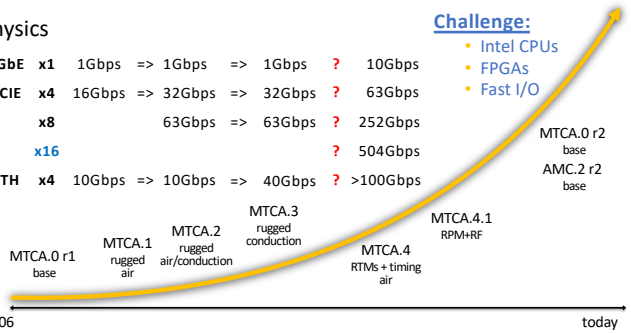
What MicroTCA needs to deliver tomorrow

- Physics

1GbE	**x1**	1Gbps	=>	1Gbps	=>	1Gbps	?	10Gbps
PCIE	**x4**	16Gbps	=>	32Gbps	=>	32Gbps	?	63Gbps
	x8			63Gbps	=>	63Gbps	?	252Gbps
	x16						?	504Gbps
ETH	**x4**	10Gbps	=>	10Gbps	=>	40Gbps	?	>100Gbps

Challenge:
- Intel CPUs
- FPGAs
- Fast I/O



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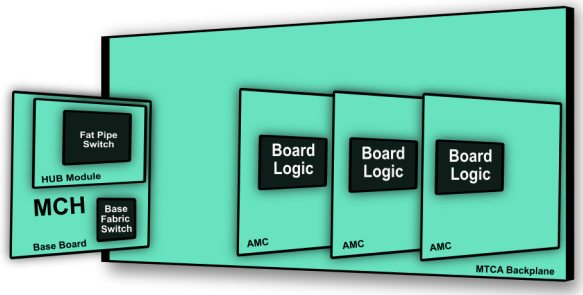
Current MicroTCA setup (common approach)



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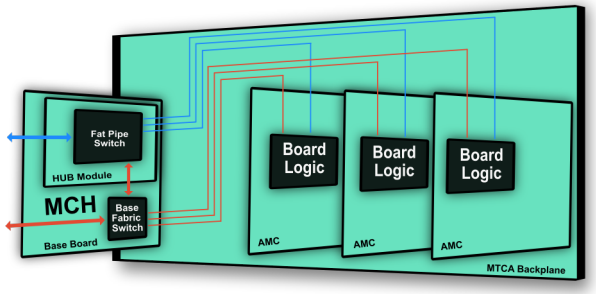
Current MicroTCA setup (common approach)



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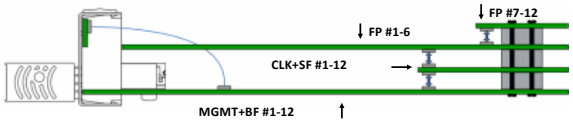
Current MCH setup and future requirements



Base Fabric
- 1GbE => 10 GbE
- Uplinks: wire => fibre

Storage Fabric => "slim fabric"
- not only storage but others, too
  i.e. USB, PCIe x1

Clocks
- high precision CLK incl. OCXO
- IEEE 1588
- GPS

Fat Pipe Fabric
- PCIe: Gen 4+5 => Gen "6"
- ETH: 40G => 100G
- Uplinks: multiple of fat pipe b/w

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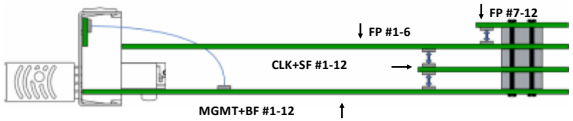
Current MCH setup and future requirements



- Challenges b/o higher bandwidths
  - MCH fat pipe switch needs more power
  - MCH fat pipes require different backplane connector
  - MCH must maintain scalability
  - MCH must maintain backwards compatibility
  - AMCs may need more power
  - management needs to be extended

=> requires a new concept for MCH

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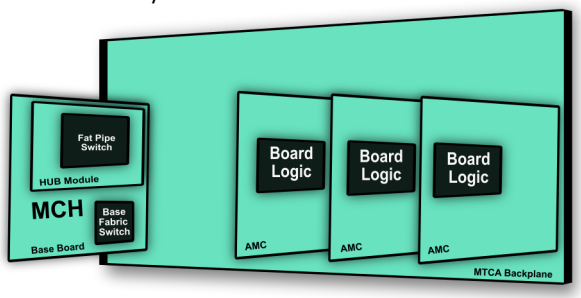
The challenge

- Current MicroTCA system



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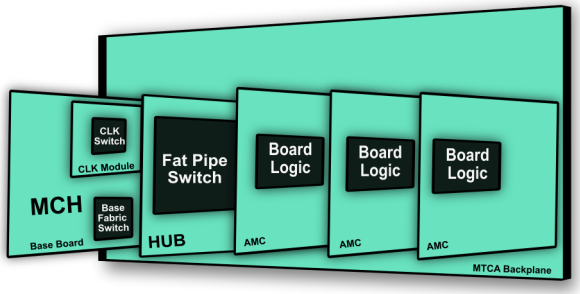
The new approach

- Future MicroTCA system



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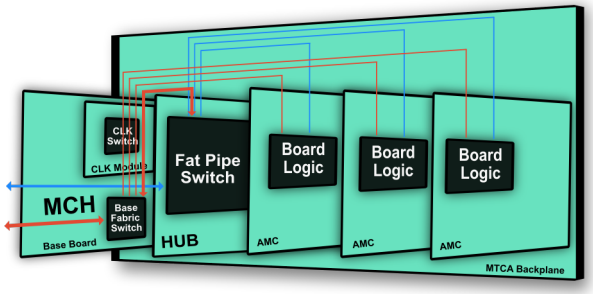
The new approach

- Future MicroTCA system



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The new approach

- new PICMG work group "Next Generation MicroTCA"
  - Since end of 2019
  - Members represent
    - Manufacturers
      - Chassis (incl. cooling and backplane)
      - Power Modules
      - MCHs
      - AMCs
      - Mechanical components such as connectors
      - Silicons
    - Users
  - Goal
    - Improve MicroTCA so that it can meet the requirements for the **next 10-15 years**
    - Keep next generation of MicroTCA backward compatible

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Conclusion

- new demands and requirements from high and low ends
- current design needs to be maintained for reasons of costs and compatibility
- a new concept for high end demands

There is no doubt… it is time! 😃

Thank you!

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