A VXS[VITA41] Trigger Processor 12GeV Experiments At Jefferson Lab

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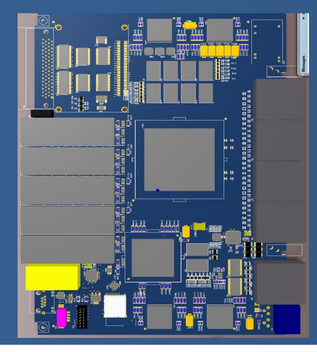
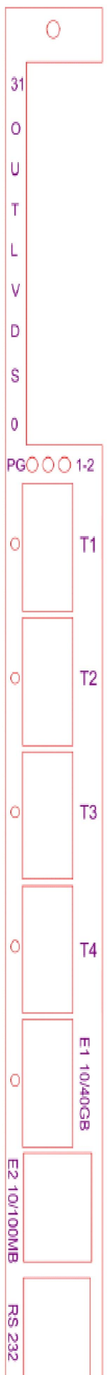


VXS Trigger Processor Specifications

3.2 Specification Summary



MECHANICAL
- Single width VITA 41 (VXS) Switch Module

Trigger Interface and Switch B signaling
(Signal Distribution module)
- 250MHz Clock (LVPECL)
- Trig1, Trig2, Sync (LVPECL)
- LINKUP out (LVTTL)
- BUSY out (LVTTL)

GIGABIT DATA STREAMS
From/To 16 Payload Slots (FADC, SSP, VETROC, DCRB, etc.)
- 4 full duplex lanes up to 8.5Gbps
- 544Gbps Aggregate

Outputs:
- 32 LVDS front panel outputs to Trigger Supervisor
- 1x RJ45: 100/1000Mbps Ethernet
- 32 I/O expansion mezzanine (LVDS/ECL/PECL/NIM/Analog)
- 4x QSFP Fiber Transceivers (34Gbps)
- 10/100/1000Mbps Ethernet (RJ45)
- 1x QSFP 10/40Gbps Ethernet
- RS232 console serial port

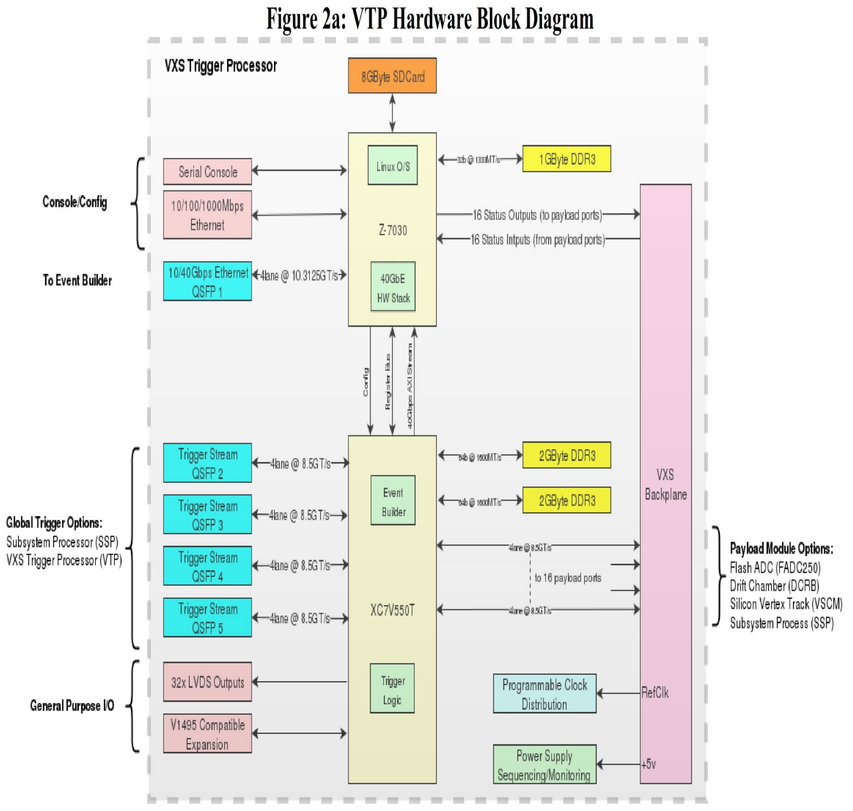
Indicators: (Front Panel)
- Power – Blue LED
- Trigger – Amber LED
- Alarm – Red LED Programming and Trigger Data Input:
- On board JTAG Port
- Virtex 7 550T; 80GTH Gigabit transceivers
- 1GHz ZYNQ-7030 SoC processor with Linux OS
- Global Trigger equation and processing for up to 16 JLAB SubSystem Processors
- Front End Trigger processing for up to 16 JLAB Flash ADC digitizers
- 8GB Micro SD card support (Linux OS file system + FPGA image)
- 1GB DDR3 SDRAM

Power Requirements:
- +5v @ 10 Amps (typ. from Backplane)
- Local regulators for other required voltages

Environment:
- Forced air cooling: Heat sink
- Commercial grade components (85°C max)

2. Functional Description

Figure 2a: VTP Hardware Block Diagram



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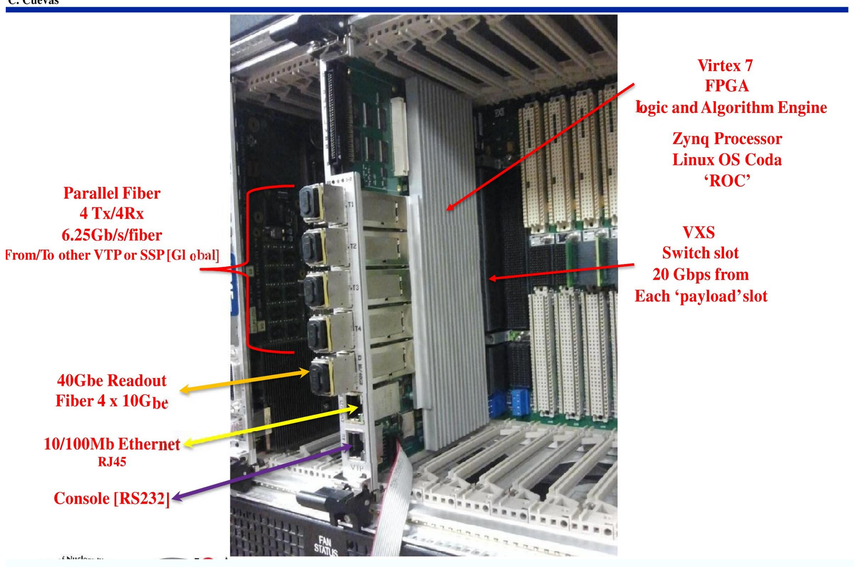
VXS Trigger Processor
Switch Slot Board



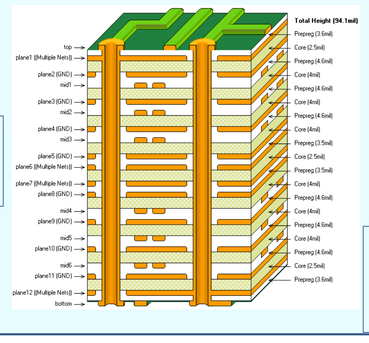
At Jefferson Lab we design and build circuits and firmware to:

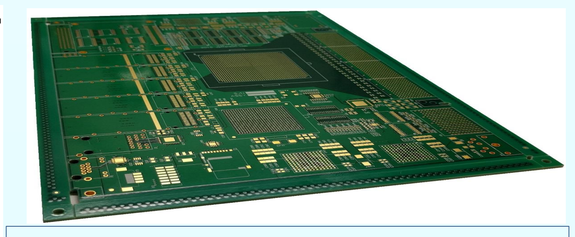
- digitize the small, ultra-fast electrical signals produced by the experimental detectors.
- look for patterns in the data and select the events of interest.

The Flash Analog to Digital Converter (FADC250) samples thousands of analog signals 250 million times per second. Each of the signals can be really fast: done and gone in just a few billionths of a second.

JLab Printed Circuit Boards (PCBs) carry many integrated circuits like Field-Programmable-Gate-Arrays (FPGA), Analog-to-Digital-Converters (ADC), Serializer/Deserializer (SerDes), and many other types.

JLab PCB boards are:
20 layers of copper
19 layers of dielectric





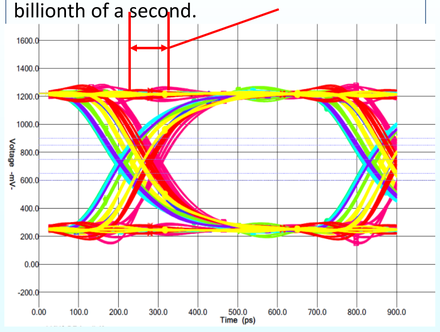
Example of JLab circuit: some components have nearly 2000 pins connected to the rest of the board throughout the 20 layers

XILINX FPGA Ball-Grid-Array Integrated Circuit

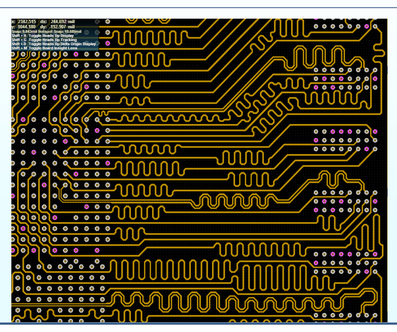
This FPGA has 1,927 solder balls that connect it to the circuit board.

VTP Electrical Modeling – DDR3 Memory Data

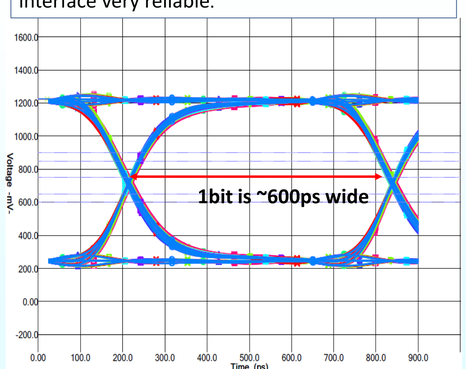
We can detect if the data bits are not aligned in time, which reduces the margin for a working design:
We can measure delays of 1/10 of one billionth of a second.



Adding some wiggles in the PCB traces/wires to make all data bits show up at the same time. 1/10 of one billionth of a second delay is equal to about 1/2" of length inside the PCB.



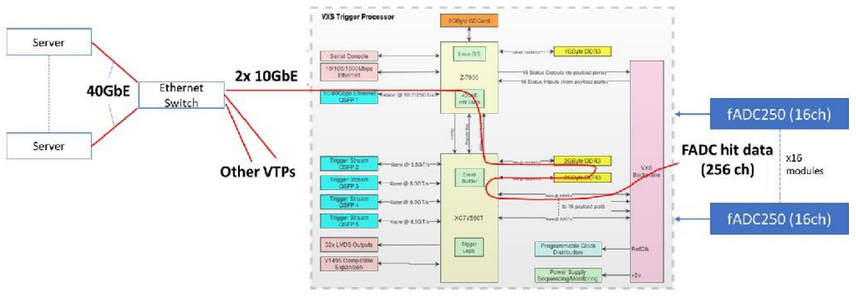
After delay correction simulation shows all data bits are transitioning together, making the interface very reliable.



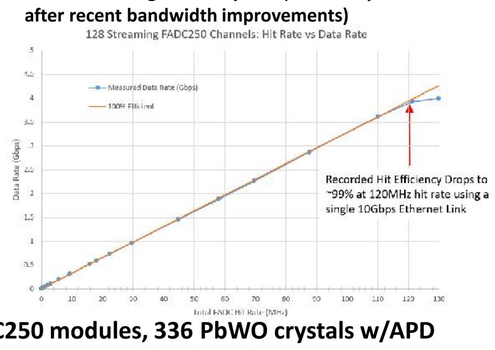
Using The VXS Trigger Processor – Detector Beam Experiment – CLAS12 Forward Tagger Calorimeter

- The VXS Trigger Processor is used in several experimental Halls at JLAB.
- Front-End digitizer and other 'PayLoad' boards send data to the VTP via the VXS back-plane. This trigger 'data' is transported to a final VTP that creates a global trigger for the given experiment.
- We are developing Streaming ReadOut DAQ systems for future experiments and will take advantage of the elegant high speed serial links that are part of the VITA41 standard.
- The diagram on the right, shows a recent example of the Streaming ReadOut system with a beam test in the CLAS12 experiment at JLAB.
- 336 PbWO crystals with APD photo detectors were instrumented to our front end flash ADC. The VTP provided the streaming data readout function and demonstrated the successful operation of the SRO software which was a combination of CODA, TRIDAS, JANA and ROOT programs.

Drawing illustrates a test we performed in a Hall B beam test Feb 2020 using the CLAS12 FT calorimeter (336 FADC channels)

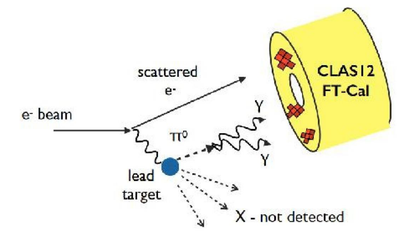


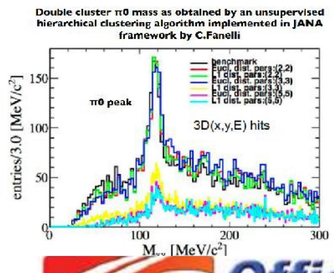
DAQ can handle close to 1MHz rate per FADC channel before suffering efficiency loss (it is nearly 2x better after recent bandwidth improvements)



Front-end setup: 2 VXS crates, each with VTP w/ 2x 10GbE optical links, 11 FADC250 modules, 336 PbWO crystals w/APD
Backend setup: servers connected to front-end ethernet switch by 40GbE. Software as a combination of CODA, TRIDAS, JANA, ROOT that together performed configuration, event selection, event reconstruction, and online monitoring.

π^0 reconstructed signal from streaming data:





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