Data Acquisition System for the COMPASS++/AMBER Experiment

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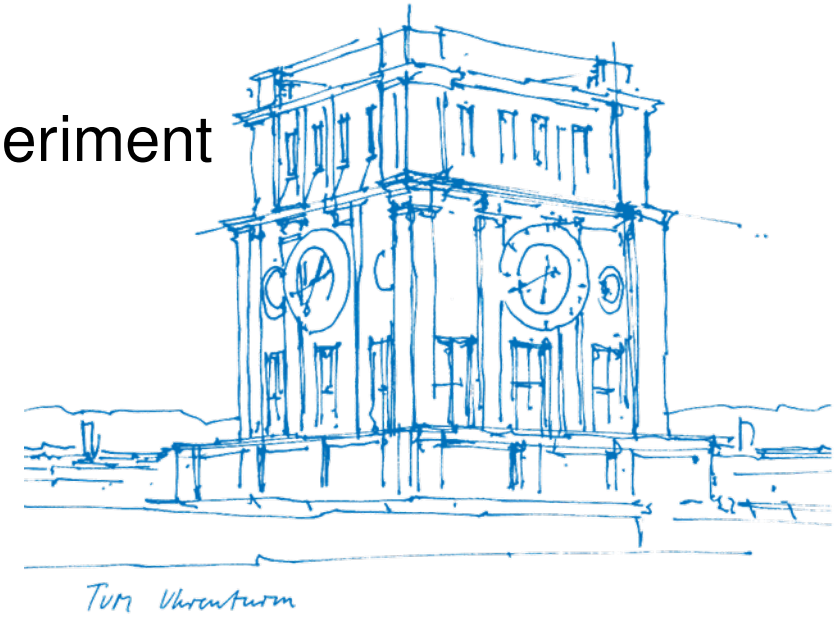
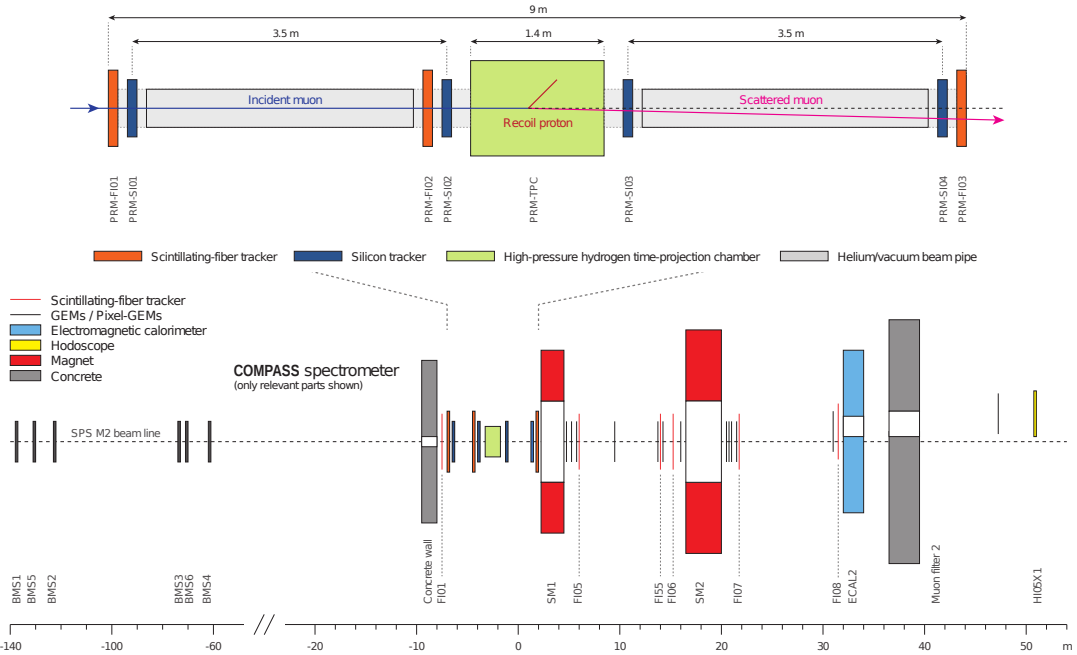
22nd IEEE Real Time Conference



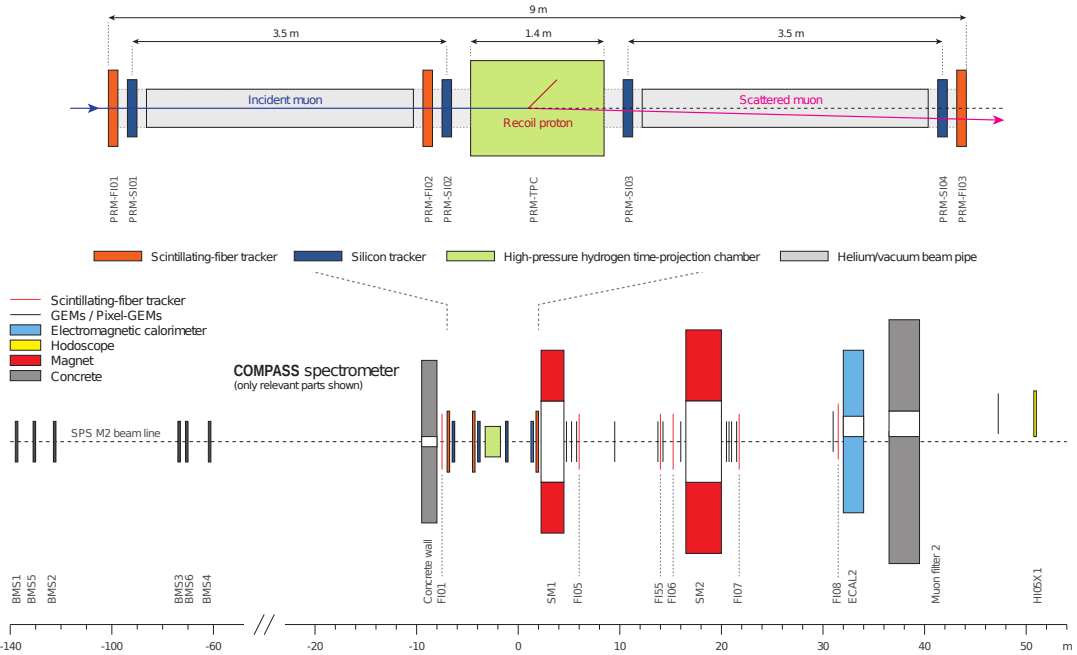
Overview

Measurements at the COMPASS++/AMBER



- Measurements
  - Drell-Yan process
  - Antiproton production cross seaction
  - Proton radium measurement with muons

Measurements at the COMPASS++/AMBER



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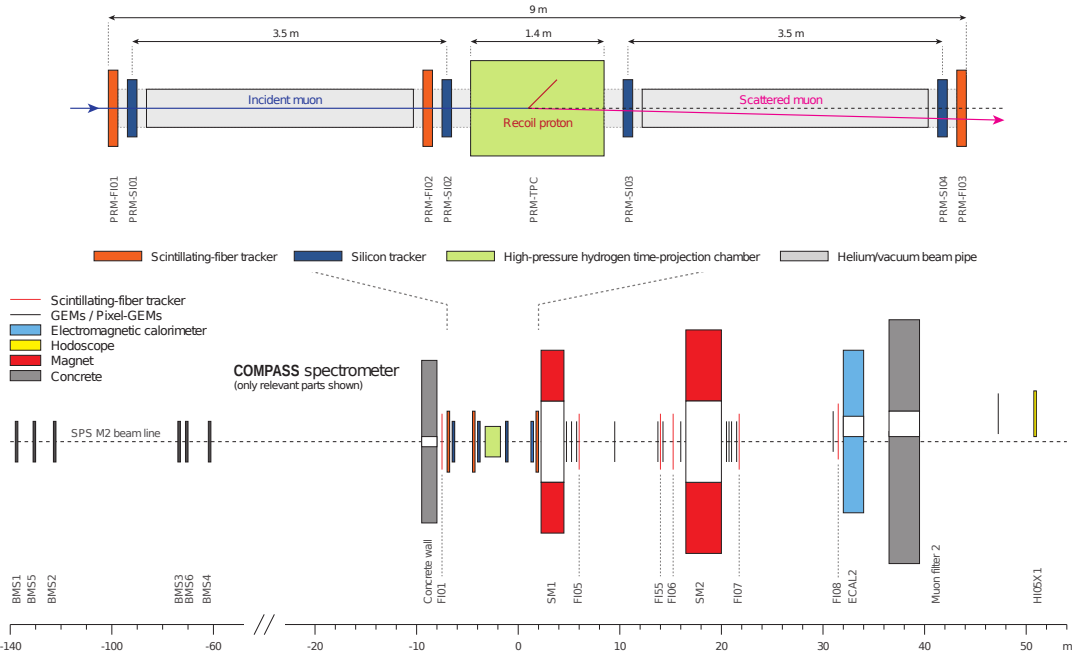
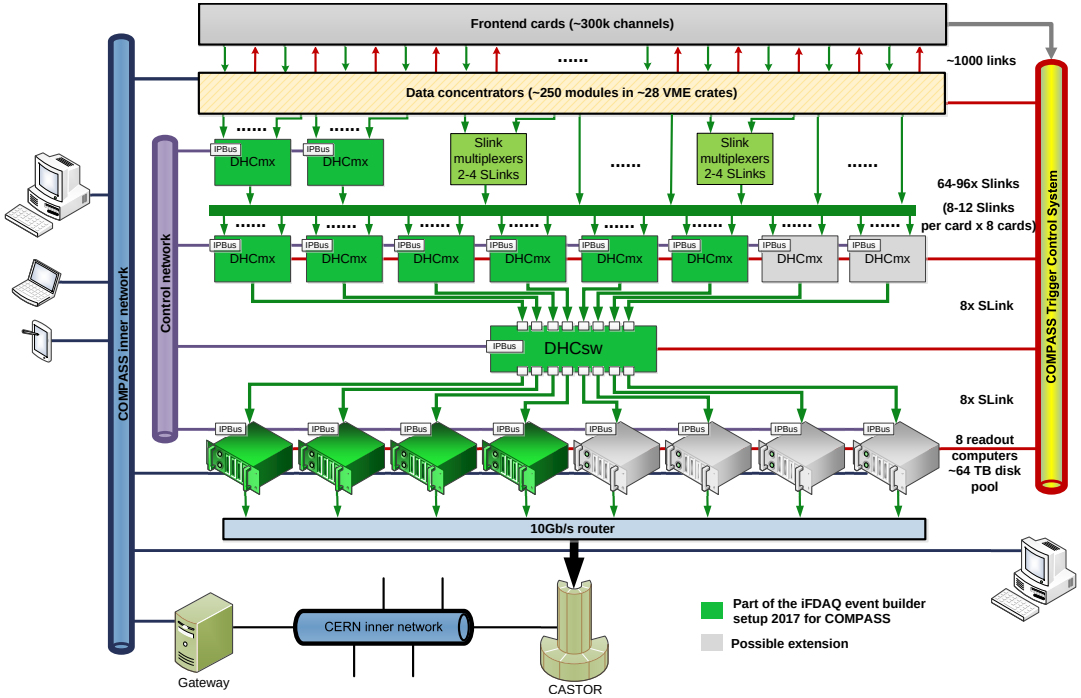


- Measurements
  - Drell-Yan process
  - Antiproton production cross seaction
  - Proton radium measurement with muons
- Low-angle scattering at active hydrogen target
- Long read-out time of the TPC
  - long trigger decision time

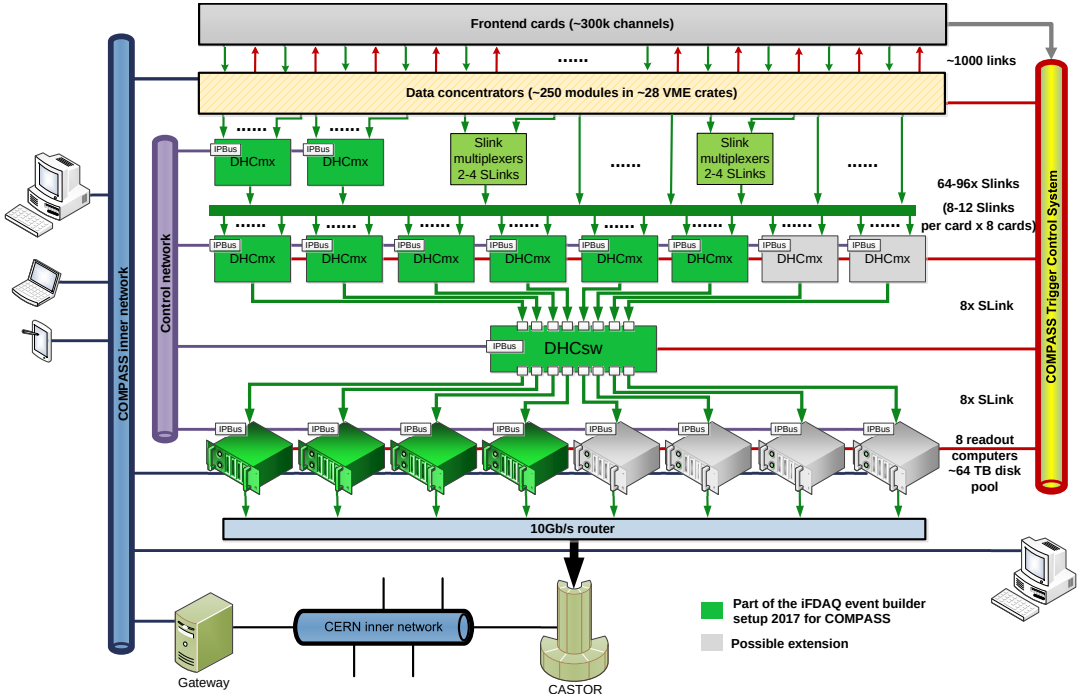
  $\Rightarrow$ free-running DAQ needed

Current COMPASS Data Acquisition Architecture



- Event builder
  - fully FPGA-based
  - events stored in external memory

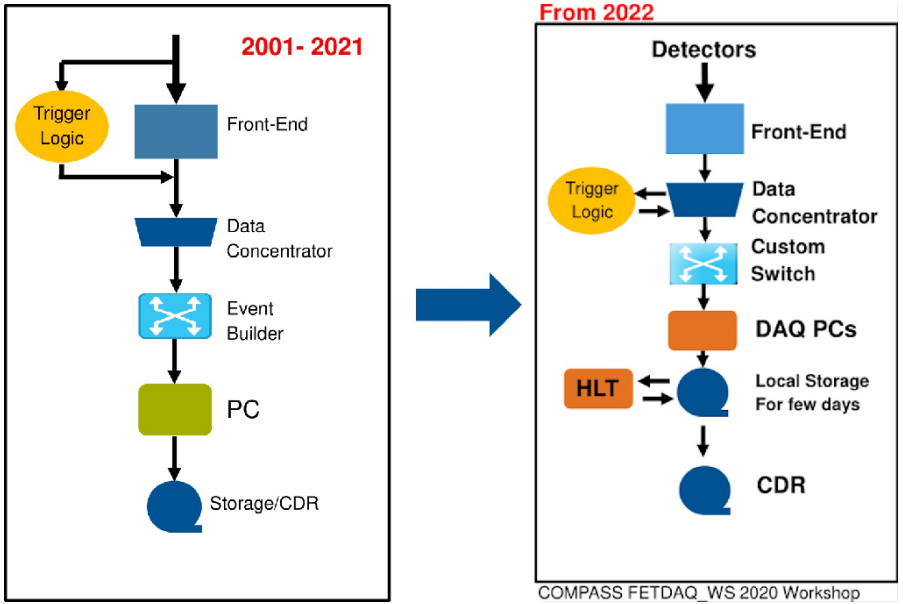
Current COMPASS Data Acquisition Architecture



- Event builder
  - fully FPGA-based
  - events stored in external memory
- Bottleneck:
  - Memory throughput 3 GB/s

  ⇒ not easy scalable

New COMPASS Data Acquisition Architecture



- **Triggered** read out until 2021
  - conventional DAQ architecture with hardware-based trigger logic
- **Triggerless** read out in 2022
  - online filtering by hardware-based trigger logic
  - offline filtering by software-based high-level trigger

New COMPASS Data Acquisition Architecture

Figure: Timeslice in a triggerless readout mode

- timeslice-based readout
  - defined for triggerless read-out
  - compatible with old data format

New COMPASS Data Acquisition Architecture

Figure: Timeslice in a triggerless readout mode

- timeslice-based readout
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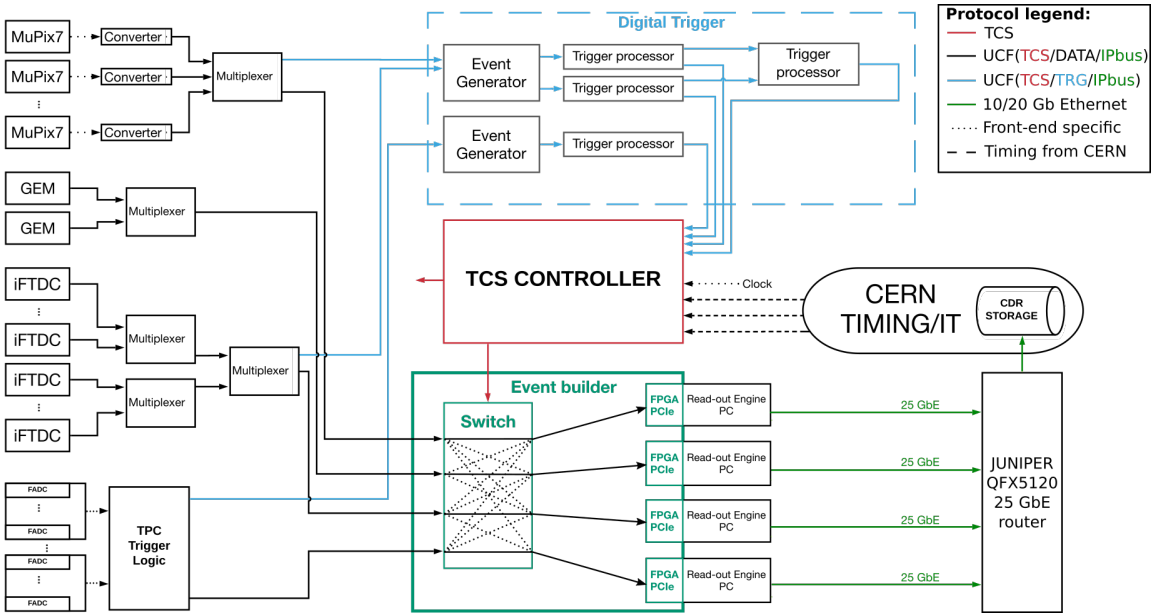
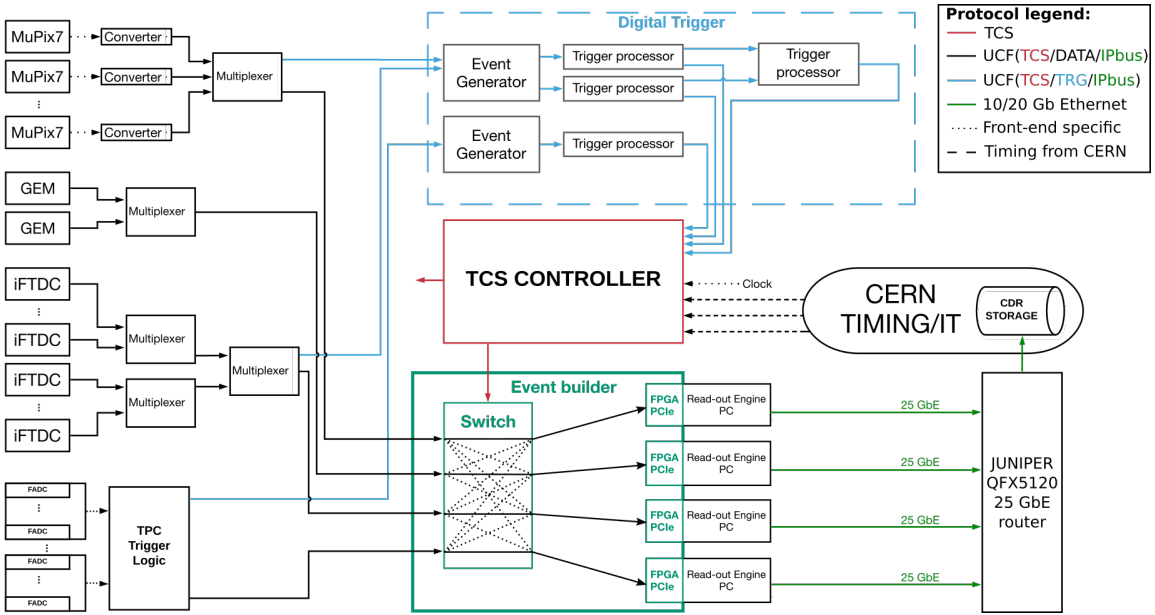
- Triggered and triggerless readout
  - **triggerless:** data frames (**images**)
    - different size due to different time resolution
    - select images for data reduction
  - **triggered:** events

New COMPASS Data Acquisition Architecture



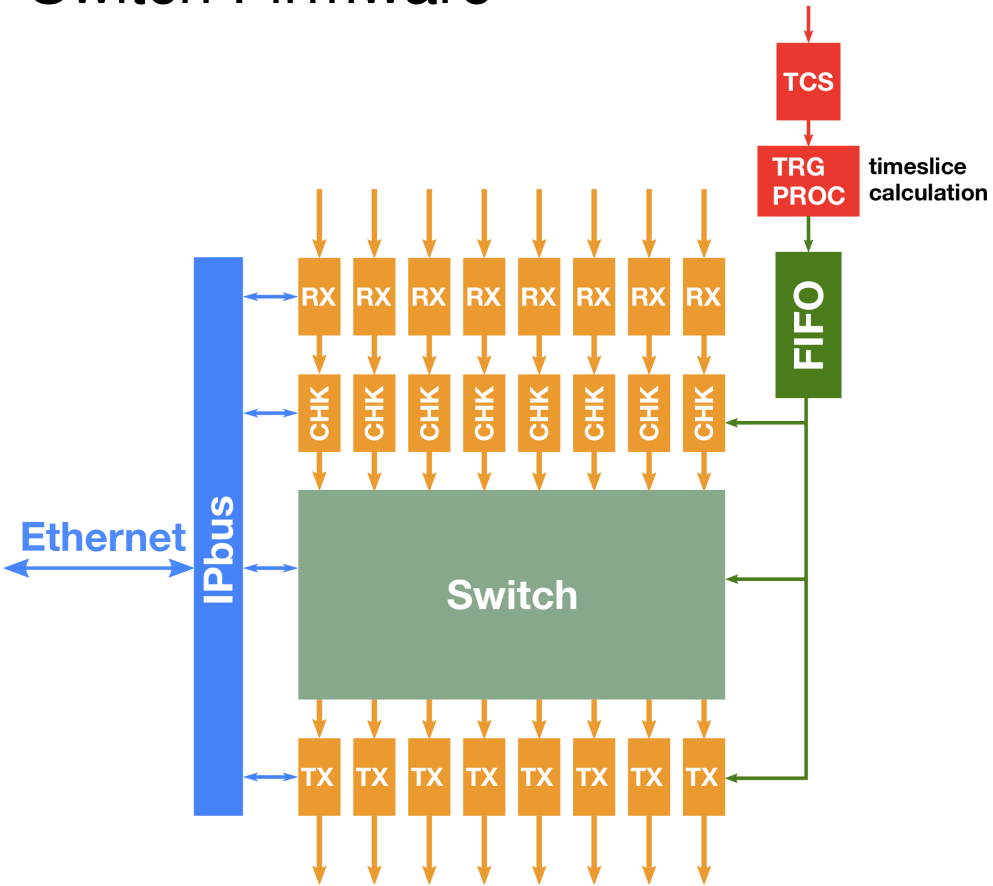
- Remove bottleneck
  - Pre-sort events before event building
  - increase number of event builder nodes

New COMPASS Data Acquisition Architecture



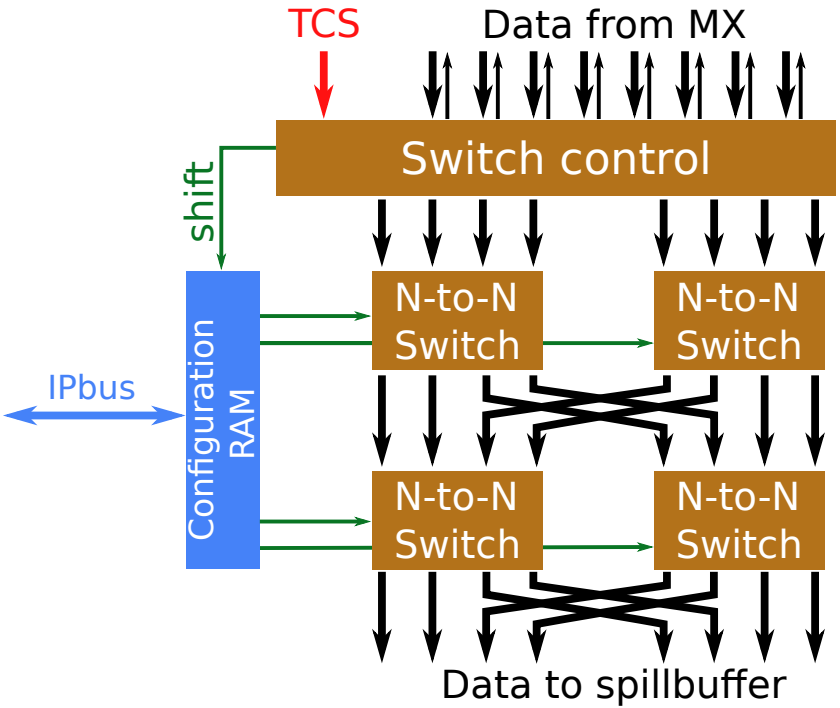
- Remove bottleneck
  - Pre-sort events before event building
  - increase number of event builder nodes
- N-to-N switch in FPGA fabric
  - no external memory for data
  - **requires memory in multiplexers**

Switch Firmware



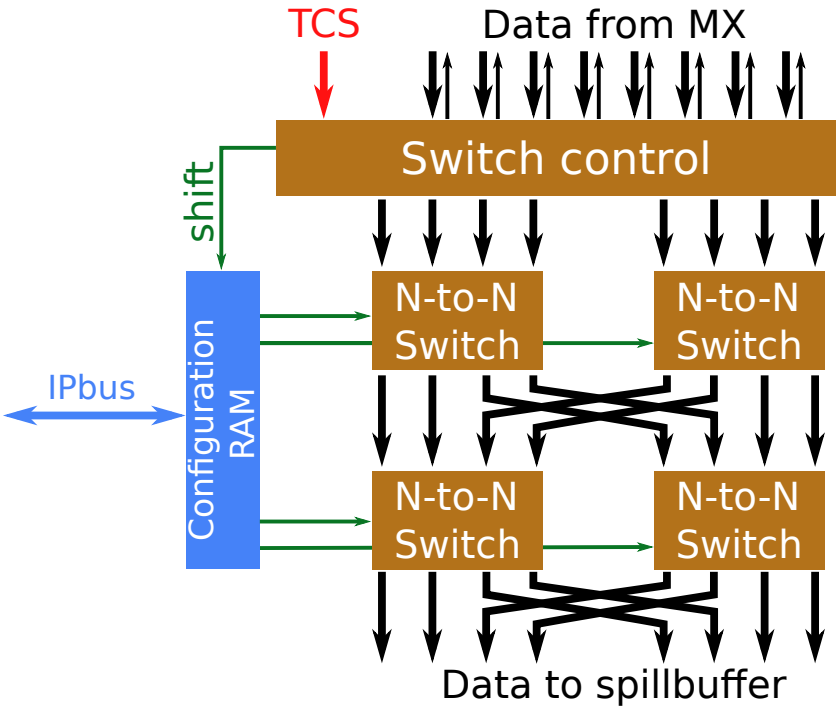
- 8 Slink receivers
- TCS receiver
- deep trigger FIFO in DDR3 memory
- 8x8 switch
- 8 6.25 Gb/s 8b/10b Aurora links
  - trigger and switch configuration distribution over sideband link
- slow control over IPbus
  - control
  - configuration
  - diagnostics

Switch Architecture



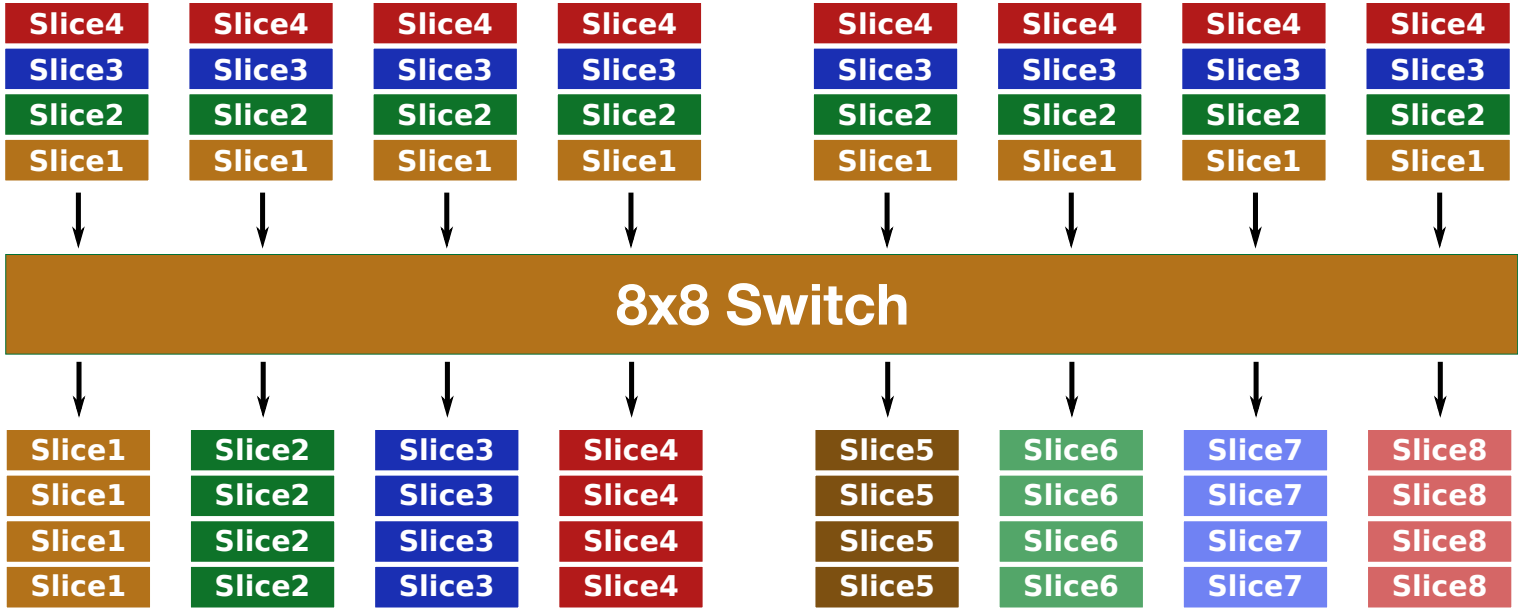
- Switch control
  - change of the switch mapping when
    - frame transmission for a given timeslice complete

Switch Architecture

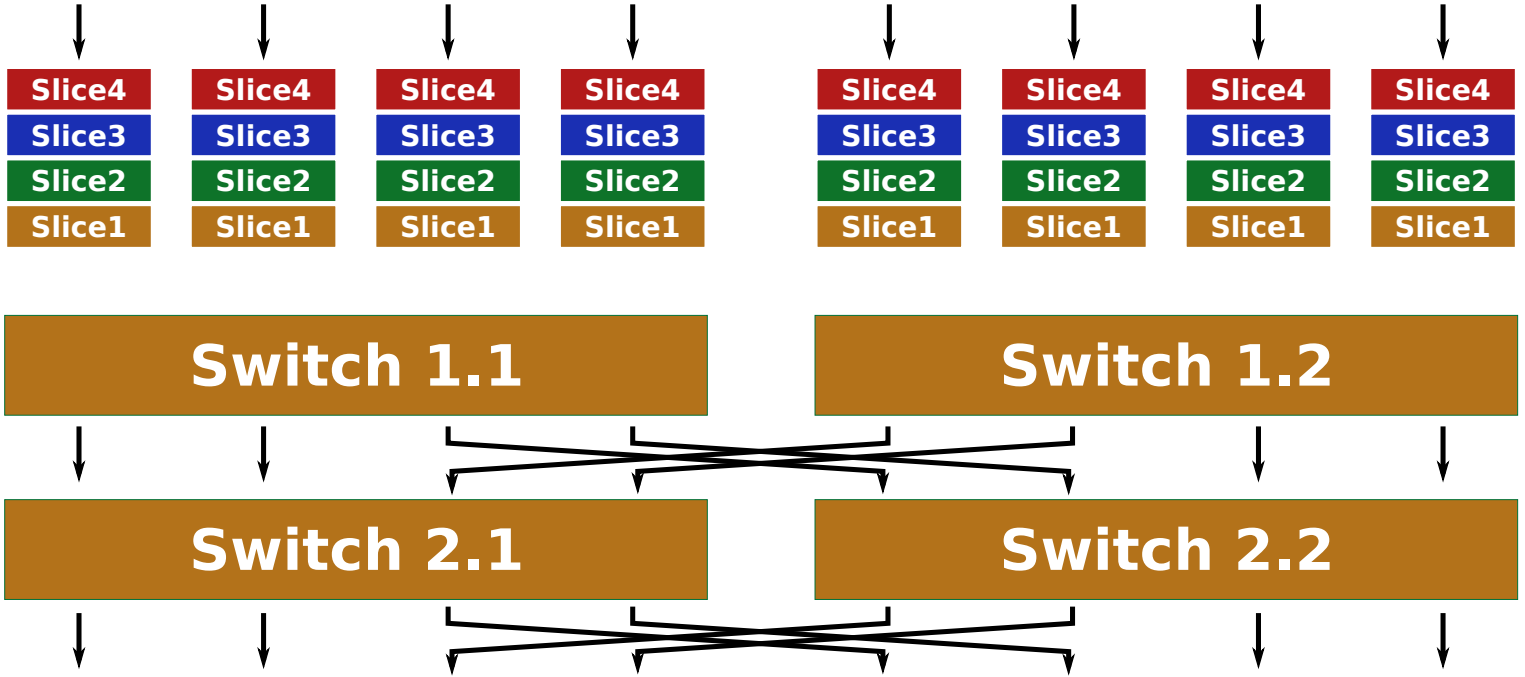


- Switch control
  - change of the switch mapping when
    - frame transmission for a given timeslice complete
- 4-to-4 switch
  - routes frames from an input to a specific output
  - input-output mapping change
  - configuration in BRAM

Switch Algorithm: General Idea



Switch Algorithm: Details



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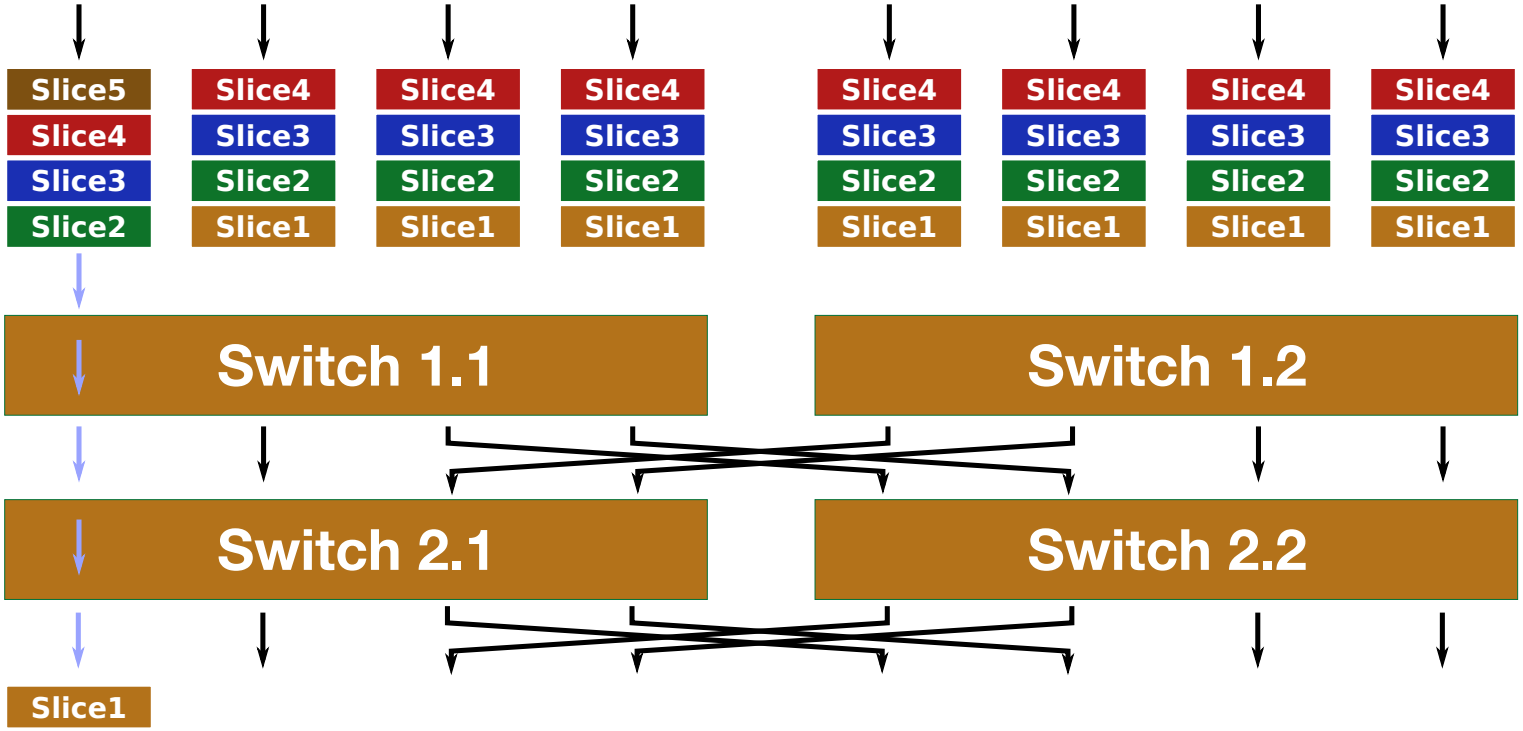

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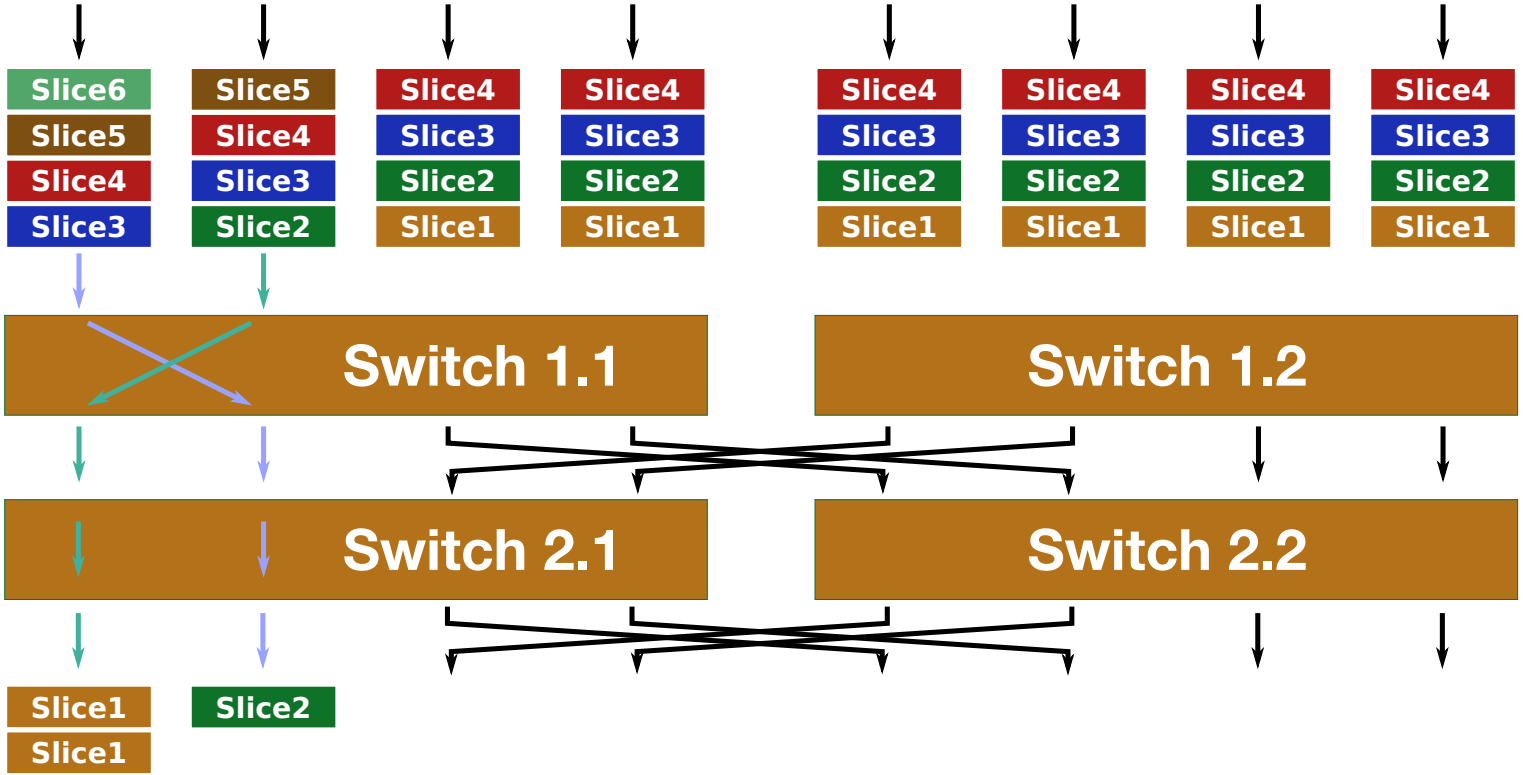

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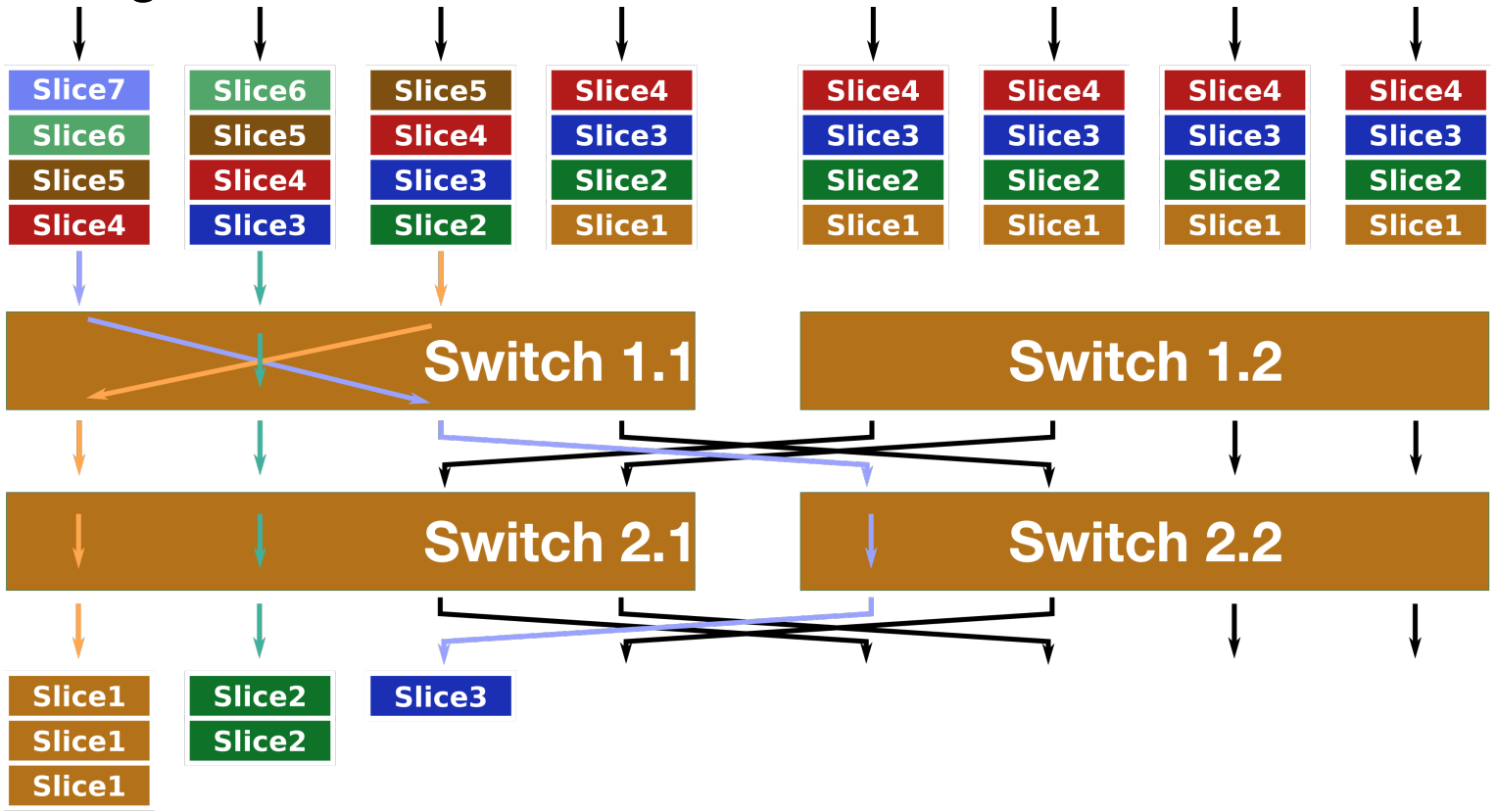

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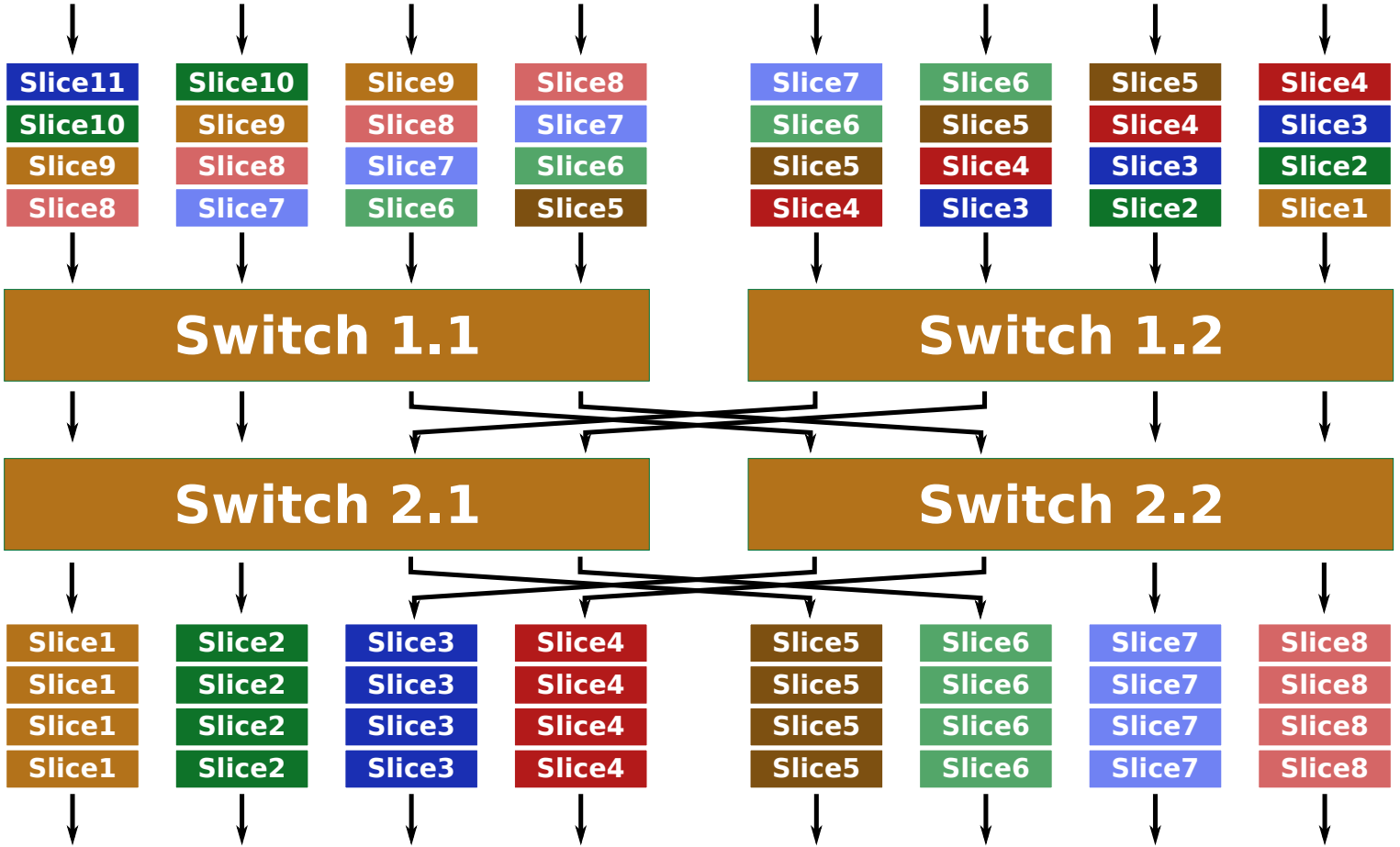
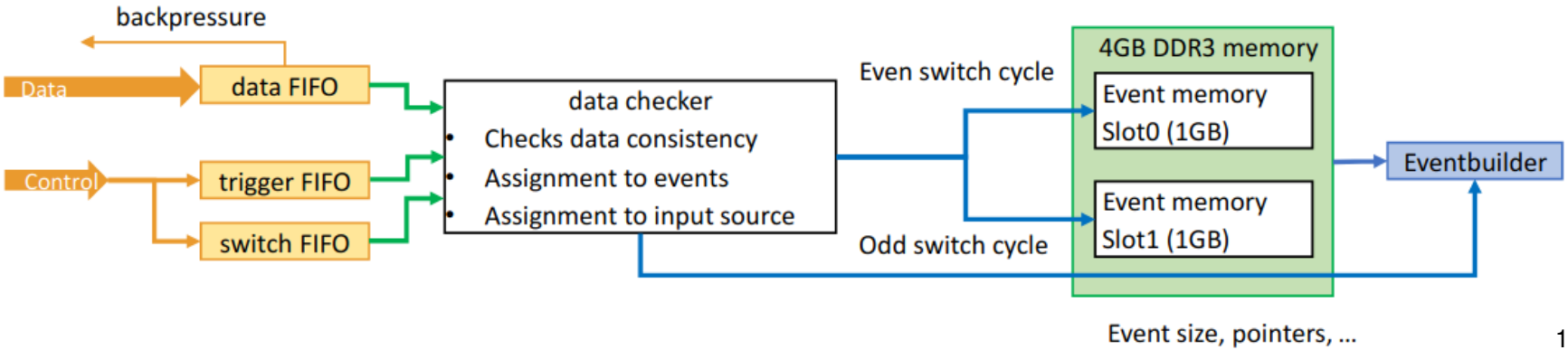


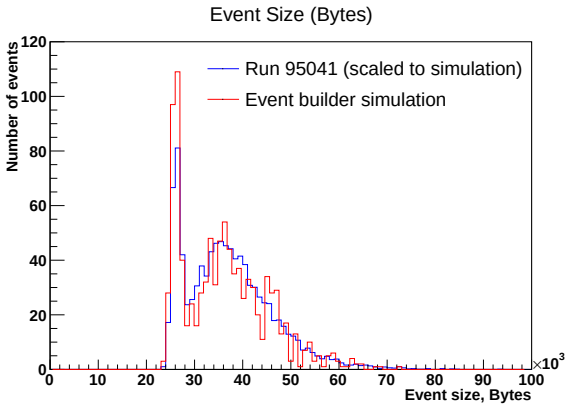
Eventbuilder Logic in PCIe Card

- Single 6.25 Gb/s 8b/10b Aurora interface
  - Data
  - Trigger information
  - Switch configuration
- Events stored in DDR3 memory
- Combination of events according to
  - event number
  - switch configuration
- Built events pushed to PCIe
- Internal bandwidth 3 GB/s



Performance in Simulation

- Simulation of **1000 events** with real event size distribution



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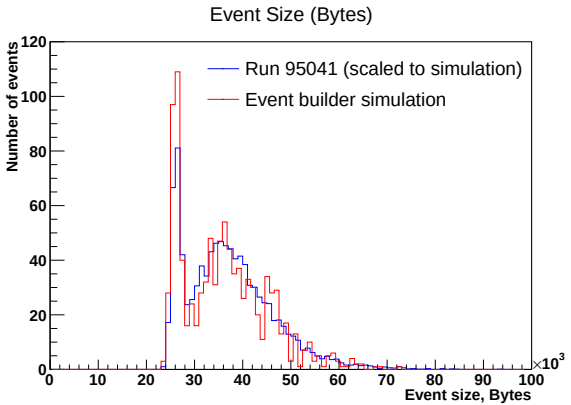

- Simulation of **1000 events** with real event size distribution
- Assumptions:
  - only event size distribution is used
  - data already available in MX
  - **100 MHz clock; 4 Gbps link rate**
  - **40 kHz trigger rate**, Poisson distribution
  - timeslice period: **500 us**

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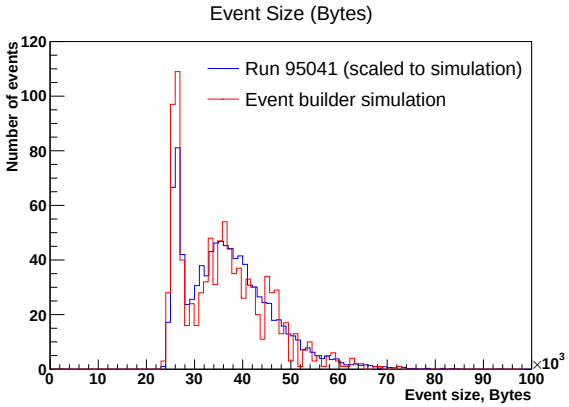

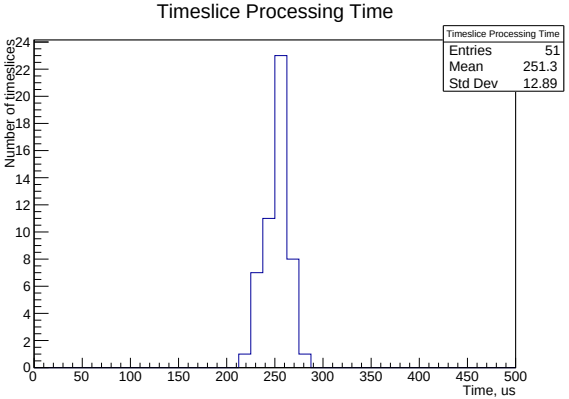

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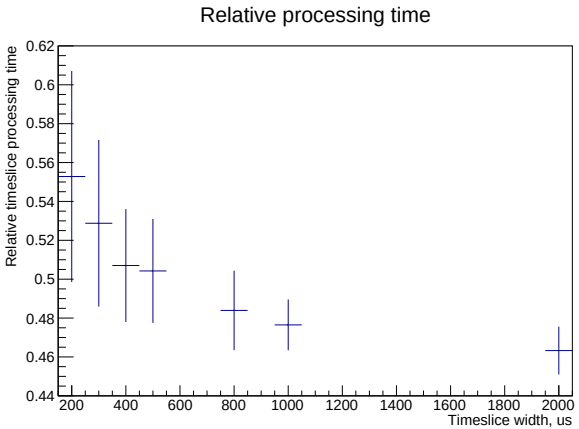
- Timeslice processing time: **251±13 us**
  - limited by the link bandwidth
  - faster processing than event generation

⇒ **Proof of the switch concept**

Performance in Simulation



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  ⇒ **Proof of the switch concept**
- Relative processing time $\frac{T_{processing}}{T_{timeslice}}$
  - smaller variation through data rate averaging

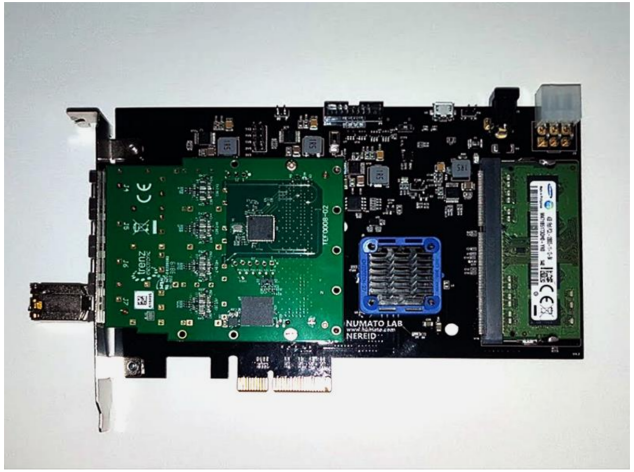
⇒ variation as safety margin for the bandwidth

Switch Hardware

- Virtex-6 VLX30T
  - custom board in AMC formfactor
  - VME carrier board
- 16 data links
  - 8x SLinks
  - 8x Aurora 8b/10b
- TCS link for synchronization
- Ethernet for slow control
- 4 GB DDR3 memory for trigger buffering

Spillbuffer Hardware

- Based on commercial hardware
  - Nereid Kintex 7 PCI Express
  - Trenz FMC – SFP adapter
- Kintex 7 XC7K160T FBG676
- 4x PCIe-Gen2 interface
- 4 GB DDR3 memory
- No dedicated TCS interface



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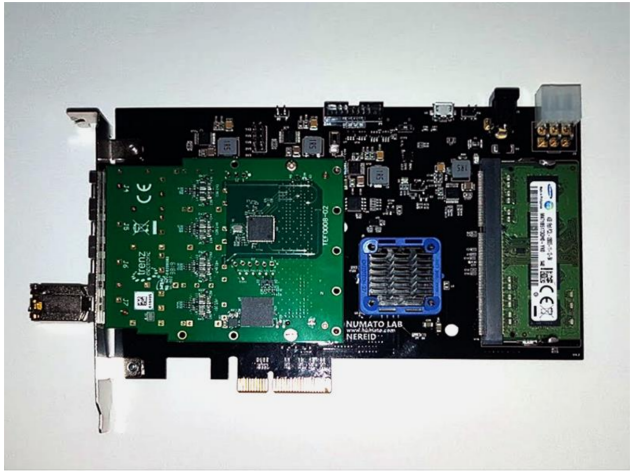
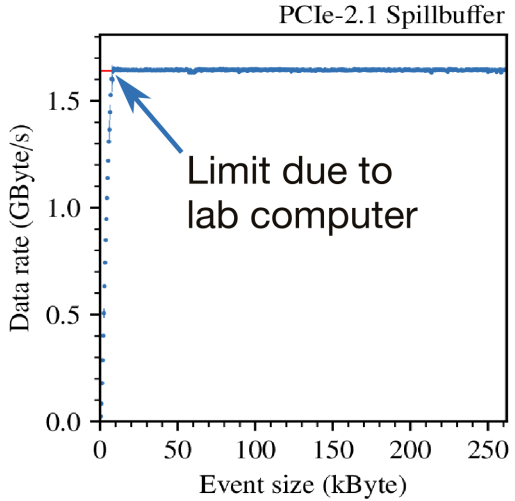


Performance tests

- Local data generator
- Scan in event sizes
- Stable data rate of > 1.6 GB/s
- Drop at small event sizes understood
  - not present in the experiment



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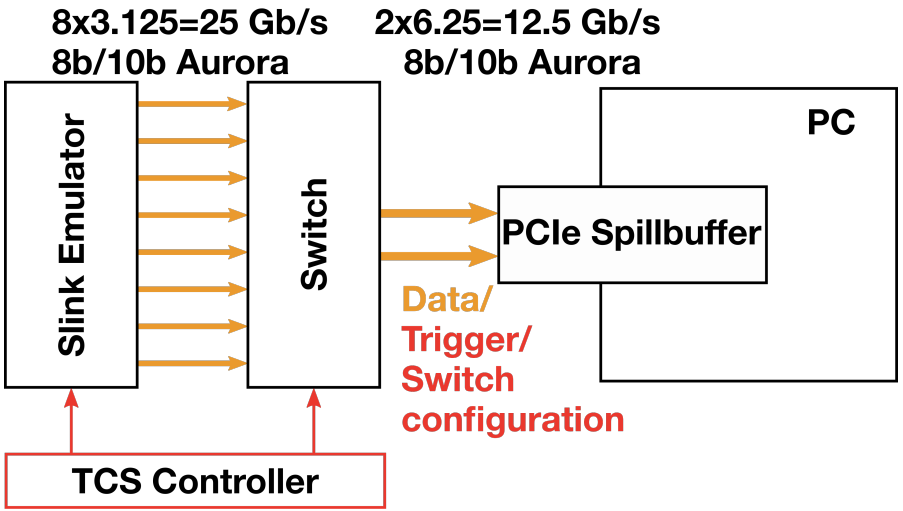
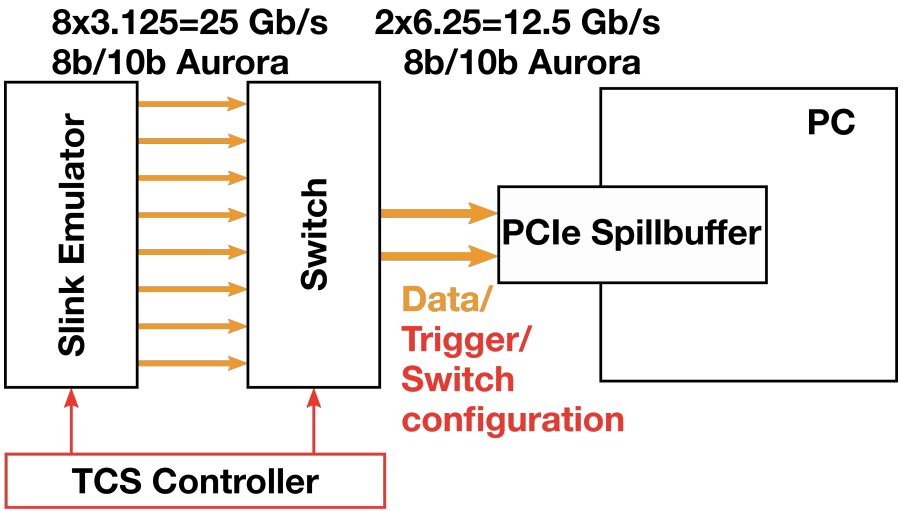


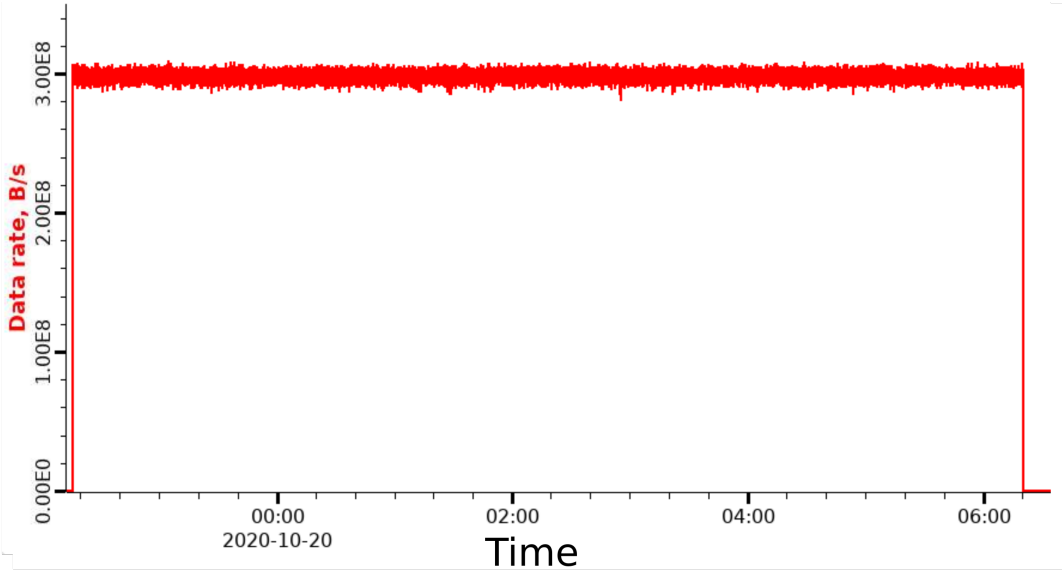
- Slink Emulator
  - TCS receiver
  - 8 data generators
  - configurable event size
  - Aurora links with back pressure
  - deep trigger FIFO

Performance in Hardware



- Slink Emulator
  - TCS receiver
  - 8 data generators
  - configurable event size
  - Aurora links with back pressure
  - deep trigger FIFO
- 2 Aurora links to the PCIe event builder node
  - data on 2nd link ignored

Test Results



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  - consistent data flow
  - correct timeslice processing

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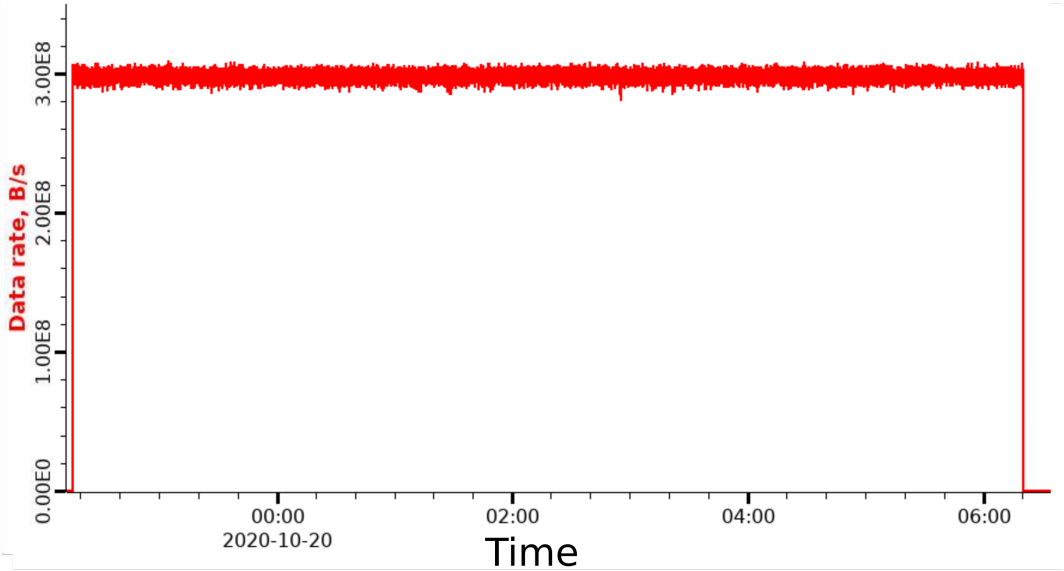

- Stable operation at **300 MB/s/link**
  - consistent data flow
  - correct timeslice processing
- Throughput limited by link bandwidth
  - can be increased by factor 2 in Virtex-6

Summary and Outlook

- Scalable event builder architecture
- Maximum performance limited by the link bandwidth
- New FPGA-based event builder at COMPASS++/AMBER
  - Switch
  - Spillbuffer
- First operation at COMPASS++/AMBER in November 2020 during the dry run