Data Acquisition Software for quality control of CBM-TOF super module detector

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1. Introduction

With the emergence of a new generation of neutron scientific apparatus characterized by high flux and high utilization efficiency, neutron scattering spectrometer requires the use of large-scale neutron detectors to achieve high precision and high efficiency of neutron detection, and to quickly complete real-time experiments, which means the large number of detector units, the large span of installation location and the complex and flexible experiment scheme. The traditional centralized trigger system and clock synchronization system often use star fan-out structure, and use dedicated links to fan out step by step, which is difficult to adapt to the needs of flexible triggering of different neutron detectors to set time window separately and switch between different trigger sources, along with the need of the wide range synchronization.

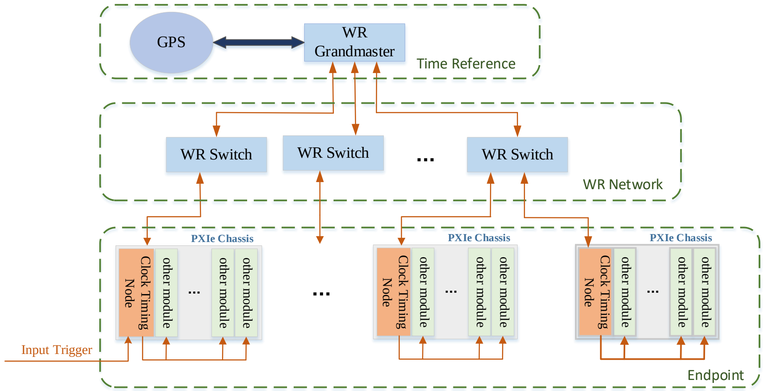

Fig. 1.The hierarchical network model of the clock trigger system

A distributed clock trigger node (CTN) based on the White Rabbit (WR) high-precision time synchronization technology was preliminarily designed to realize clock synchronization through network links and complete distributed autonomous triggering, which could also be used as a timing card of PXI Express (PXIe) chassis to further fan out the synchronous clock and trigger into each module in the chassis. As shown in Fig.1, the input trigger signal can be time-stamped by a clock trigger node, and then broadcast to multiple clock trigger nodes at different locations through WR network. These nodes can process the received message at the same time and generate the trigger autonomously according to the trigger timestamp and the set trigger delay, and then fan out it to other measurement modules through the trigger bus of the chassis. Such a distributed clock trigger system gives consideration to flexibility, integration and universality.

2. Hardware Architecture

CTN is a standard 3U-sized PXIe board working as a common WR node, which can expand the realization of multi-slot triggering and synchronization clock distribution. The prototype circuit of CTN is shown in Fig.2.

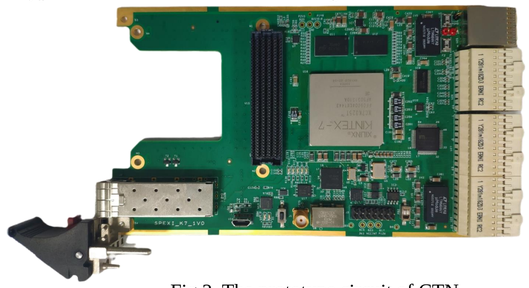

Fig.2. The prototype circuit of CTN

As shown in Fig.3, the main hardware unit of CTN can realize three main functions: time synchronization, trigger generation and distribution, data transmission and control. Xilinx kintex-7 series FPGA is selected for an optimal balance of cost, power and performance. Moreover, this device offers 16 GTX transceivers capable of operating at data rates up to 12.5 Gbps, among which 4 GTX are used to receive and forward high-rate data from FPGA Mezzanine Card (FMC), 8 GTX are used to realize 8-lane PCIe for high-speed data transmission and back-end control, and 1 GTX was used to realize WR network link.

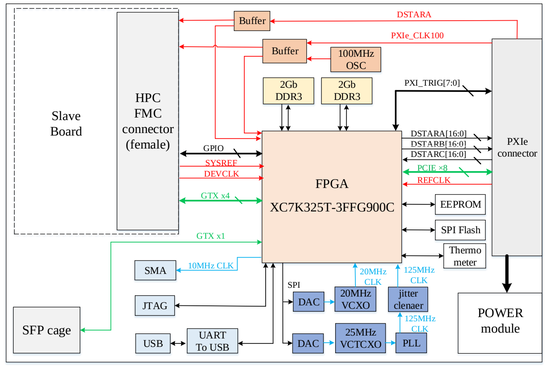

Fig. 3. The hardware block diagram of CTN

3. Time Synchronization

The function of time synchronization is based on WR technology, which realizes delay measurement between master and slave through the fiber optic link using communication protocol, and completes one-way delay compensation to achieve synchronization on both sides. The clock resources of WR node design include a local clock Phase Locked Loop (PLL) to compensate the phase of local clock and a reference clock PLL to generate the reference clock of Digital Dual Mixer Time Difference (DDMTD). The reference clock PLL of DDMTD is composed of an external Digital-to-Analog Converter (DAC) chip and a 20MHz voltage-controlled oscillator (VCO). The local clock PLL is composed of DDMTD realized by FPGA internal logic, an external DAC chip and a 25MHz VCO, the clock frequency of which is multiplied to 125MHz by an external PLL chip; moreover, an additional jitter cleaner is used in CTN to eliminate the jitter generated by the multi-level synchronization of WR network. FPGA realizes the phase locking and phase compensation of local clock by adjusting the input parameters of DAC. Besides, a SFP transceiver is required to establish the fiber optic link. The synchronized clock can be fan-out to other slots in the PXIe chassis as the system clock via the DSTARA star bus on the PXIe backplane.

4. Trigger Distribution

Real-time trigger information is received through the fiber optic link, then the corresponding trigger is generated in the internal logic of the FPGA as introduced in Part 1. Furthermore, external trigger signals can also be received with a digital IO FMC mezzanine board for IO extension, and then fan out to other modules via the PXI_TRIG trigger bus on the PXIe backplane.

5. Data Transmission and Control

CTN can be extended with different mezzanine board to realize data acquisition of ADC and TDC. The high-speed data are received through GTX, and then transmitted to the chassis controller through PCIe link on the backplane. Moreover, two DDR3 chips are used for caching high speed data for further data processing.

In addition, the chassis controller reads and writes the registers in FPGA through the PCIe link to realize the simple control function.

6. Acknowledgement

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