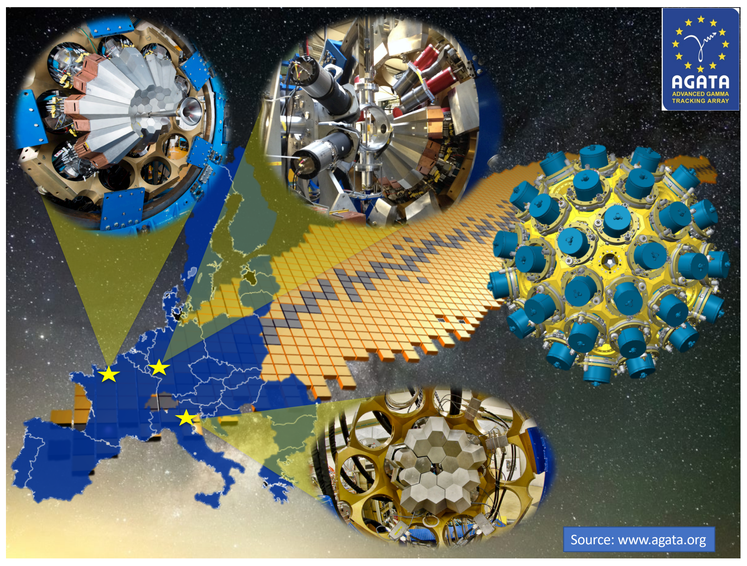
Advanced GammA Tracking Array Project

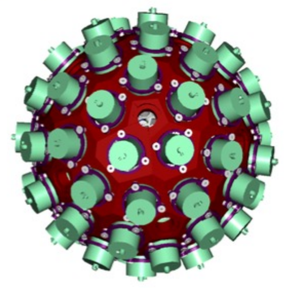
40 Gbps Readout interface STARE for the AGATA Project

Serial Transfer Acquisition and Readout over Ethernet



AGATA project

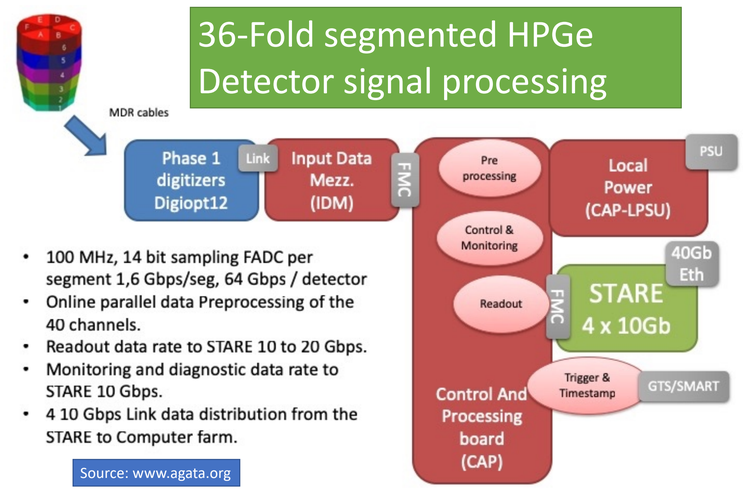
http://www.agata.org
http://agata.in2p3.fr



- 180 segmented crystals (60 triple clusters)
- 362 kg of Ge
- 82 % solid angle
- **50 kHz** Ge crystal counting rate
- ***Data reduction from 14.4 TBps to 40 TB/ week***
- **Energy resolution** & range: ~0.2%, 5 keV-180 MeV
- **Angular resolution** : ~1°
- **Efficiency**: 35 % (M_γ=1) , 20% (M_γ=30)
  Pic/Total: 50%(M_γ=1), 40% (M_γ=30)
- **Mobile detector**
- Large inner radius to accommodate ancillary devices

Source: www.agata.org

36-Fold segmented HPGe Detector signal processing



- 100 MHz, 14 bit sampling FADC per segment 1,6 Gbps/seg, 64 Gbps / detector
- Online parallel data Preprocessing of the 40 channels.
- Readout data rate to STARE 10 to 20 Gbps.
- Monitoring and diagnostic data rate to STARE 10 Gbps.
- 4 10 Gbps Link data distribution from the STARE to Computer farm.

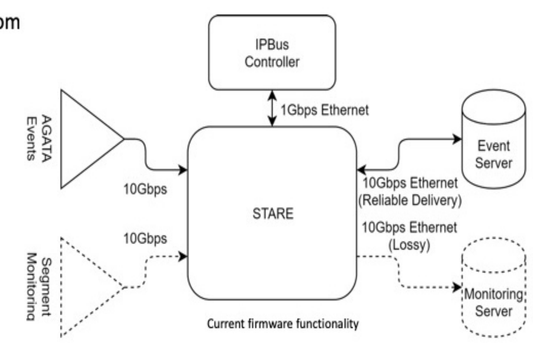
Source: www.agata.org

STARE Characteristics

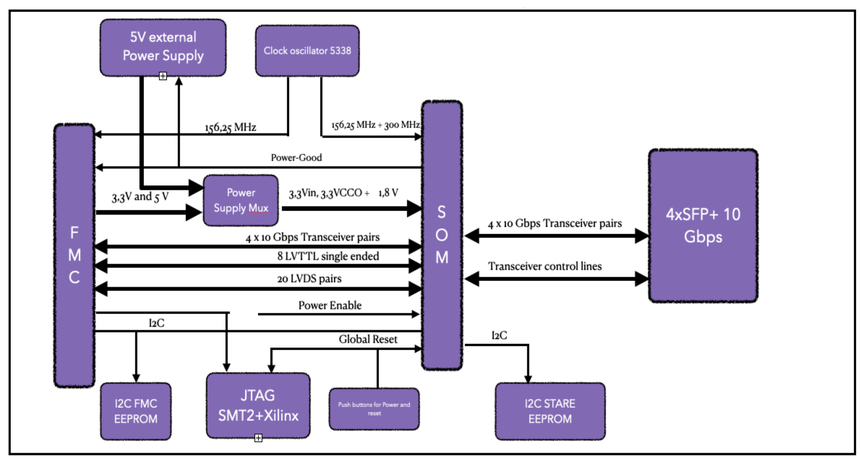
- FMC (FPGA Mezzanine Card) standard board.
- Input data rate from pre-processing : 4 x 10 Gbps (2 for data 1 for monitoring 1 spare).
- 2 Power supply sources (Internal and external PSU using hot swap mux)
- Spare LVDS I/O with the pre-processing for future use
- Full clock management for the SOM and the FMC carrier.
- Network Bandwidth up to 4 x 10 Gbps in parallel.
- Reliability UDP protocol with 0 % data loss using external Memory data rate @ 10 Gbps.
- Transmitting side uses Selective Repeat Protocole with stopping mechanism and sending side timeouts.
- Receiving side algorithm using ACK (package received) and NACK (package loss) messages.
- 1 Gbps IPBus Interface for slow control.
- On board facilities to make diagnostics and SPY data (raw data storage, local Histograms, built in self test etc...).

The STARE Concept

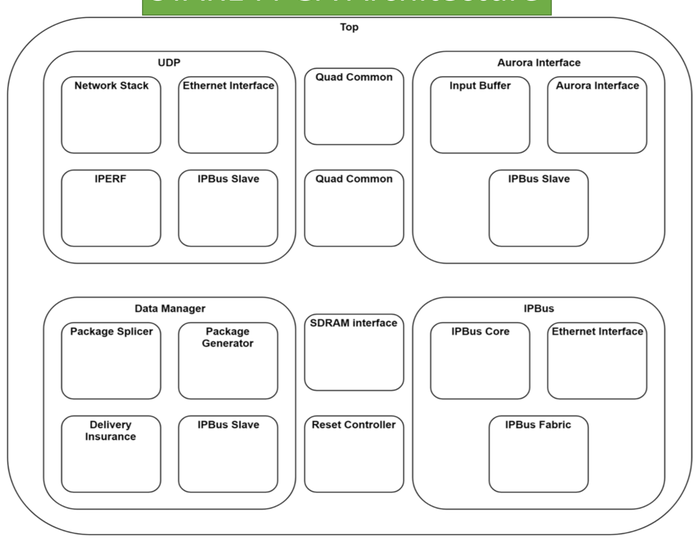
- Decoupling the custom hardware from the server farm
- Input through FMC
  - 4 Transceivers
  - 20 LVDS Pairs
- Ethernet output
  - 4 SFP+ links
  - UDP Transport
- IPBus slow control



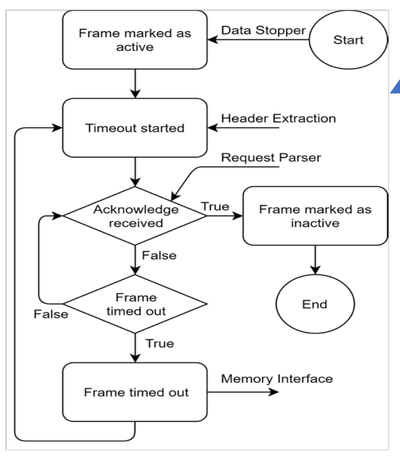
The STARE Block Diagram



STARE FPGA Architecture



Frame life External Memory Interface and the RUDP Core Algorithm.



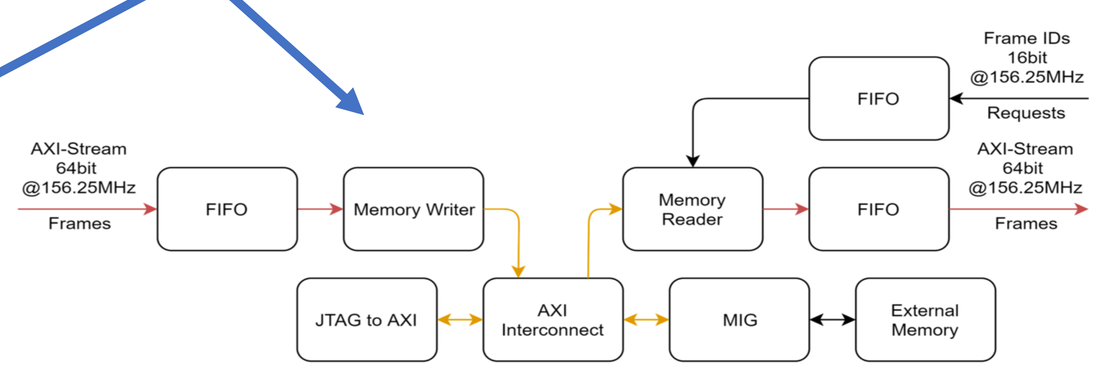
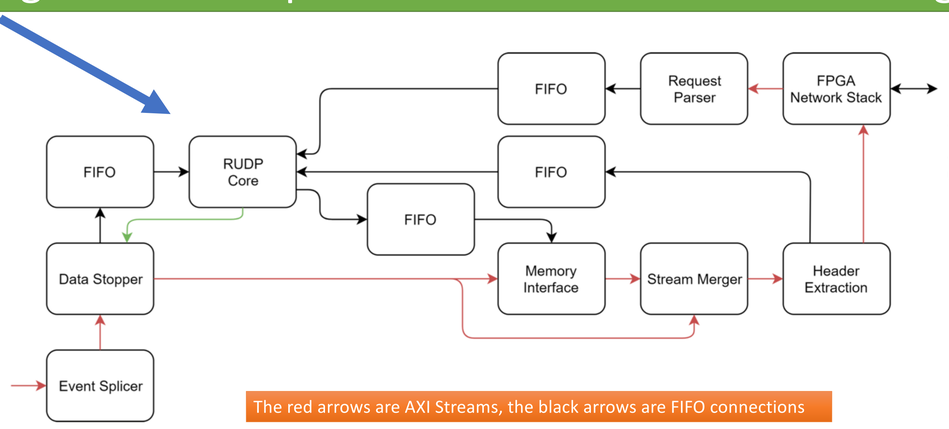


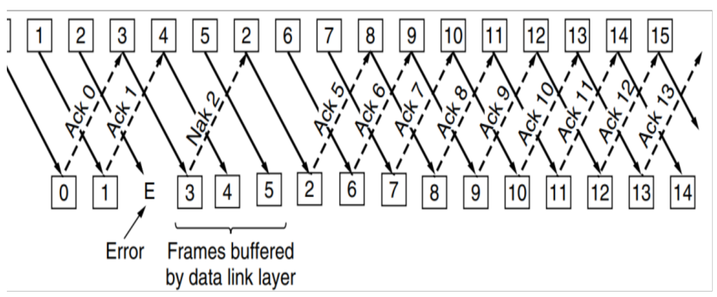
Figure 17: The implemented memory interface. The yellow arrows indicates that the connection uses the AXI4 protocol while red arrows indicate the AXI Stream protocol is used.

Transmitting and Receiving Selective Repeat Protocol architecture and Algorithm

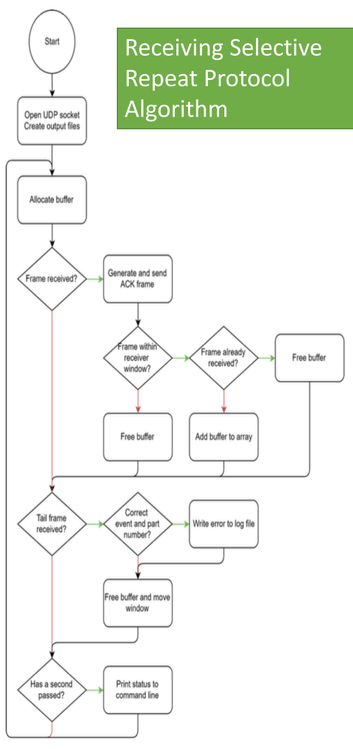


The red arrows are AXI Streams, the black arrows are FIFO connections

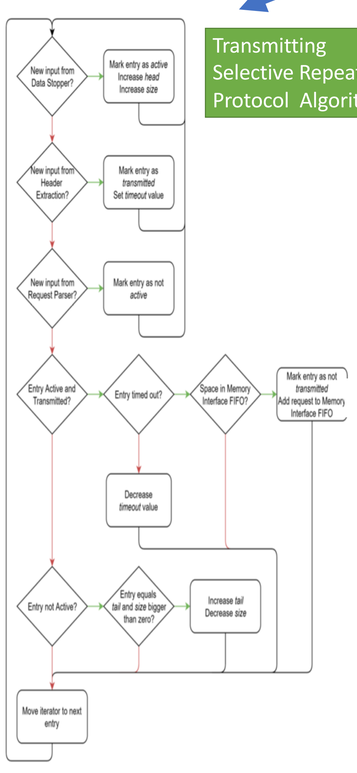
Ack (frame received) and NACK (frame lost) sequencing



Receiving Selective Repeat Protocol Algorithm



Transmitting Selective Repeat Protocol Algorithm



First Results of the Receiving Selective Repeat Protocol algorithm, Rate was limited by the server lack of computing power

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The data transfer rate is 1.19 Gbps and the total transfer rate is 1.19 Gbps
The data transfer rate is 4.92 Gbps and the total transfer rate is 4.92 Gbps
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The data transfer rate is 4.89 Gbps and the total transfer rate is 4.94 Gbps
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The data transfer rate is 4.82 Gbps and the total transfer rate is 4.99 Gbps
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Attempts were also made to increase the bandwidth further. Unfortunately the implemented Data Generator has no steps between 5Gbps and 10Gbps. When tested at 10Gbps the software only re- ported a total transfer rate of around 6Gbps. At the same time the monitors in the firmware re- ported that the full link capacity was used. The reason for this is most likely that the server is un- able to process the incoming data.
A more optimised software is therefore needed to make a final evaluation of the performance of the Selective Repeat protocol implementation. The current software could however prove that no errors occurred during transfer and showed clear signs that the implementation could reach higher speeds.

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