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Development of an 16 channel low power and high intergration readout ASIC for time projection chamber in 65 nm CMOS

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The paper presents the development of a 16 channel low power and high integration readout ASIC for time projection chamber (TPC) for the CEPC (Circular Electron Positron Collider) experiment. In order to achieve high spatial and momentum resolution, ˜1 million readout channels are required with waveform sampling in 8-10 bits and 10-40 MS/s. Power consumption became very critical and was addressed by using 65 nm CMOS process and circuit structures with less analog circuits in our design. A 16 channel TPC readout ASIC has been developed based on our previously successful prototype chips. Each channel consists of the analog front end (AFE) and a free running SAR ADC. The power consumption of the AFE and the core ADC were simulated to be 1.4 mW and 1 mW per channel respectively. The ENC of the AFE was optimized to be 263 e+ 3.7 e/pF * Cin. The input dynamic range is up to 120 fC with the integral non-linearity less than 0.37%. The digital trapezoidal filter is also under development as a pre-filter for data compression. More detailed design and test results will be given in the paper.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

Authors: Mr LIU, wei (Tsinghua University); Prof. DENG, zhi (Tsinghua University)

Presenter: Mr LIU, wei (Tsinghua University)

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