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A Prototype Design of the Readout Electronics of MRPC Detectors in CEE in HIRFL

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In Cooling storage ring External-target Experiment (CEE) in Heavy Ion Research Facility in Lanzhou (HIRFL), Multi-gap Resistive Plate Chambers (MRPC) detectors are utilized for high precision Time Of Flight (TOF) measurement. Especially for some Internal TOF (iTOF) detectors, which is designed to identify the particles scattered after the ion beam hit the target, a very high precision of the time measurement (detector together with the electronics are required to be less than 50 ps in total) is required, which requires the time precision of the readout electronics to be less than 10 ps RMS. Based on our previous work on the readout electronics system of the start time (T₀) detector in CEE, we design this prototype to verify our scheme, which contains a Front-End Electronics (FEE) module utilizing NINO ASIC to achieve the low-noise, high-precision discrimination and a Time Digitization Module (TDM) with double-chain Tapped Delay Line (TDL) Field Programmable Gate Array (FPGA) Time to Digital Convertors (TDCs) implemented in Xilinx Artix-7 FPGA. By constraining the TDLs at appropriate positions and choosing a main clock of 320 MHz according to the transmission speed of the hit signal on the TDL, we optimize the Differential NonLinearity (DNL) of the TDL. According to the test results, a 7.1 ps RMS time precision of the TDM is achieved. We also test the performance of the whole system under different input signal charges and the results indicate that the prototype achieves the expectations.

Minioral

Yes

IEEE Member

No

Are you a student?

Yes

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