A Prototype Design of the Readout Electronics of MRPC Detectors in CEE in HIRFL

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Introduction

In Cooling storage ring External-target Experiment (CEE) in Heavy Ion Research Facility in Lanzhou (HIRFL), Multi-gap Resistive Plate Chambers (MRPC) detectors are utilized for high precision Time Of Flight (TOF) measurement. Especially for some Internal TOF (iTOF) detectors, which is designed to identify the particles scattered after the ion beam hit the target, a very high precision of the time measurement (detector together with the electronics are required to be less than 50 ps in total) is required, which requires the time precision of the readout electronics to be less than 10 ps RMS. Based on our previous work on the readout electronics system of the start time (T0) detector in CEE, we design this porotype to verify our scheme, which contains a Front-End Electronics (FEE) module utilizing NINO ASIC to achieve the low-noise, high-precision discrimination and a Time Digitization Module (TDM) with double-chain Tapped Delay Line (TDL) Field Programmable Gate Array (FPGA) Time to Digital Convertors (TDCs) implemented in Xilinx Artix-7 FPGA. By constraining the TDLs at appropriate positions and choosing a main clock of 320 MHz according to the transmission speed of the hit signal on the TDL, we optimize the Differential NonLinearity (DNL) of the TDL. According to the test results, a 7.1 ps RMS time precision of the TDM is achieved. We also test the performance of the whole system under different input signal charges and the results indicate that the prototype achieves the expectations.

The Structure of the Readout Electronics

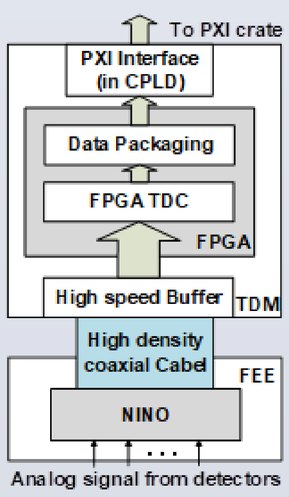

Fig. 1. Block diagram of the readout electronics system of iTOF.

The analog signals from the MRPC detectors are firstly amplified and discriminated by the NINO ASIC on the FEE module located near the detectors. Via a 5-meter high density coaxial cable of SAMTECH Inc., the output hit signals (LVDS standard) are transmitted to the TDM. After buffered by a high speed repeator, the hit signals are finally fed into FPGA on the TDM for digitization. Finally, the time measurement results are transmitted though the PXI interface to the Single Board Computer (SBC) in the Slot 0 of the crate.

The Design of the Double-Chain TDL FPGA TDC

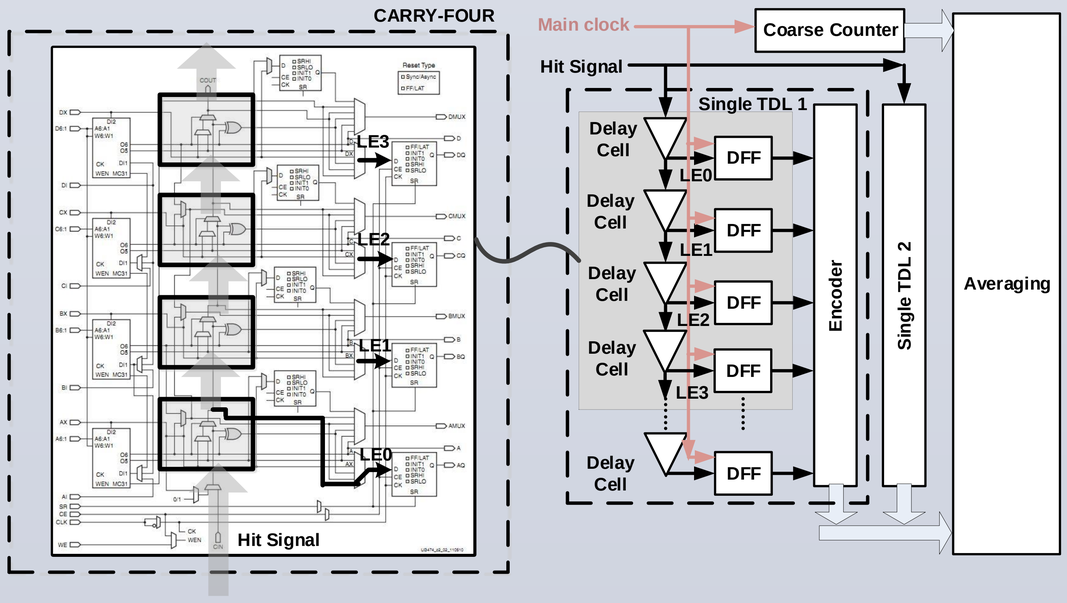

Fig. 2. Block diagram of the double-chain TDL FPGA TDC.

The structure of the TDL employed in our design is shown in Fig.2. After the hit signal being detected by the pulse detector, at the rising edge of the main clock, the D flip-flop array connected to the CARRY-FOURs records the fine time information in the form of thermometer code. The fine time information together with the coarse time provides the arrival time of the hit signal.

One of the most significant origins of the Differential NonLinearity (DNL) is that the TDL is implemented across the LAB boundaries. In Artix-7 FPGA, “ultra-wide bins” exist where the TDL is implemented across two different clock regions.

In our work, firstly, we estimate that it takes 69.4ps for the leading edge of the hit signal transmit across one CARRY-4. And we notice that, depending on the structure of the slice resource, the longest carry chain that can be implemented in the Artix-7 FPGA without crossing two different clock regions contains fifty CARRY-4s at most. Subsequently, we set the frequency of the main clock to 320 MHz, and constrain the first CARRY-4 of the TDL at the bottom of one clock region, which guarantee the hit signal not transmit beyond this clock region within one main clock period. Finally, to achieve the high time precision, we combine two such implemented TDLs into one TDC channel. We average the time measurement results of the two channels and the final arrival time of the hit signal is obtained.

Testing Results

1) Performance of the Single-Chain TDL TDC. Fig.4 shows the DNL of one single-chain TDL TDC channel. Fig.5 shows the time precision of two single-chain TDL TDC channels. The result indicates that the time precision of one single channel is 10.0 ps RMS.

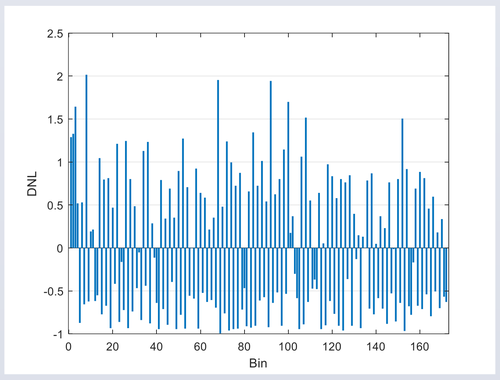

Fig.4. DNL of one single-chain TDL TDC channel.

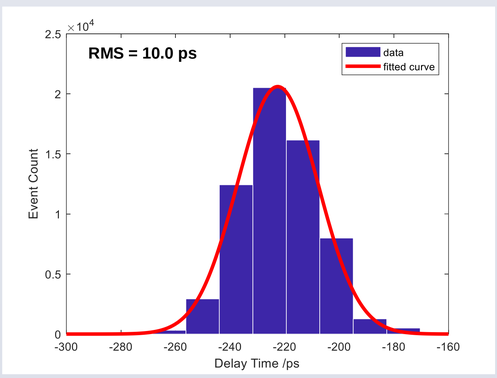

Fig.5. Time precision of the single-chain TDL TDC.

To evaluate the effects of the constraint of the TDL, we implemented a TDC channel with the first level of CARRY-4 constrained at the middle position of the clock region. As we anticipated, bin No.100 is an “ultra-wide bin” exists where the TDL cross the clock region. We test the time precision of this channel, and the result is 14.9 ps, worse than the channel implemented at the bottom of the clock region.

2) Performance of the Double-Chain TDL TDC. Fig.6 shows the time precision of two double-chain TDL TDC channels. The result indicates that the time precision of one single channel is 7.1 ps RMS.

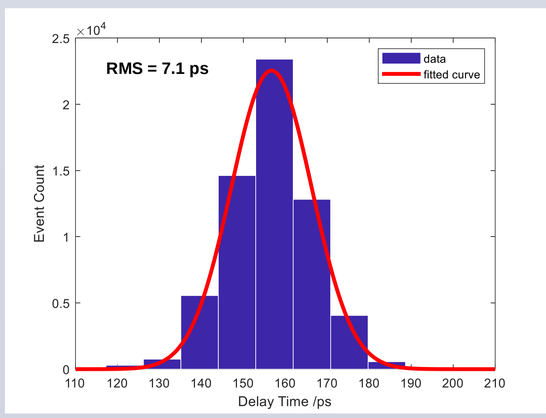

Fig.6. Time precision of double-chain TDL TDC channels.

3) Performance of the Prototype Readout Electronics. We test the electronics system, the time precision varies from 7.8 to 9.0 ps RMS while the charge of the input signal varies from 2000 to 200fC. The result indicates that the time precision of the system is better than 10 ps RMS.

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