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Readout firmware of the Vertex Locator for LHCb Run 3 and beyond

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The new LHCb Vertex Locator for LHCb, comprising a new pixel detector and readout electronics will be installed in 2020 for data-taking in Run 3 at the LHC. The electronics centres around the “VeloPix” ASIC at the front-end operating in a triggerless readout at 40 MHz. A custom serialiser, called GWT (Gigabit Wireline Transmitter) and associated custom protocol have been designed for the VeloPix. The GWT data are sent from the serialisers of the VeloPix at a line rate of 5.12 Gb/s, reaching a total data rate of 2-3 Tb/s for the full VELO detector.

Data are sent over 300 m optic-fibre links to the control and readout electronics cards for deserialisation and processing in Intel Arria 10 FPGAs. Due to the VeloPix triggerless design, latency variances up to 12 μs can occur between adjacent datagrams. It is therefore essential to buffer and synchronise the data in firmware prior to onward propagation or suffer a huge CPU processing penalty. This paper will describe the architecture of the readout firmware in detail with focus given to the re-synchronisation mechanism and techniques for clusterisation. Issues found during readout commissioning, and scaling resource utilisation, along with the their solutions, will be illustrated. The latest results of the firmware data processing chain be presented as well as the verification procedures employed in simulation. Challenges for the next generation of the detector will also be presented with ideas for a readout processing solution.

Minioral

Yes

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No

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